VI Scuola Nazionale "Rivelatori ed Elettronica per Fisica delle Alte Energie, Astrofisica, Applicazioni Spaziali e Fisica Medica

Noise performance of 65 nm CMOS transistors exposed to ionizing radiation

26th March 2015

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Activity overview

Main purpose:

- Evaluate ionizing radiation effects on the analog performance of TSMC 65 nm CMOS devices after exposure to a TID of 1Grad

Test chip:

- 1 chip with test devices submitted in June 2014 (delivered in September 2014)
- Test devices bonded in a QFN48 “Open-Pak” package
- 2 bonding diagrams

Measurements:

- Static and signal parameters

  measured by means of an Agilent E5270B Precision Measurement Mainframe with E5281B SMU Modules
- Noise in the devices channel current

  measured by means of a purposely developed wide-band interface circuit, which allows for noise measurements in the 100 Hz-100 MHz range

ATLAS-CMS RD53 Collaboration

This activity has been carried out in framework of RD53 collaboration and the aim of this project is the design of the next generation of hybrid pixel readout chips to enable the ATLAS and CMS phase 2

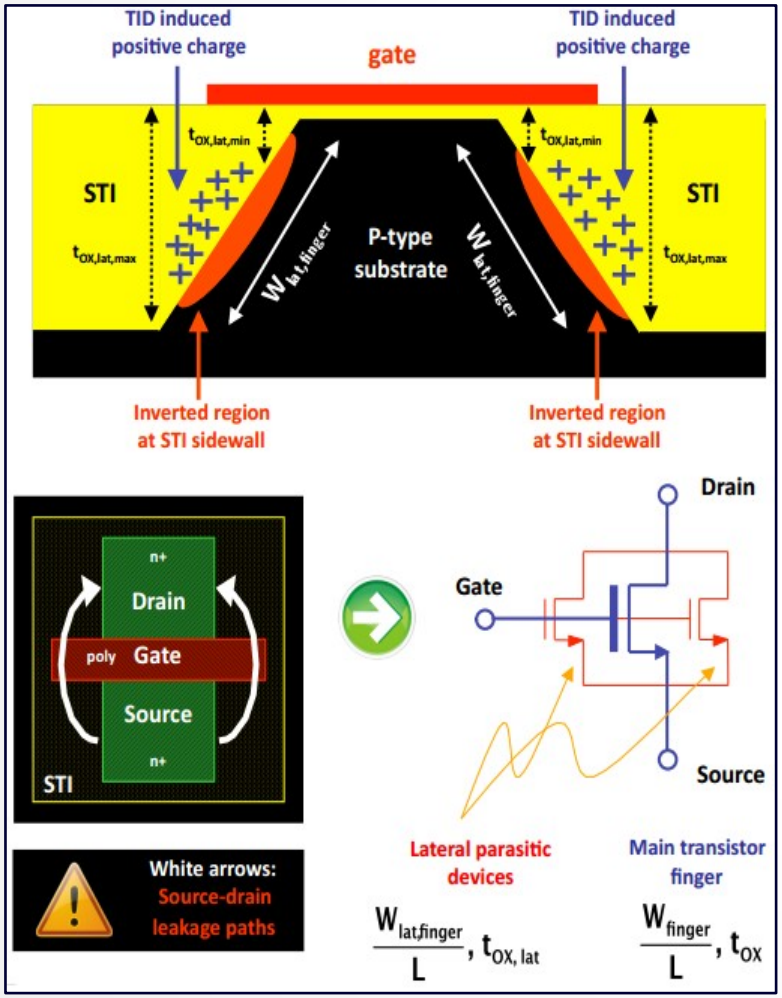
- Similar/identical requirements, same technology choice and limited availability of rad hard IC design experts in HEP makes this ideal for a close CMS-ATLAS RD collaboration
- Institutes: 17
  - ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, RAL, UC Santa Cruz.
  - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Torino
- Collaborators: 99, ~50% chip designers
- Collaboration organized by Institute Board (IB) with technical work done in specialized Working Groups (WG)
- Initial work program covers 3 years to make foundation for final pixel chips

WG1. Radiation test/qualification

- Qualification of technology to 10 MGy TID, 10 16 n.eq./cm^2
- Transistor simulation models after irradiation
- Evaluation of logic cell libraries after irradiation
- Expertise on radiation effects in 65nm

Ionizing radiation effects in sub-100 nm CMOS

Radiation induced positive charge is removed from thin gate oxides by tunneling (which also prevents the formation of interface states)

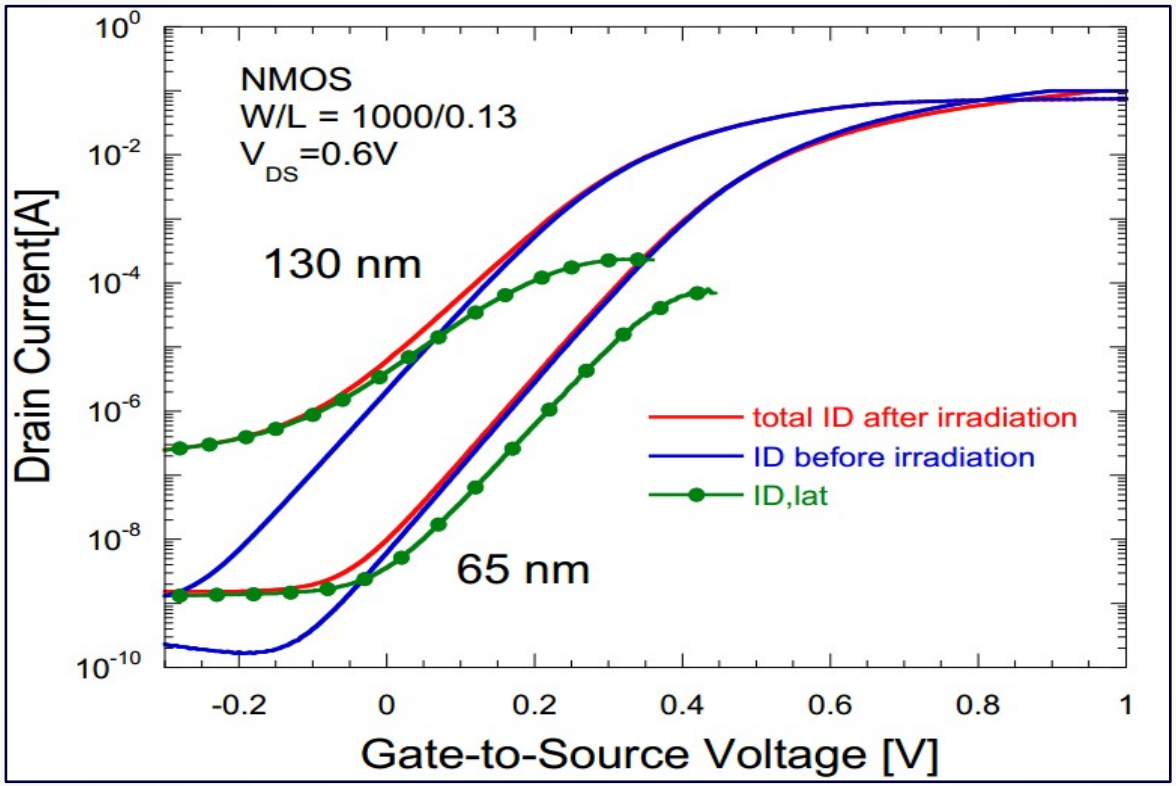


- Isolation oxides remain thick (order of 100 nm) also in nanoscale CMOS, and they are radiation soft
- In NMOS, edge effects due to radiation-induced positive charge in the STI oxide generate sidewall leakage paths
- In an interdigitated device, this can be modeled considering that two lateral transistors for each finger are turned on
- The effect of these parasitic devices on the noise and static characteristics must be carefully evaluated

Previous measurements

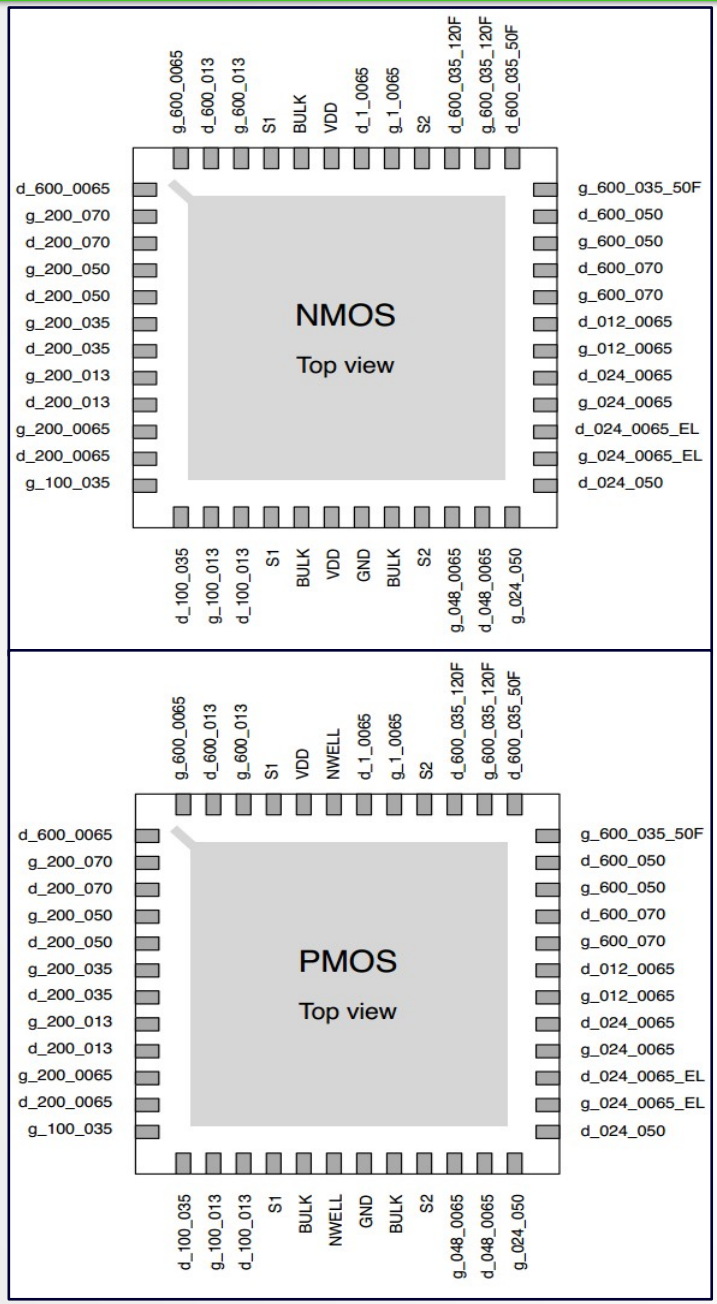
(September 2013)

I_D- V_{GS} before and after exposure to a 10 Mrad total dose of γ-rays



- A larger amount of lateral leakage takes place in 130 nm devices
- The smaller I_D,lat of 65 nm devices suggests that the sensitivity to positive charge buildup in STI oxides is mitigated by the higher doping of the P-type body with respect to less scaled processes

Available geometries and bonding diagrams



W [µm]	L [µm]	Note
0.12	0.065	
0.24	0.065	
	0.065	EL
	0.50	
0.48	0.065	
1	0.065	
100	0.13	
	0.35	
200	0.065	
	0.13	
	0.35	
	0.50	
	0.70	
600	0.065	
	0.13	
	0.35	50f
	0.35	120f
	0.50	
	0.70	

Pre and post-irradiation measurements

Static measurements

For all avaliable geometries of NMOS and PMOS

$I_D - V_{GS}$ characteristics

- V_{GS} from -0.3 V to 1.2 V with 5 mV steps
- V_{DS} form 0 V to 1.2 V with 0.2 V steps and V_{DS} = 10 mV

$I_D - V_{DS}$ characteristics

- V_{DS} from 0 V to 1.2 V with 5 mV steps
- V_{GS} from 0 V to 1.2 V with 0.2 V steps

Noise measurements:

For NMOS and PMOS devices with W = 100, 200 and 600 µm

Frequency range → 100 Hz - 100 MHz

Bias conditions →

- $|V_{DS}|$ = 0.6 V
- I_D = 20, 50, 100, 250 and 500 µA

Irradiation Procedure and Plans

Radiation source → X-Ray facilities at LNL, Legnaro (PD)

Bias conditions during irradiation

- NMOS with V_{GS} = 1.2 V and V_D= V_S= 0 V
- PMOS with V_{GS}= V_D= V_S= 0 V

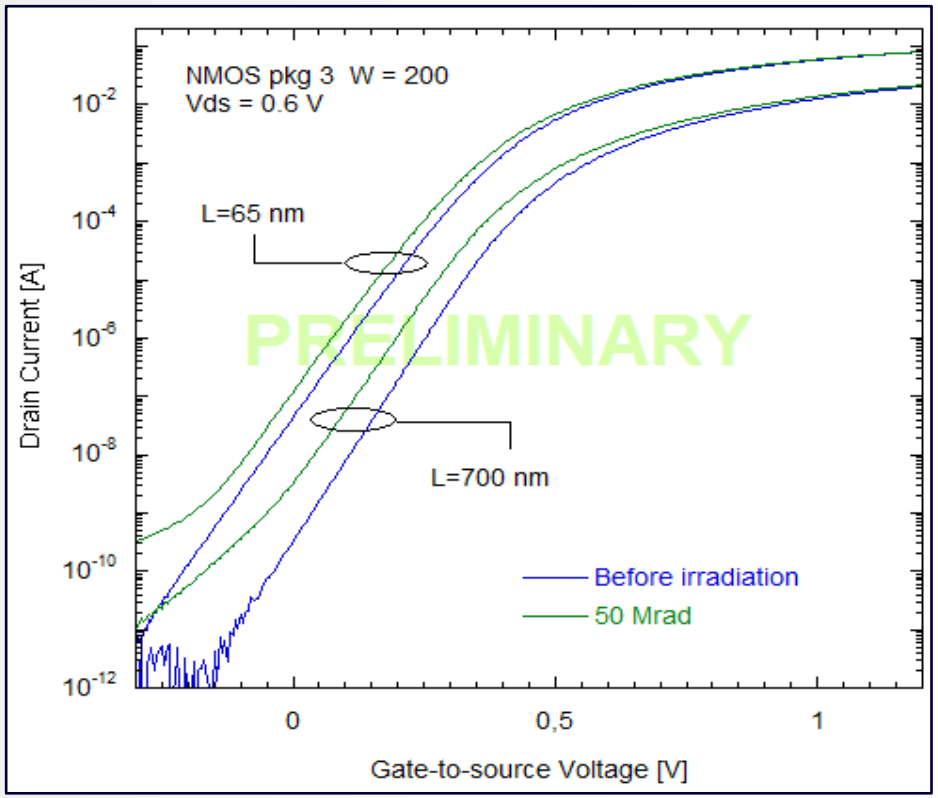
Temperature

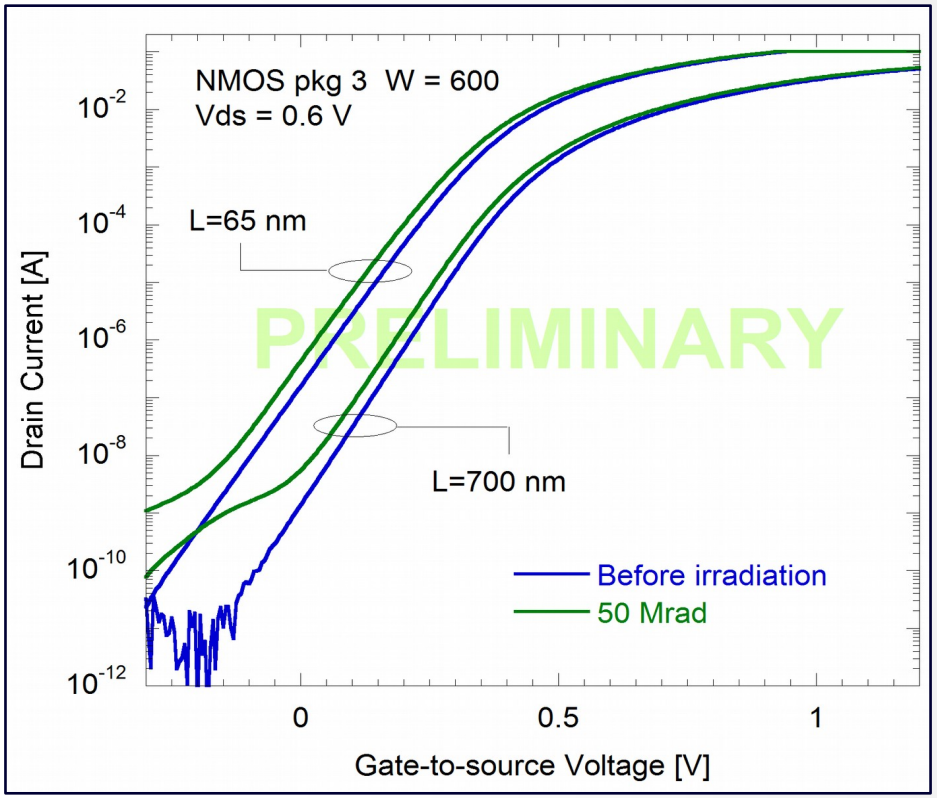
- Irradiaton and measurements: ambient
- Storage ≈ 0 °C

Irradiaton Plan

1 NMOS Chip			1 PMOS Chip		
TID [Mrad]	Step [Mrad]	Date	TID [Mrad]	Step [Mrad]	Date
50	50	Feb			
100	50	Mar	100	100	Mar
500	400	Apr	500	400	Apr
1000	500	May	1000	500	May

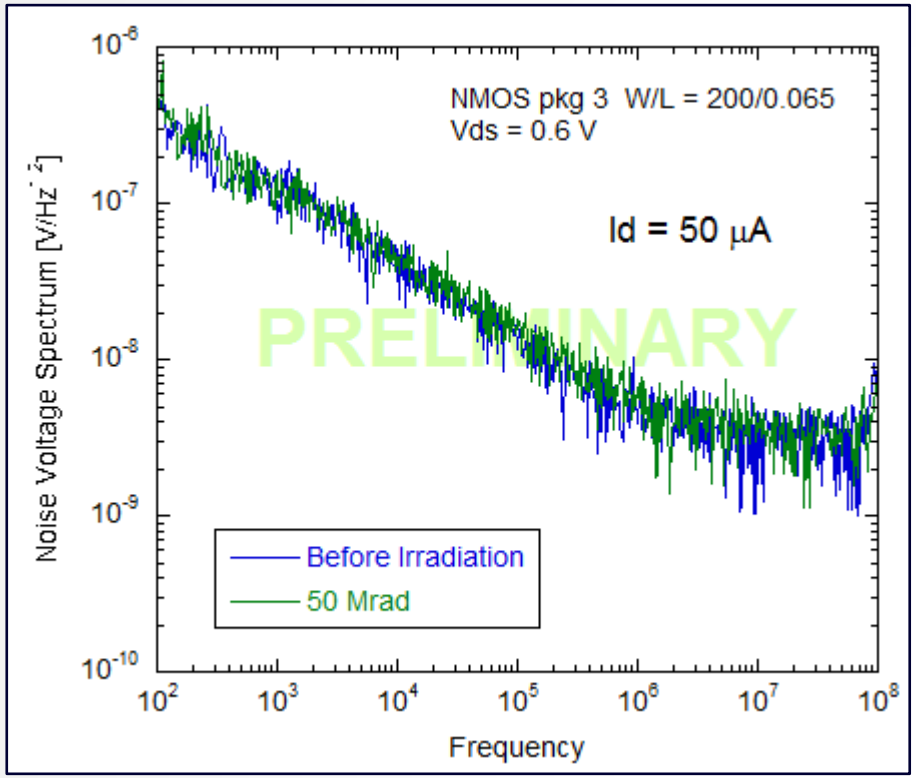
Drain Current

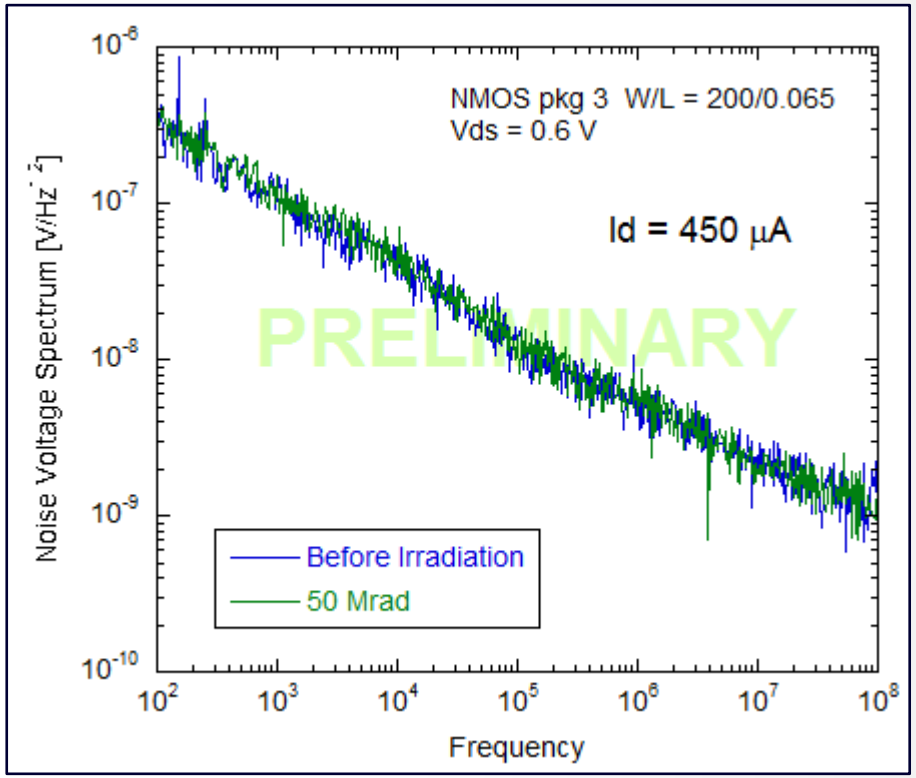




- **Devices with L = 65 nm:** an increase in the subthreshold current detected for both channel widths W = 200 μm and W = 600 μm
- **Devices with L = 700 nm:** a more marked increase in the subthreshold current detected for the device with channel widths W = 200 μm

Noise





- No increase in the 1/f noise region detected
- No increase in the white noise region detected
- Same results for low and high current density

Summary

Bg/Pv Group activity mainly concerned with the evaluation of ionizing radiation effects on the analog performance of TSMC 65 nm CMOS devices

Status

- 1 chip of NMOS devices exposed to a first step of ionizing radiation up to a total dose of 50 Mrad of X-ray
- Static and noise measurements performed before and after irradiation
- Processing of measurement results in progress

Plan

- Next irradiation steps of NMOS and PMOS chips with X-ray scheduled for March
- Irradiation with 3 MeV proton beam (CN accelerator, INFN-LNL in Padova) scheduled for April