A new analog front-end for the HL_LHC upgrade of the CMS experiment

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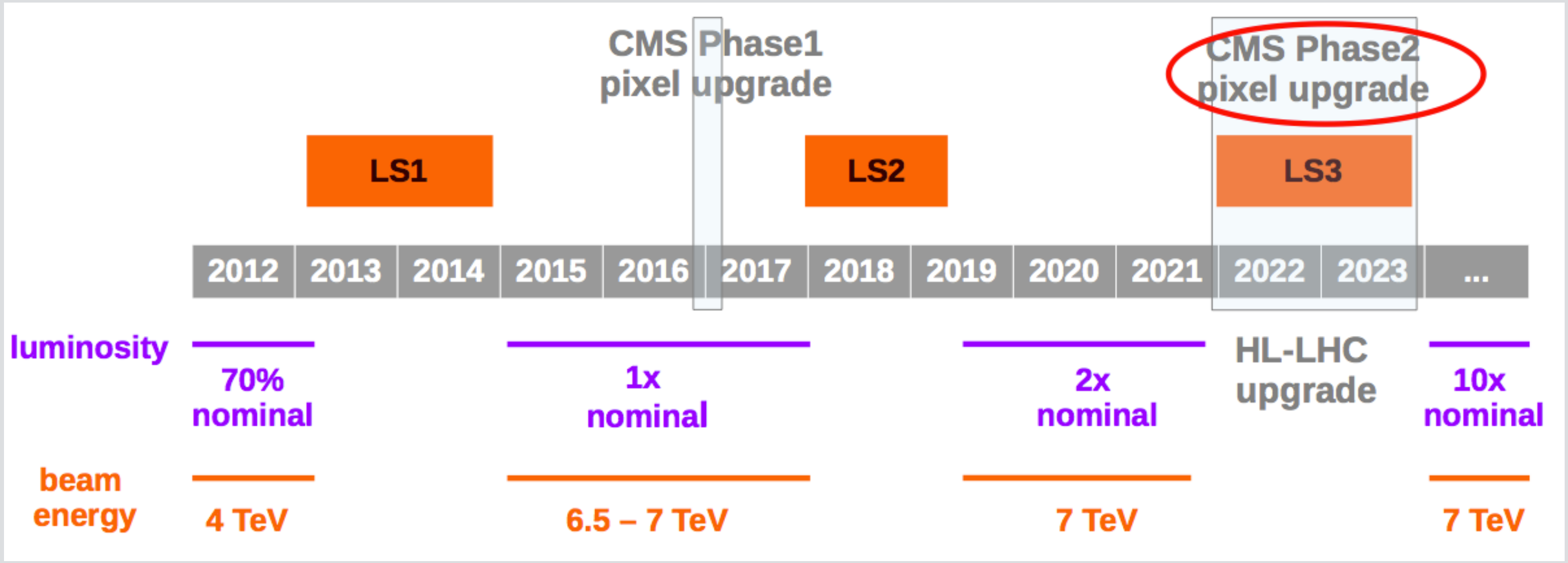
The HL_LHC upgrade



- During the phase 2:
  - The luminosity of the machine will be increased by an order of magnitude (**$5x10^{34}$ / 10^{35} cm^{-2} s^{-1} foreseen**)
  - Unprecedented Pile-Up conditions (**140-200 collisions per event**)
  - Unprecedented radiation levels (around **1 GRad in 10 years**)

The HL_LHC upgrade

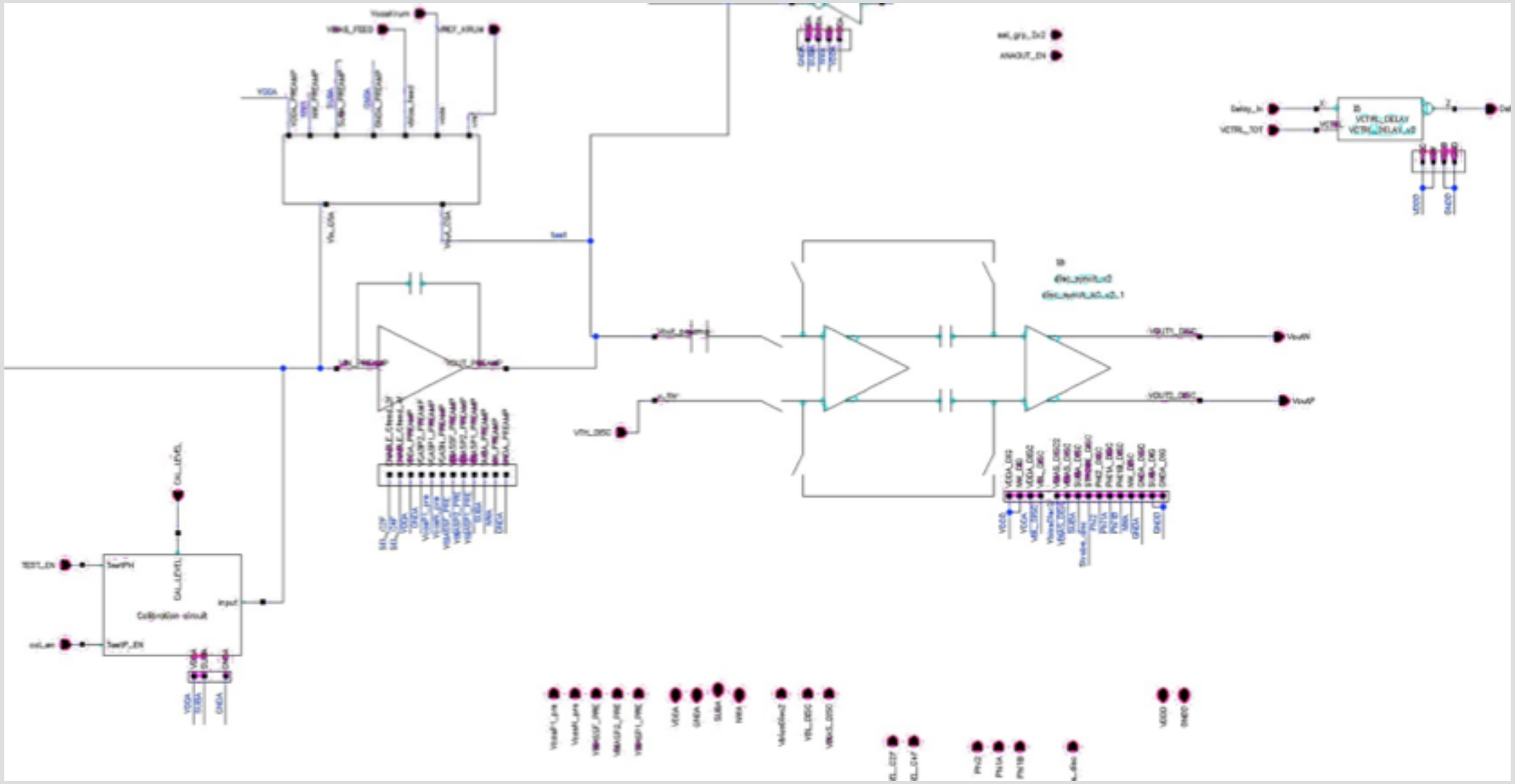
PARAMETER or FEATURE	1st generation LHC phase 0	2nd generation LHC Phase 1	3rd generation LHC Phase 2
Max Particle Flux	~50 MHz/cm^2	~200 MHz/cm^2	~500 MHz/cm^2
Max Pixel Flux	200 MHz/cm^2	600 MHz/cm^2	2 GHz/cm^2
Rad. Hardness	1.5 MGy	3.5 MGy	10 MGy
Pixel Dimension	100x150 mm^2 50x400 mm^2	100x150 mm^2 50x250 mm^2	25x150 mm^2 50x100 mm^2
Signal Threshold	2500-3000 e$^-$	1500-2000 e$^-$	~1000 e$^-$
L1 Trigger Latency	2-3 us	4-6 us	6-20 us
Power Budget	~0.3 W/cm^2	~0.3 W/cm^2	<0.4 W/cm^2
Electronics technology node	250nm CMOS	250nm CMOS (CMS) 130nm CMOS (ATLAS)	65nm CMOS

- **New readout chip required**
  - The present one can not survive the extreme Phase 2 conditions
- RD53, a CMS-ATLAS collaboration, has been developed in order to design the new chip
- INFN contribute: CHIPIX 65 collaboration, a group 5 project approved in 2013 for the 2014-2016 period. 7 INFN sections involved (TO, MI, BA, PD, PI, PV, PG)

Main challenges

- Surviving the extreme HL_LHC conditions
- Very **high particle flux** (2 GHz/cm^2)
- Maintaining or improving the detector performance
  - **New pixel size** (50x50 μm^2 or 25x100 μm^2)
- **Low power** architecture
  - Required to maintain the material budget (cooling) as low as possible
  - 0.4 W/cm^2 -> 10 μW per pixel

Analog Front-End studied in Torino

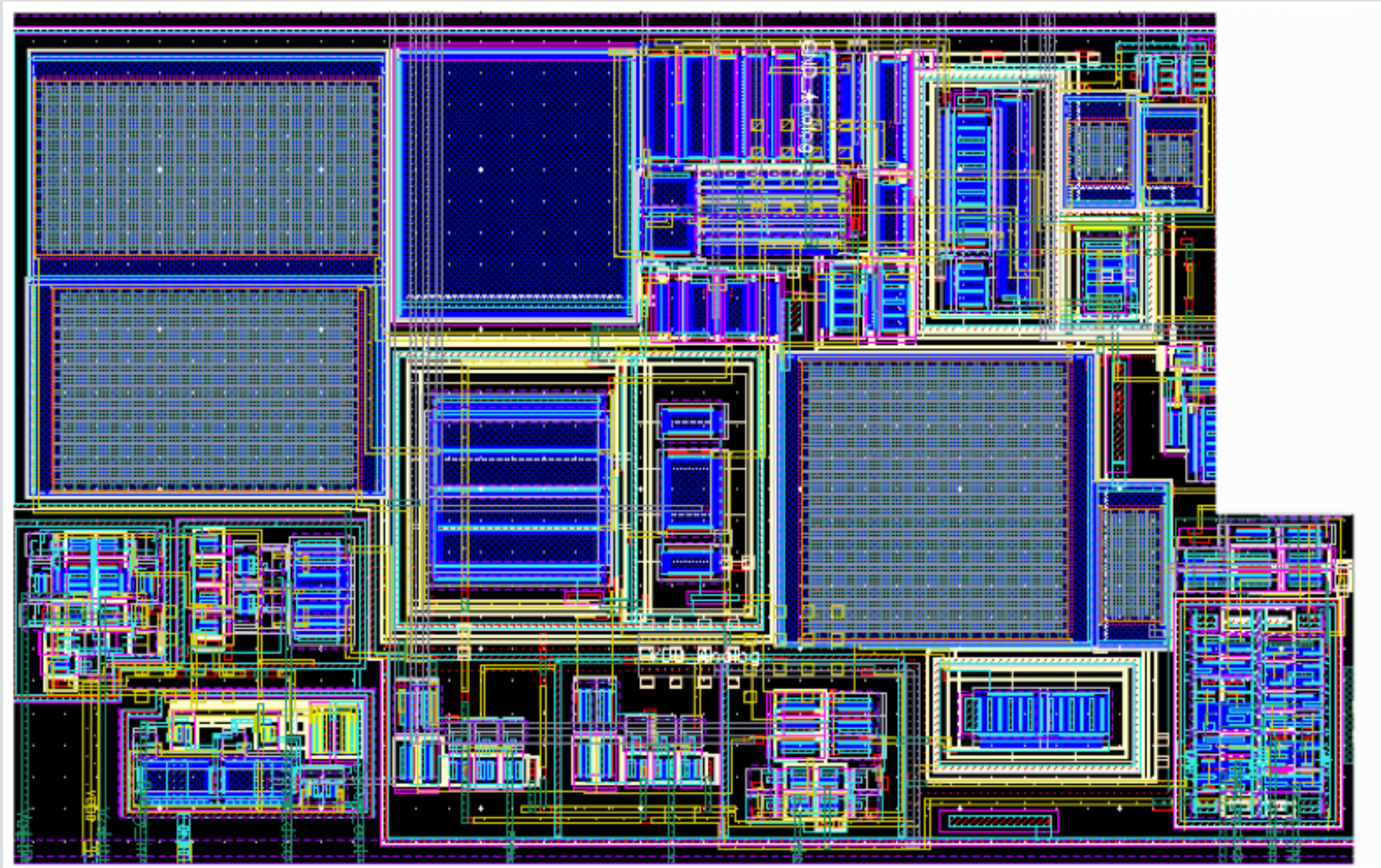


- PREAMP: **one stage CSA** with Krummenacher feedback
- COMPARATOR: **synchronous** with latch, AC coupled
- THRESHOLD TRIMMING: made by hardware, offset self-compensated
- FAST ToT: **local oscillator** inside the comparator

Performance summary

- **Low power**: around 5.5 μW/pixel (analog part)
  - Compliant with the requirements
- **Low noise**: around 100e- for Cdet = 100 fF
  - Ok for a threshold of 1 ke^-
- **Fast ToT**: 30ke^- signal into max 250 ns
  - Changing the feedback current it can be run in fast or slow ToT mode
- **No threshold trimming via DAC**
  - Hardware solution (corrections stored in capacitors)
- Dimensions: area of around 26x39 μm^2

VFE layout



- **CSA + Disc + Calibration circuit + Fast_Tot = 26x39 um2**
  - MOM (Metal-Oxide-Metal) capacitors used

- Room to make it smaller -> Work in progress on a new version

Power consumption

- Static power consumption around 4.5 μW
  - Preamplifier -> 3 μW
  - Comparator -> 1.5 μW

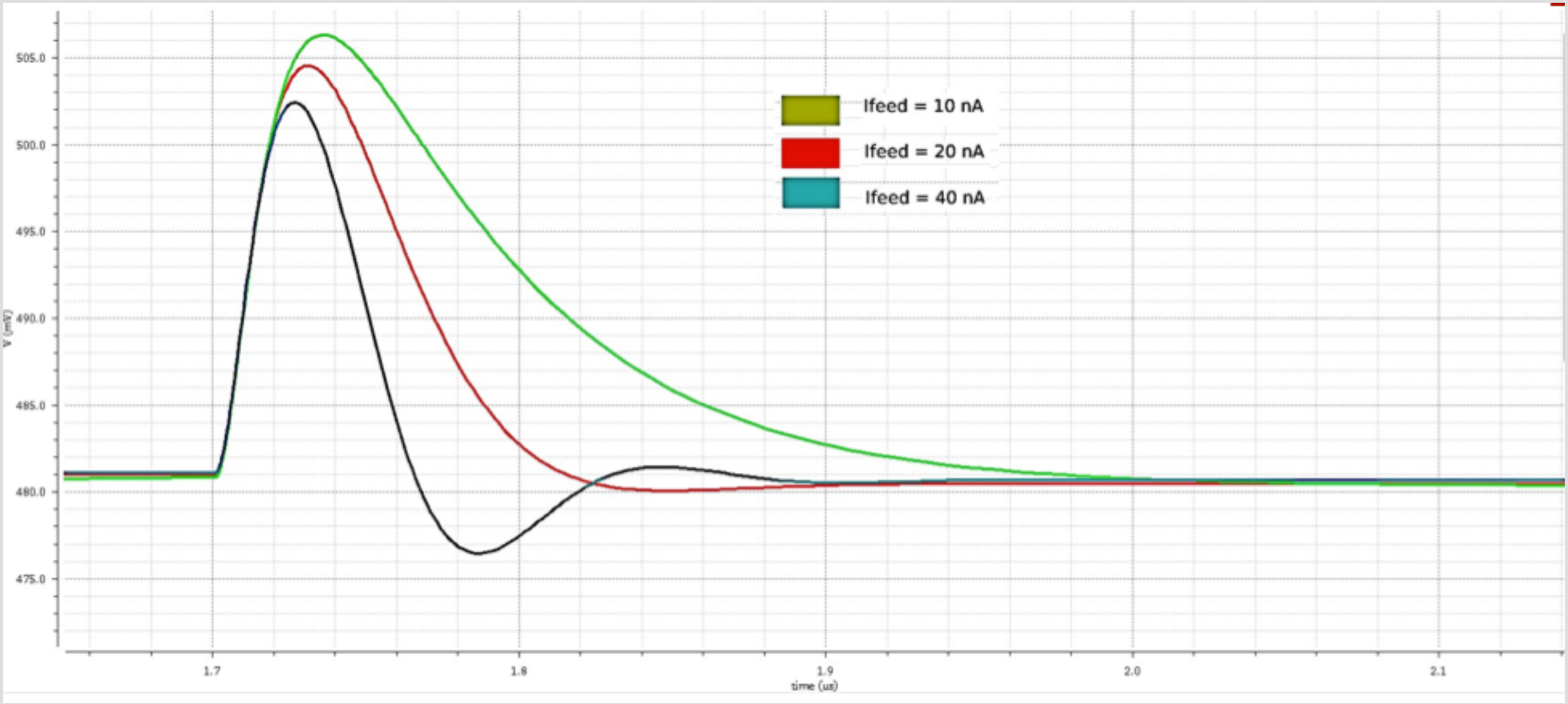
- Dynamic power consumption around 1 μW

- On average the total analog power consumption **is around 5.5 μW per pixel**

- This value corresponds, considering a 50x50 μm^2 pixel, to a power consumption of 0.22 W/cm^2
  - OK -> ~50% of 0.4 W/cm^2

Signal at the preamp output

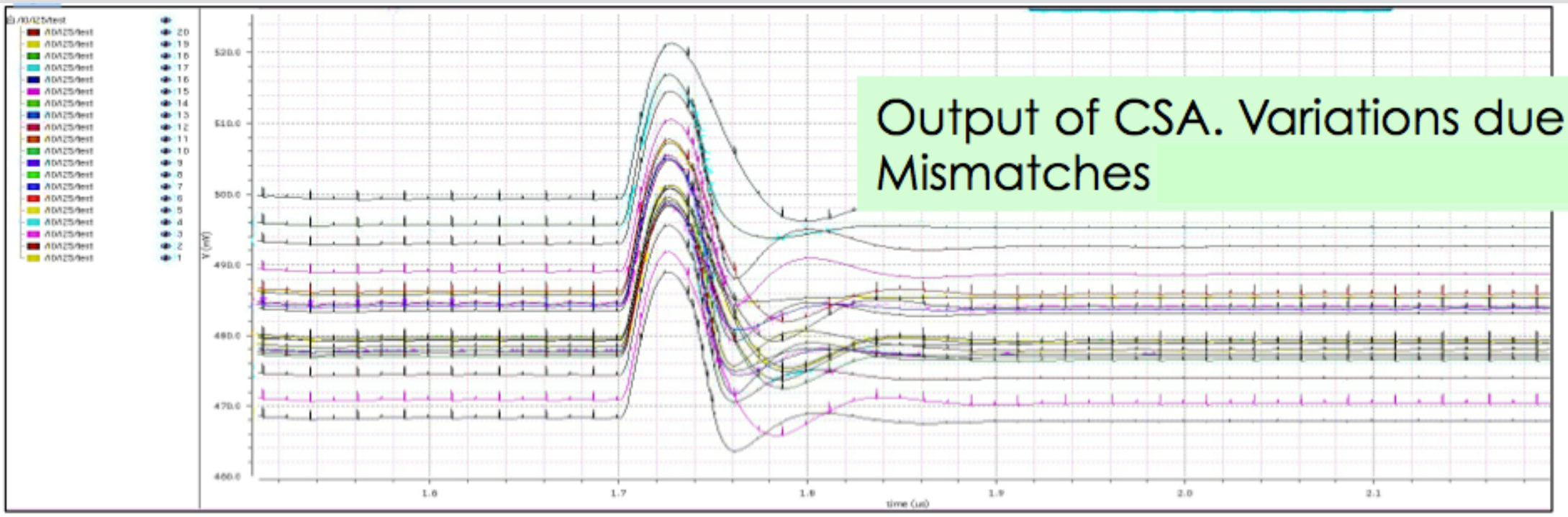
- Input charge -> 1 ke^-

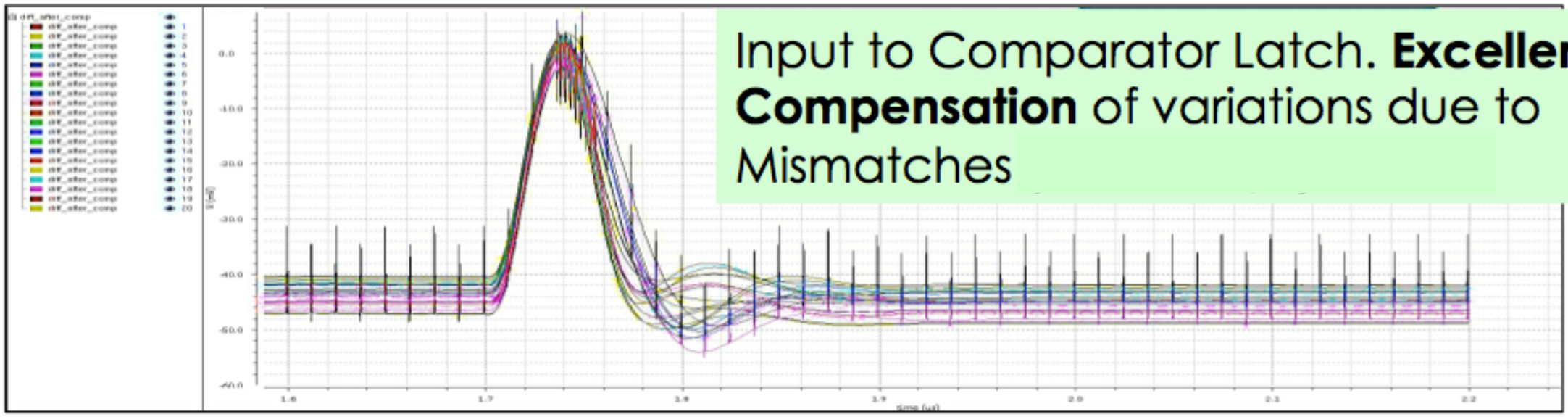


- Ifeed = 40 nA -> Fast ToT mode
- Ifeed 10 nA -> Slow ToT mode (lower ballistic deficit)

Offset compensation

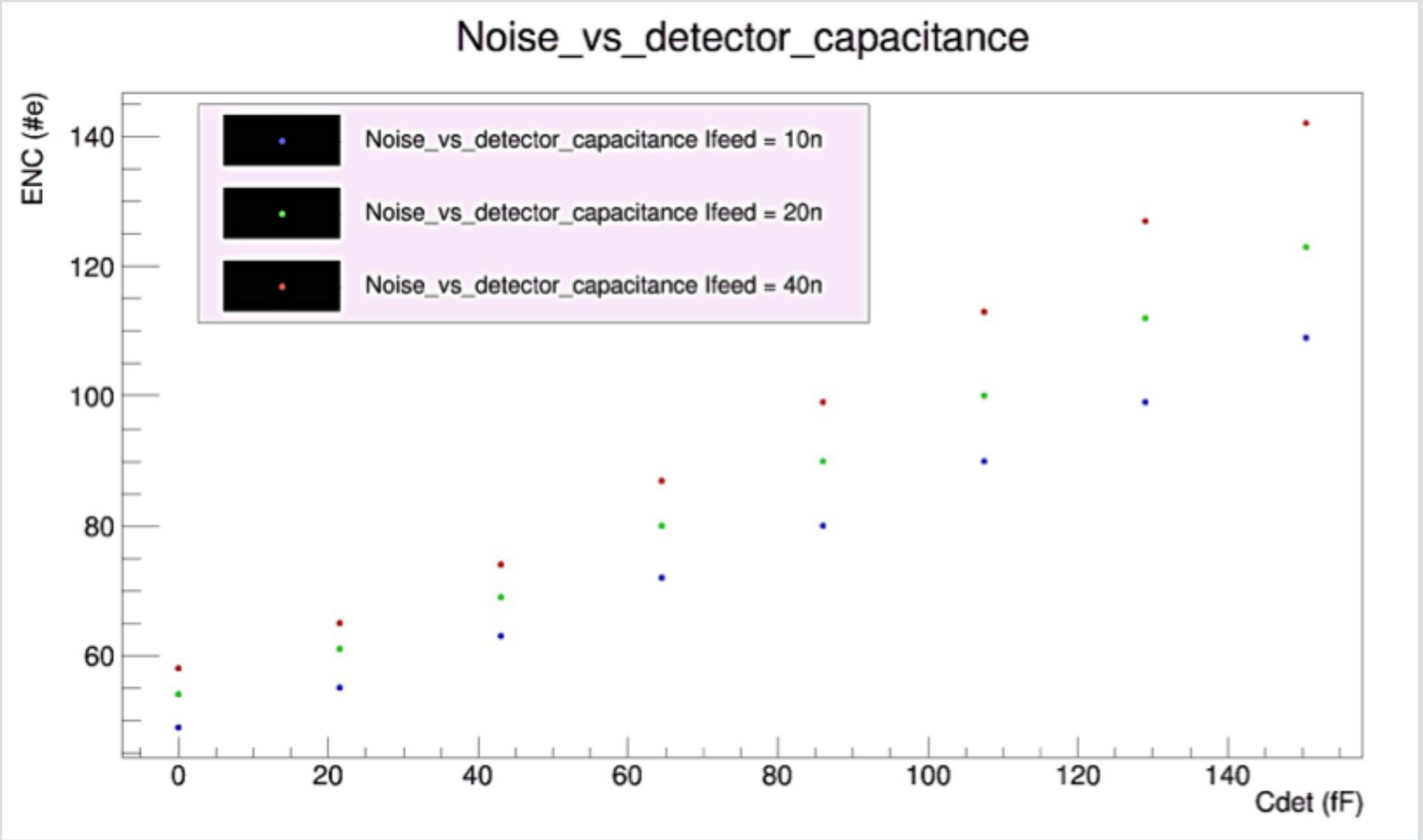
- Results obtained with Monte Carlo simulation





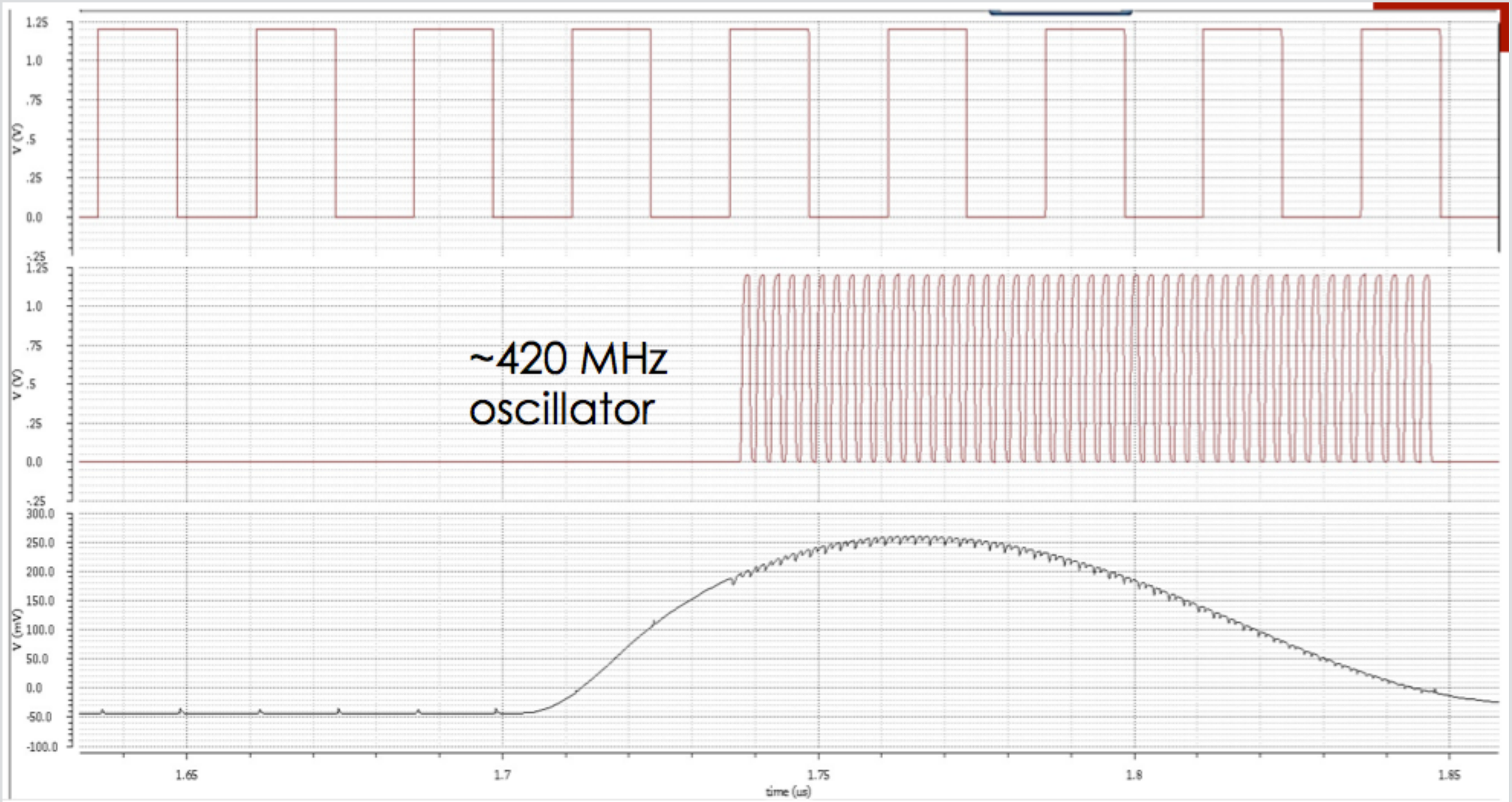
Noise performance

- Simulation results:



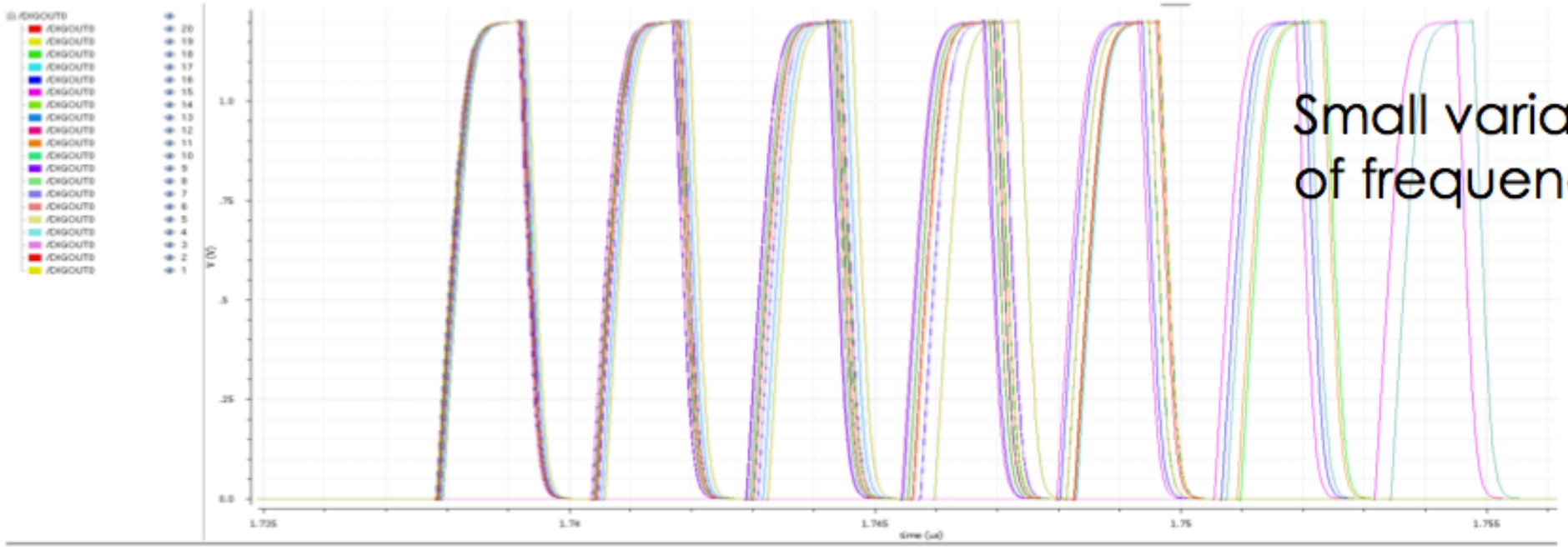
- For Cdet = 100 fF (nominal value):
  - Noise ~ 100e^- for fast ToT configuration
  - Noise ~ 80e^- for slow ToT configuration (30ke^- in 1us)

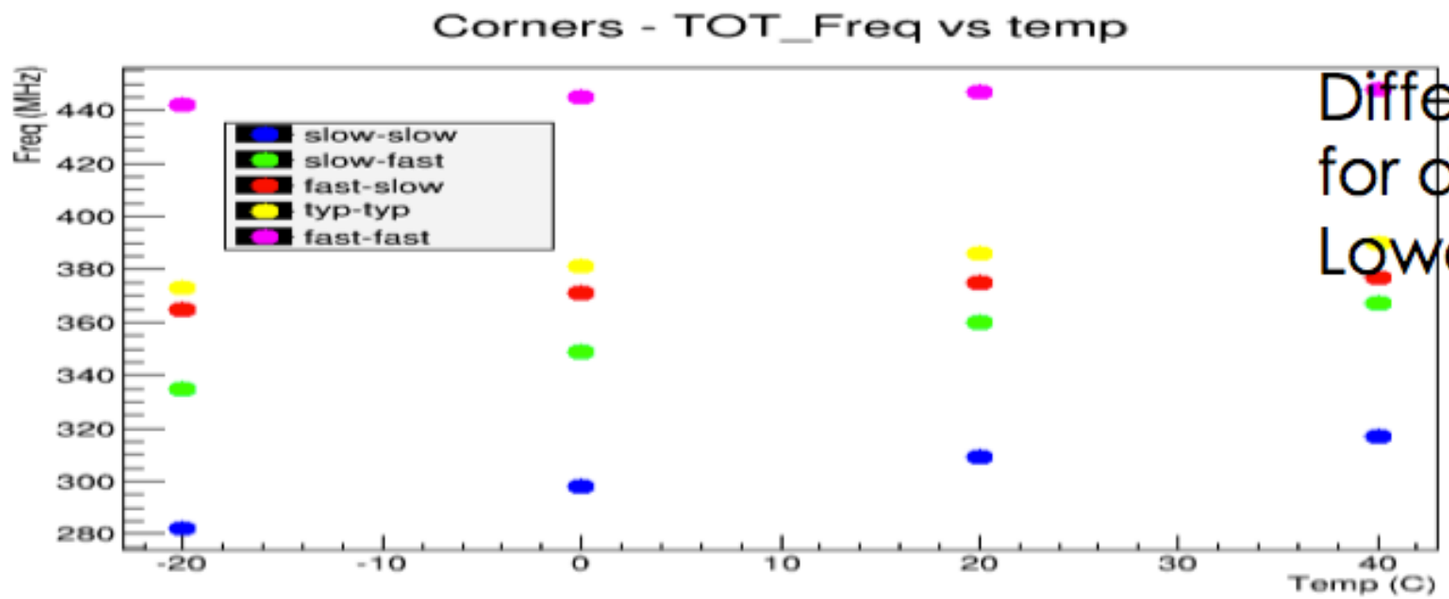
Fast ToT



- The signals in figure are (from top to bottom):
  - 40 MHz clock, fast ToT oscillator, analog signal at latch input

Fast ToT





Different calibration
for different corners
Lower dependence on T

Ongoing activity & further developments

- A first version of this design has been submitted in october 2014
- First tests on the chip started in February 2015
- Radiation tests to be done in the next months
- Activity of simulation and layout still ongoing
  - New layout of the submitted design
  - Design of variants of this design
  - A second submission planned in the next months

Conclusions

- The Phase 2 upgrade of the CMS silicon pixel detectors requires the design of a new readout chip

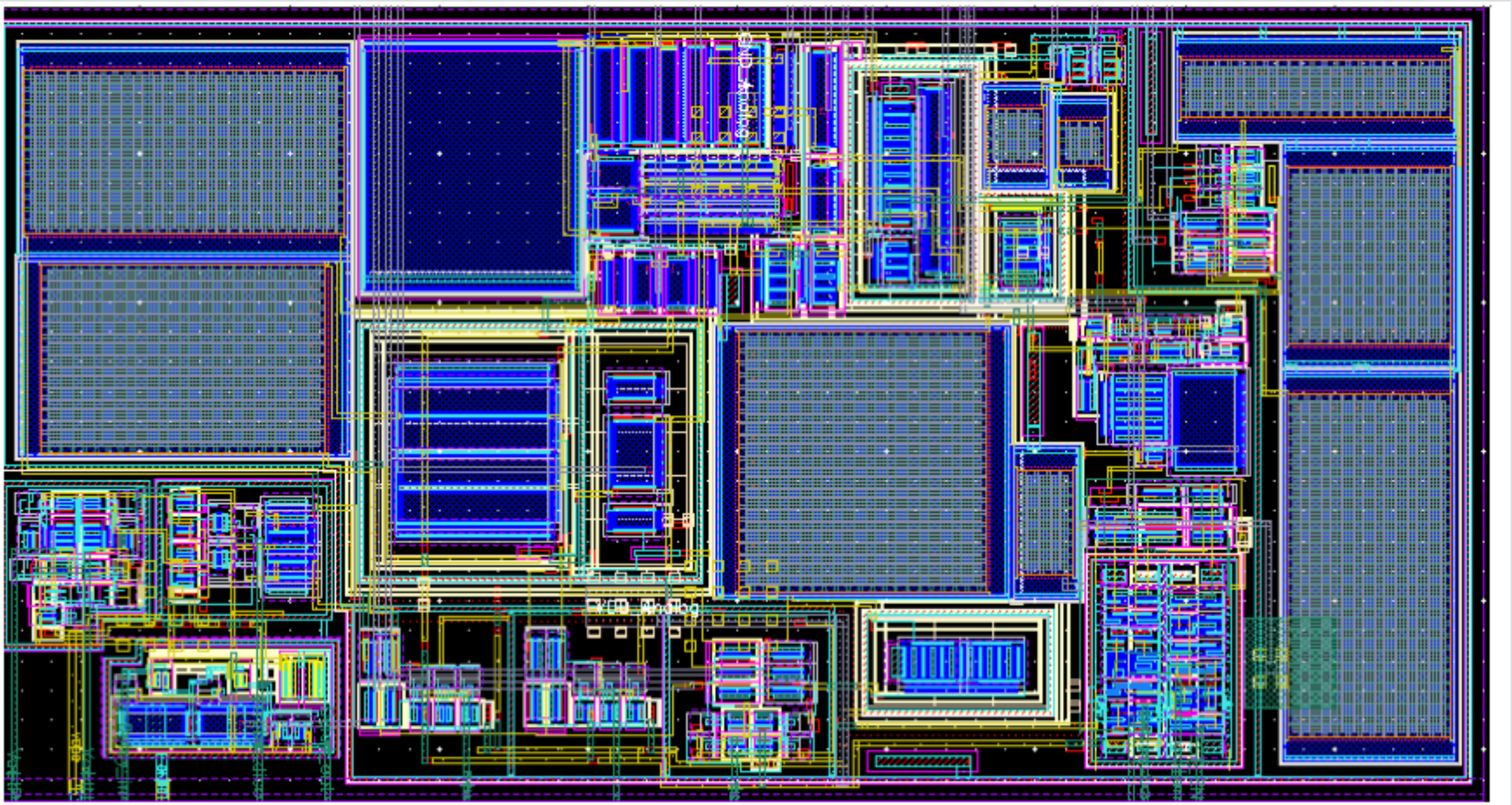
- The simulation results comply with the requirements of the upgrade

- A first version of a new front-end has been submitted in october 2014 and now there are test ongoing on it

- An upgraded version of this design and other options will be submitted in the next months

Backup

Full layout

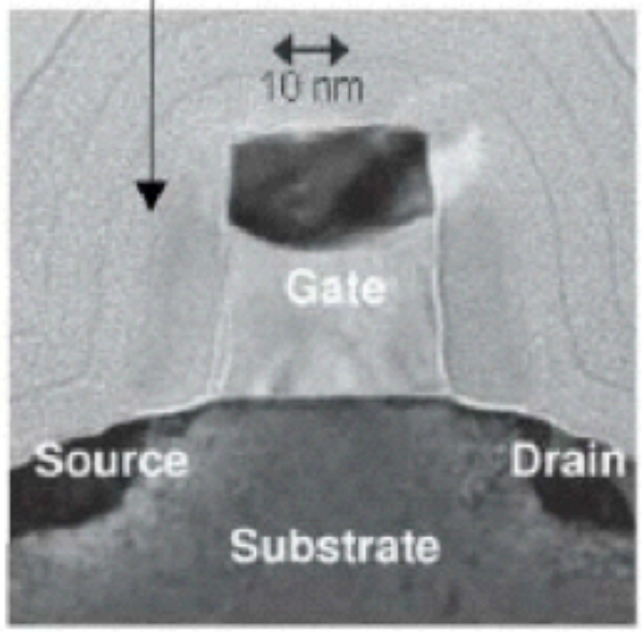


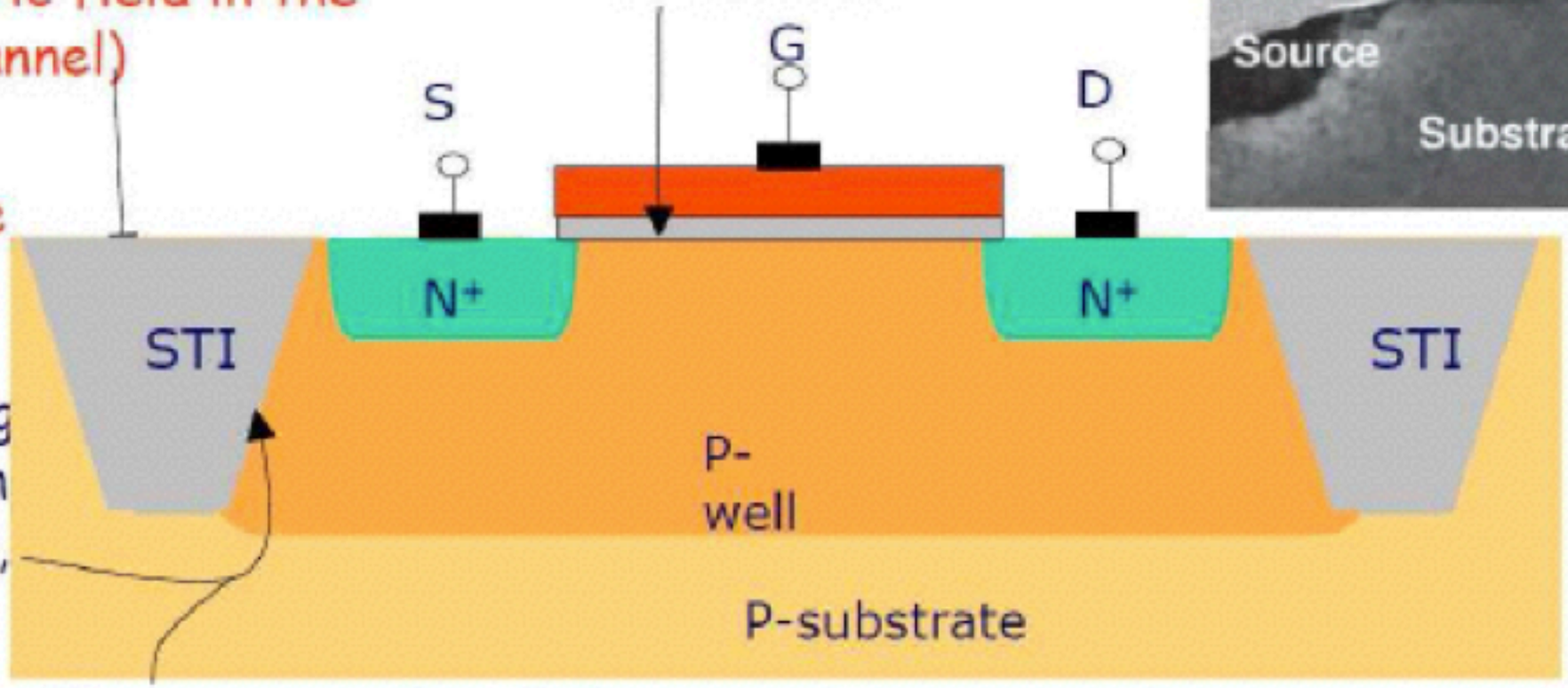
CMOS radiation damage

Thick Shallow Trench Isolation Oxide (~ 300 nm): radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel)

Thin (rad-hard) gate oxide for core devices, becomes thicker (and rad-softer) for I/O transistors

Spacer dielectrics may be radiation-sensitive





Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices

Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)