Ionizing Radiation and Single Event Effects in Electronic Devices and Circuits

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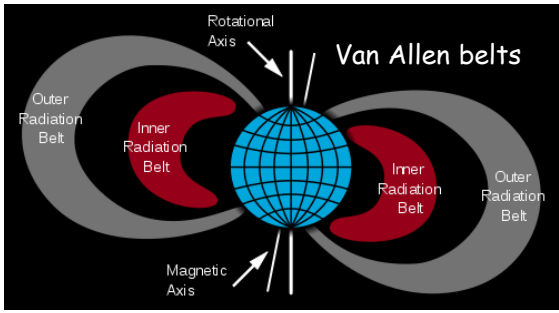
Outline

- Introduction
- Radiation environments
- Ionizing radiation effects in MOSFETs
- Single event effects in devices and circuits
- Radiation-resistant technologies and hardening techniques

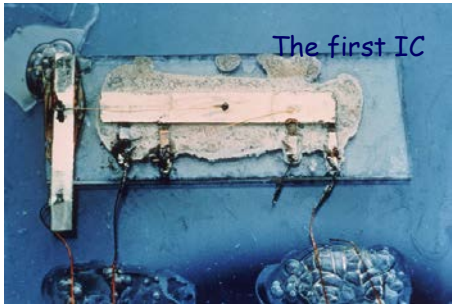
Introduction

- From a historical standpoint, the study of radiation effects in electronic circuits started in the early 60's mainly as a response to two concerns:
  1. the increasing demand for hardened electronics that could survive the impact of a nuclear explosion (nuclear arms race was in full swing at the time)
  2. the discovery of radiation belts by Van Allen and Vernov and the resulting need for protection from them (in the wake of early space exploration)



- The first steps of electronics can be dated back to about the same period: the first satellite (Sputnik 1, 1957) appeared at the same time as the first integrated circuit in germanium (1958); the metal-oxide-semiconductor (MOS) transistor was born in 1960, just the same year as the first interplanetary space probe Pioneer; the Apollo program was a contemporary of the first 256-bit computer memory

- The advance in the microelectronics field, at a pace that has never abated since its debut, has made the use of electronic devices ever more attractive, even for applications in hostile environments



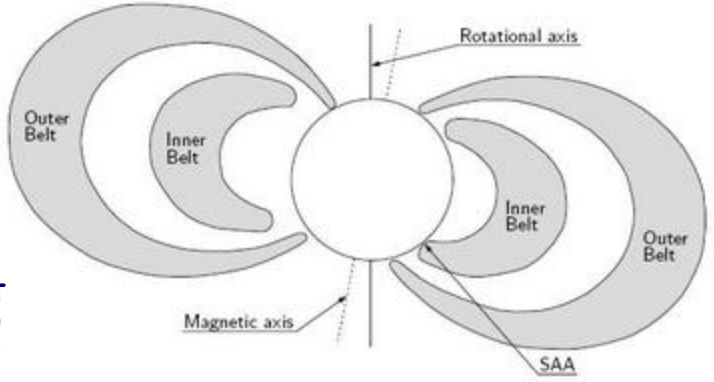
Introduction

- Electronic circuits are used in several fields where a more or less high degree of radiation tolerance is required: space and avionic applications, high energy physics experiments, nuclear and (still experimental) thermonuclear power plants, medical diagnostic imaging and therapy, industrial imaging and material processing
- When operated in these environments, solid-state devices and integrated circuits may be directly struck by photons, electrons, protons, neutrons or heavier particles; alteration of their electrical properties may cause an electronic subsystem to fail
- Depending on the type and characteristics of the impinging radiation, different effects, either irreversible or (partially or totally) reversible, may arise
- Knowledge of the mechanisms underlying the radiation response of electronic devices is of paramount importance for
  1. devising hardness assurance methodologies to guarantee that the tested devices can work reliably in the target environment
  2. developing rad-hard circuits and design techniques to improve the tolerance of electronic circuits to specific effects of radiation in some specific applications

Radiation environments

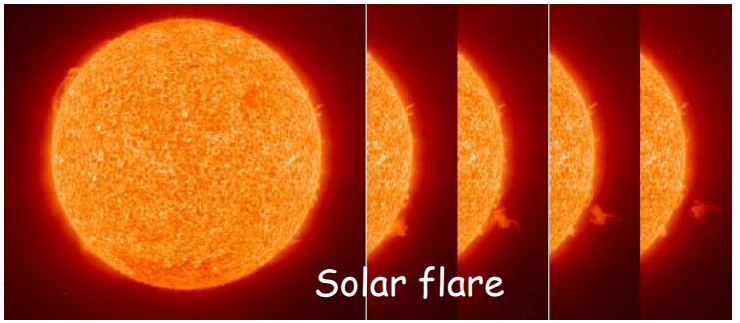
Space environment

- The Earth and its immediate surroundings are protected by the atmosphere, which acts as a semi-permeable shield letting through light and heat while stopping radiation and UV's; because no such protection is available in space, human beings and electronics (onboard Earth orbiting satellites, space shuttles, space probes) must be able to cope with the resulting set of constraints
- **Radiation belts**: the idea that particles trapped stably in the geomagnetic field formed "belts" (geometrically speaking, taking the form of a torus) of intense radiation was first advanced in 1958 by Van Allen in US and Vernov in the Soviet Union
  - Particle trapping in the inner belt (consisting mainly of energetic protons, 800 to 6000 km above the Earth surface) is caused by neutron decay resulting from the interaction of heavy ions or protons with the Earth atmosphere; in the outer belt (mainly including electrons, 2500 to 36000 km above the Earth surface), particles are trapped directly from the solar wind
  - Energy can reach 30 MeV in the case of trapped electrons, about 400 MeV in the case of protons; the flux, both for electrons and protons, is a function of the altitude and energy and can get as high as 10^{10} $cm^{-2}s^{-1}$



Space environment

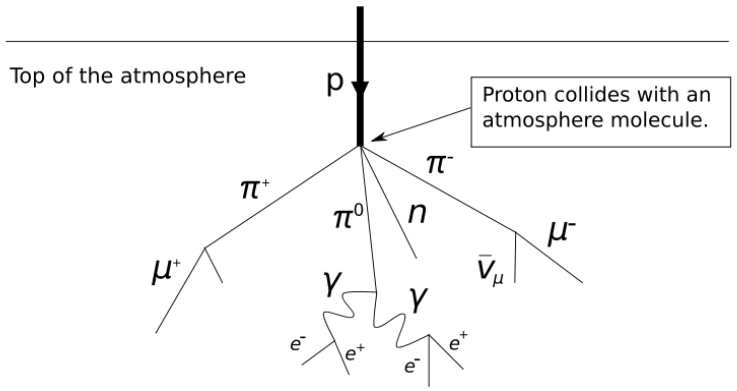
- **Solar activity**: since the launching of artificial satellites, solar activity, featuring an 11 year (sun spot) cycle modulated by an 80 year (Gleissberg) one, has been correlated with particle fluence level
- Two main event categories:
  - **coronal mass ejections**: emit mainly protons with energy up to several hundred MeV
  - **impulsive events (e.g., solar flares)**: involve large emissions of heavy ions, with energies up to hundreds of GeV per nucleon



- **Cosmic rays**: their true nature being still under investigation, cosmic rays consist of protons, He nuclei, electrons and heavy ions, with energies as high as 10^{21} eV
- **Solar wind**: consists of a radial flow of solar gas from the Sun arising from evaporation of the coronal plasma; the solar corona temperature reaches several million of degrees, resulting in its electrons escaping the Sun gravity; the consequent charge imbalance leads to flights of protons and ions into interplanetary space, at a speed of about 400 km/s (corresponding to 1 eV for electrons and a few keV for protons)

Earth environment

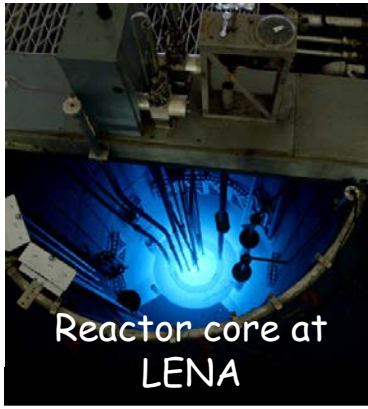
- As early as 1984, it was predicted that **atmospheric neutrons** would cause single event upsets in electronic devices; the first in-flight upset was actually observed in 1992 and, after that, several hundreds have been recorded
- Cosmic rays cover a large spectrum of energies, with a comparatively high flux in the 100 MeV to 10 GeV range and a peak around 500 MeV; cosmic particles collide with the nuclei of atoms making up the Earth atmosphere and initiate the so-called air showers, producing particles such as neutrons, protons, muons, pions, electrons and gamma-rays



- Analysis of particle flux as a function of the distance from the Earth surface shows a predominance of neutrons at the altitude where the aircraft flights take place
- Atmospheric protons play a minor role while, on the other hand, the impact of heavy ions is strongly mitigated by the atmosphere

Commercial nuclear industry and power plants

- In today commercial nuclear industry, there is a growing demand for remote handling and inspection equipment for operation in radiation environments; such environments are associated with nuclear power generation in fission and (still experimental) fusion reactors
- **Fission-based nuclear power** has undergone spectacular development since the oil crisis in the 1970s; the relevant radiation environments are associated with the various stages in the nuclear power cycle:
  - **fuel fabrication plants**: relatively low energy (several tens to several hundreds of keV) photon radiation, with doses below the sensitivity levels of electronic devices
  - **fission reactors**: mainly gamma-rays and neutrons, with dose rates (up to 1 Grad/h) and fluxes (up to 10^{13} 1Mev neutrons $cm^{-2}s^{-1}$) strongly dependent on the distance from the core and on the operation of the reactor
  - **spent fuel reprocessing facilities**: take care of activities like handling of spent fuel, mechanical cutting and washing, chemical treatment, separation of waste and fission products, packaging and storage or waste removal; dose rates may range from those of background radiation to just behind the values recorded in the core of a working reactor (1 Grad/h)
  - **radioactive waste storage**: permanent storage of very high level, solidified waste implies complex shielding, surveillance and teleoperated devices; vitrified waste management involves active elements in concentrated form and dose rates of up to 1 Mrad/y
  - **power plant dismantling and decommissioning**: old nuclear power plants need to be revamped or dismantled; robots and other teleoperated systems involved in such activities may have to withstand doses as high as 1 Mrad


Reactor core at LENA

Commercial nuclear industry and power plants

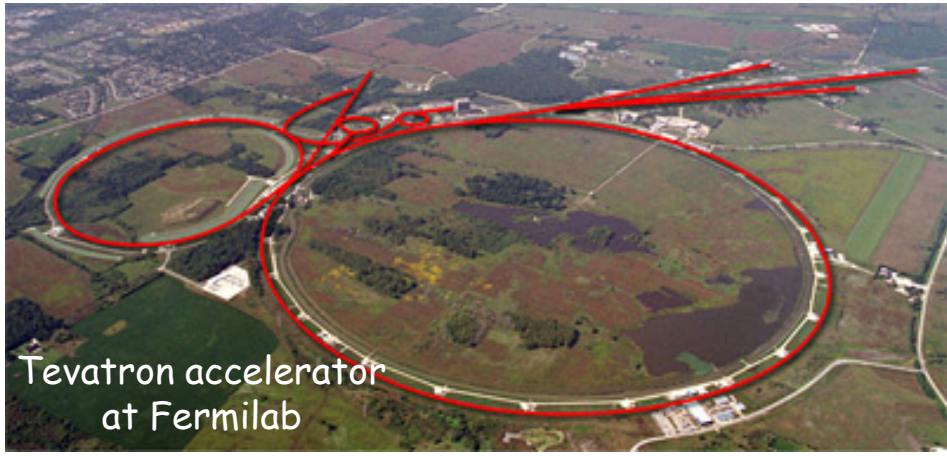
- **Controlled thermonuclear fusion** is still at the experimental stage; two approaches to this technique are currently being explored:
  - **magnetic confinement fusion**: typical radiation levels for a TOKAMAK reactor goes from 100 Mrad/h for gamma-rays and 3×10^{14} 1MeV neutrons $cm^{-2}s^{-1}$ for neutrons inside the reactor to about 1 rad/s and 10^5 1MeV neutrons $cm^{-2}s^{-1}$ on the external surface of the shield; in the design of the remote manipulators for the ITER (international thermonuclear experimental reactor) project, a total dose of 10 Grad was credited
  - **inertial confinement fusion**: in an inertial confinement experiment, a deuterium-tritium target is made to implode by means of extremely powerful laser beams; since the energy is released in a very short time (~100 ps), the radiation environment features extremely high dose rates, $\sim 5 \times 10^{11}$ rad/s for neutrons and 3×10^{10} rad/s for gammas, which must be taken into account in designing measurement devices for plasma diagnostic

Model of the ITER vacuum vessel

High energy physics research environment

- Particle accelerators were developed in the first half of the XX century (thanks to the pioneering work of Van de Graaf, Cockroft, Walton and Lawrence) as a way to overcome the limitations of natural radiation sources and produce artificial particles

- In the most recently fabricated machines (like the Tevatron at Fermilab, USA, and the LHC in Geneva, Europe), particles can be made to smash into each other with energies in the TeV scale

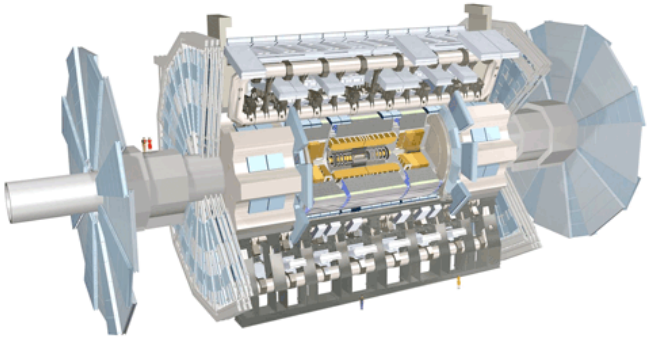

Tevatron accelerator at Fermilab

- Used in fundamental physics research, modern large accelerators can afford such high intensities to produce many types of radiation with potential damage for electronic components and surrounding materials

- Detectors and the relevant readout electronics located close to the interaction points have to survive the hostile environment preserving acceptable sensitivity performance over the entire experiment duration or for a significant part of it before being replaced

High energy physics research environment

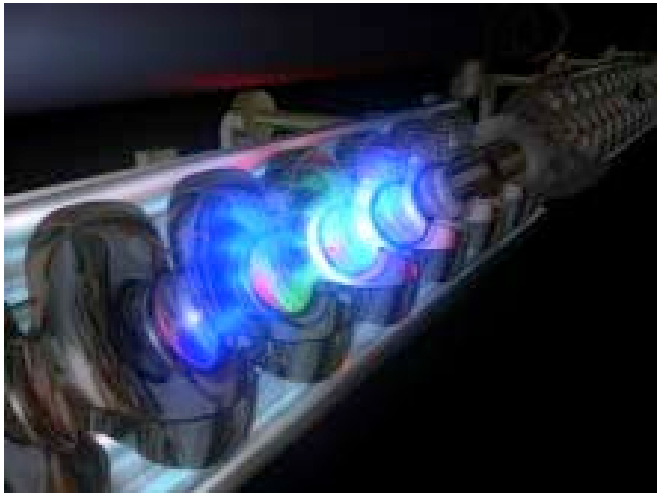
- **Circular electron colliders**: electron colliders (like the LEP, the large electron positron collider, used at CERN until 2000) generate intense synchrotron radiation from which protection is required; the yearly absorbed dose for electronics may be at most of the order of 100 krad
- **Hadron colliders**: accelerate protons and heavy ions and feature negligible synchrotron radiation; beam losses (due to interaction with residual gas and/or machine components) are the main source of radiation, with maximum yearly absorbed dose values of 1 krad for the auxiliary electronics
- **Detector environments**: large detectors for high energy physics experiments consist of huge cylinders placed at selected beam interaction points, at whose centers the desired collisions take place; for instance, the zoo of secondary particles from proton collisions at the LHC gives rise to a severe radiation environment for detectors and the associated electronics; for the phase 2 upgrade of the LHC experiments, ionizing doses of ~1 Grad and fluences in excess of 10^{16} 1MeV eq. n cm^{-2} are anticipated



ATLAS detector at the LHC

Photon science research environment

- Synchrotron radiation sources and X-ray free electron lasers provide the mean for investigating phenomena featuring extremely small space and time scale (properties of materials and organic and inorganic molecules, extremely fast chemical and biological processes)



- Photon energy is not high enough to trigger secondary electron emission through Compton scattering, so bulk damage is generally not an issue
- Especially in FEL lasers, extremely intense X ray flashes are emitted by the source, resulting in very high instantaneous dose rates and very large integrated doses (in the order of several Grad over the lifetime of the equipment) in the focal plane of the detector
- The electronics is shielded by the (several hundreds of micrometer thick) detector, so that the absorbed dose is smaller, but still in the 100 Mrad to 1 Grad range.

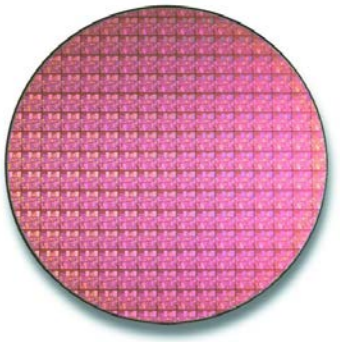
Medical and industrial applications

- Radiation sources are widely used for diagnostic instrumentation, both for medical and industrial applications, and for medical treatment; also many industrial processes involve some kind of material irradiation
- **Protontherapy and hadrontherapy**: hadrontherapy centers are more and more being included in existing hospital facilities; by taking advantage of the so called Bragg peak, hadrontherapy machines can deliver dose more selectively to a given region of the body; proton therapy makes use of beams with high intensities (up to several hundreds of nanoamperes) and energy ranging from 60 to 250 MeV; electronic equipment is exposed to several tens of krad per year of ionizing radiation and to single event upsets (SEU) induced by scattered protons and neutrons (featuring a much larger flux than in the case of atmospheric neutrons)

Proton treatment of a patient at the Loma Linda center

Medical and industrial applications

- Other industrial sectors use irradiation treatment
  - **food irradiation** (e.g., fruit, vegetables)
  - **medical irradiation** (sterilization of instruments and equipment)
  - **waste and water treatment**
  - **radiation-assisted polymerisation**
  - **microelectronic processing** (e.g., ionic implantation)



Silicon wafer

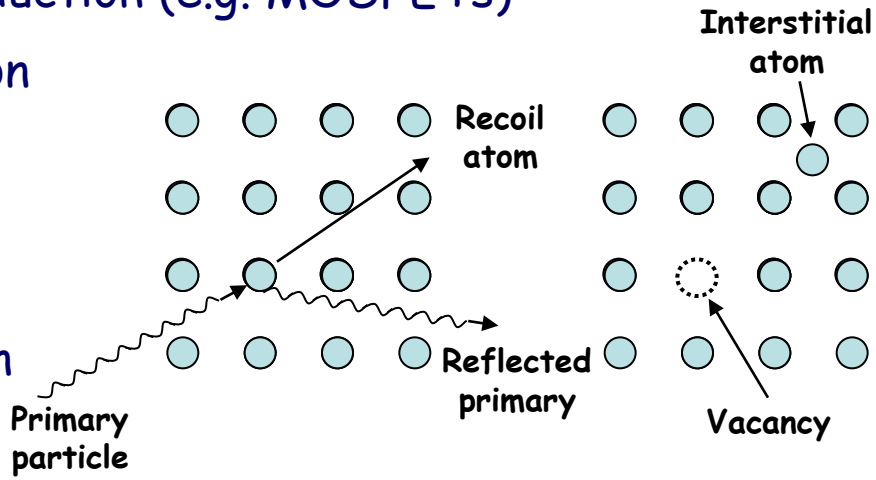
Radiation damage mechanisms and effects

Dosimetry

- Measurement of the amount of energy absorbed by (or of particle or photon flux striking) a sample exposed to a radiation source
- Dosimetry methods have been developed to deal with the two different effects radiation may have on materials
  - deposition of **ionization energy** in silicon dioxide, silicon and a few other materials involved in the fabrication of electronic circuits
  - **non-ionizing energy loss** (**NIEL**), mainly in the form of atomic displacement in crystalline lattices
- Deposited energy is measured in rad (corresponding to the specific energy of 100 erg/g) or Gray (Gy, an SI unit, corresponding to the specific energy of 1 J/kg); based on the definitions, 1 Gy=100 rad (remember that 1 erg=10^{-7} J)
- Particle flux is generally measured in (number of particles) $cm^{-2}s^{-1}$; particle fluence is measured in (number of particles) cm^{-2} and is, by definition, the time integral of the particle flux
- Fluence is often expressed in terms of equivalent number of neutrons with an energy of 1 MeV (1 MeV neutron equivalent) per cm^2

Basic damage mechanisms in semiconductor devices

- Despite the complexity of the interaction processes and their dependence on the properties of the incident particle and of the target material, two are the basic radiation damage mechanisms affecting semiconductor devices
- **Ionization damage**: takes place when energy deposited in a semiconductor or in insulating layers, chiefly SiO_2, frees charge carriers (electron-hole pairs), which diffuse or drift to other locations where they may get trapped, leading to unintended concentrations of charge and parasitic fields; this kind of damage is the primary effect of exposure to X- and γ-rays and charged particles; it affects mainly devices based on surface conduction (e.g. MOSFETs)
- **Displacement damage (DD)**: incident radiation dislodges atoms from their lattice site, the resulting defects altering the electronic properties of the crystal; this is the primary mechanism of device degradation for high energy neutron irradiation, although a certain amount of atomic displacement may be determined by charged particles (including Compton secondary electrons); DD mainly affects devices based on bulk conduction (e.g. BJTs, diodes, JFETs)



Displacement effect in a bidimensional crystal

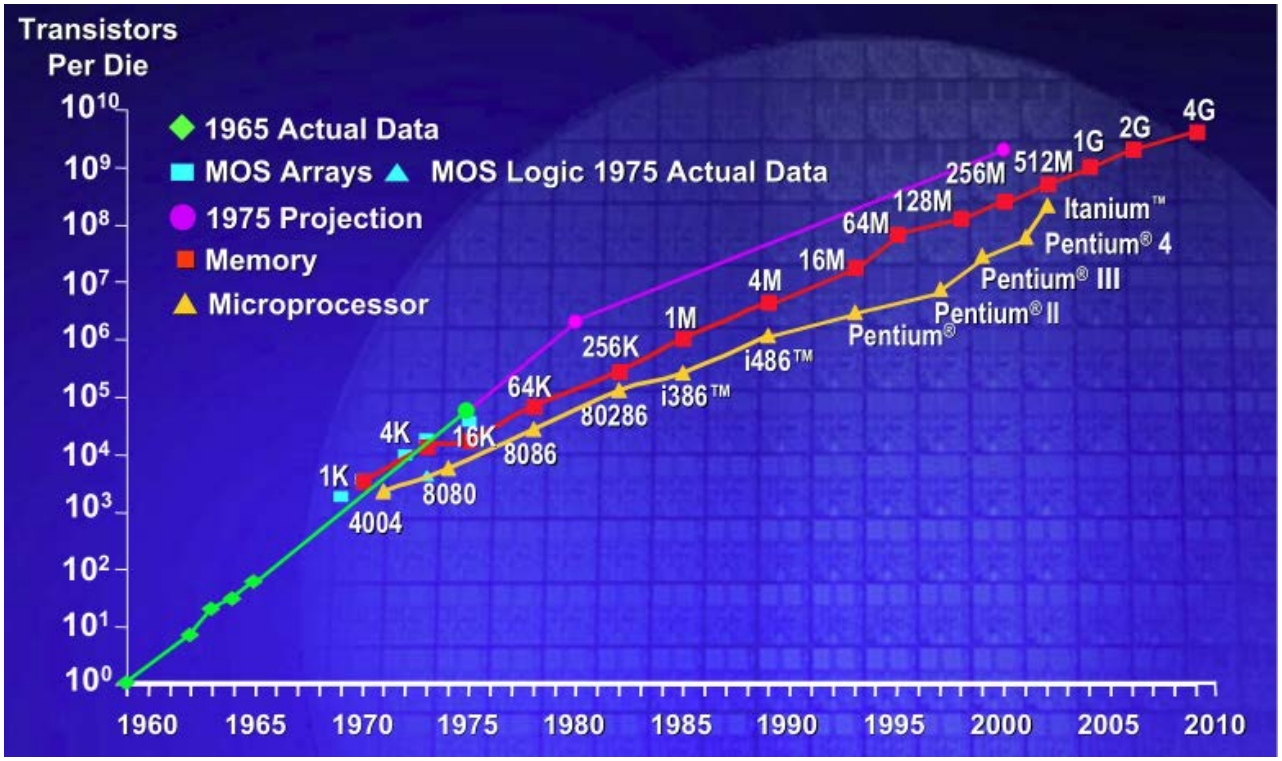
Basic effects of radiation damage

- Effects of radiation in semiconductor devices can be included in one of two broad classes
- **Total dose (TD) effects**: are due to the progressive build-up of trapped charge in insulating layers or at the Si/SiO_2 interface (as a consequence of ionization phenomena) or of defects in the bulk of the devices (originating from accumulation of displacement events)
- **Single event effects (SEE)**: are due to charge deposition induced by a single particle that crosses a sensitive device region; the effects may lead to destructive or non-destructive damage of the device
  - SEEs occur stochastically, while TD is cumulative and may become visible after the device has been exposed to radiation for some time
  - TD is usually related to long term response of devices, whereas SEE is concerned with short time response
  - Only a tiny part of the device is affected by SEE, corresponding to the position of the particle strike, while TD uniformly affects the whole device, because it results from the effect of several particles randomly hitting the device
  - As far as SEE is concerned, the most important figure is the rate of occurrence; TD is characterized by the maximum drift of the main device parameters

Ionizing radiation effects in MOSFETs

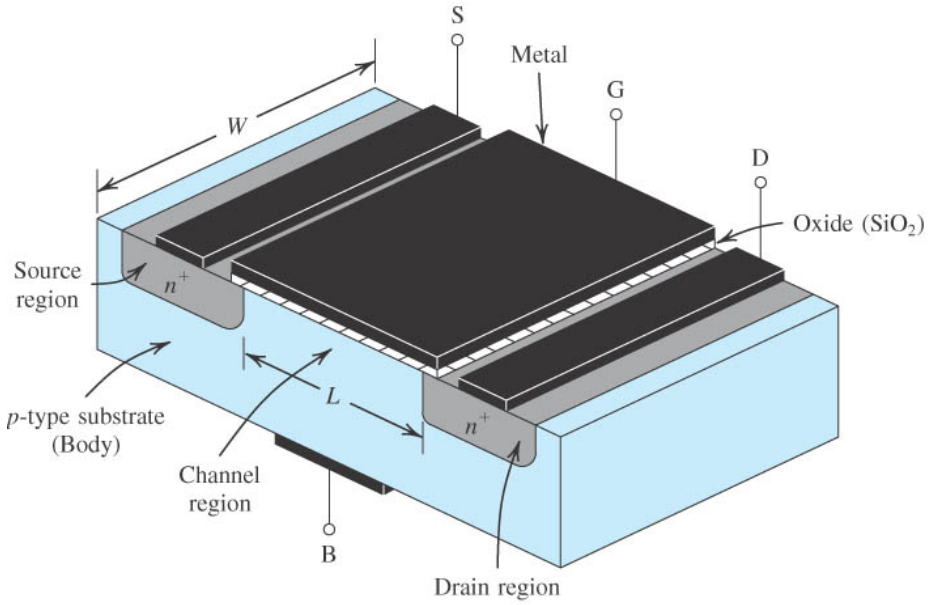
CMOS technologies

- CMOS (complementary MOS) technologies have become dominant in the area of digital integrated circuits because they enable the design of very high density and low power systems
- The development of CMOS processes has been driven by the fast growth of the computer and communication market (ICT, information and communication technology)
- For example, the number of transistors integrated in a microprocessor has increased in the past years at an exponential pace not so far from Moore's prediction, who said that the number of transistors on a chip would double every two years

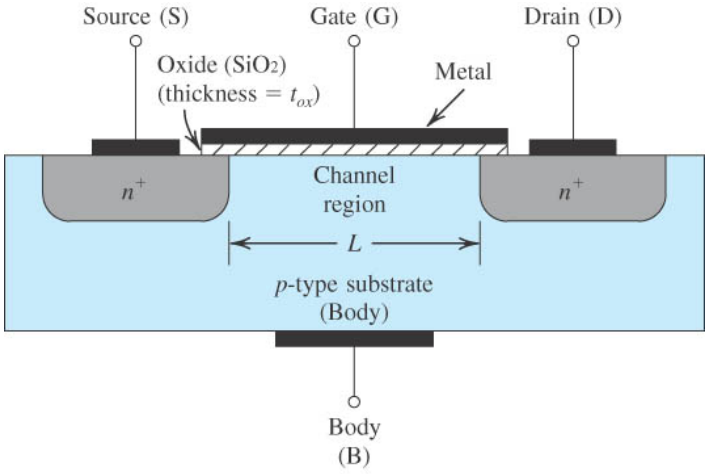


The MOSFET transistor

- MOS transistors come in two flavors, N-type (using electrons as carriers) and P-type (where the current flowing in the device channel is made of holes)
- Fabrication of CMOS transistors requires a sequence of processing steps, performed on a silicon wafer (generally less than 1 mm thick and 30 cm in diameter) including ion implantation, thermal cycling for diffusion and damage annealing, deposition of oxides, metal strips and masking layers and selective attack of the wafer surface (etching)



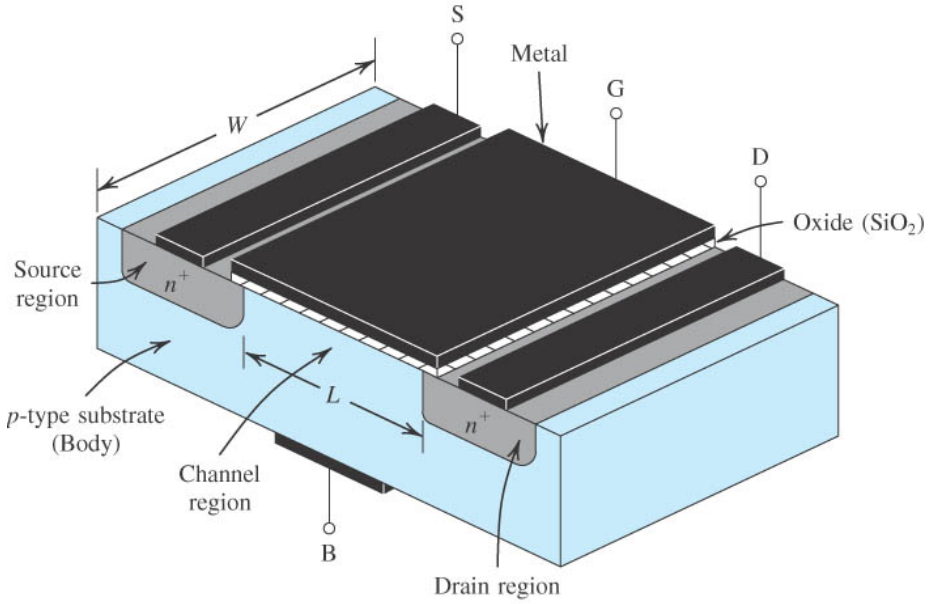
(a)

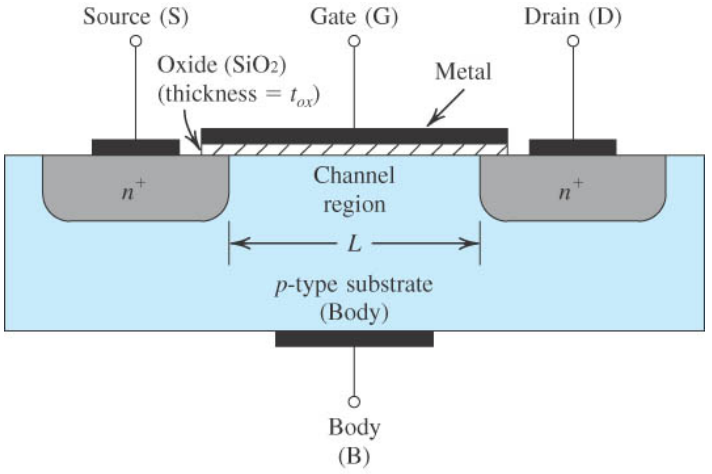


(b)

Operation of the MOSFET transistor

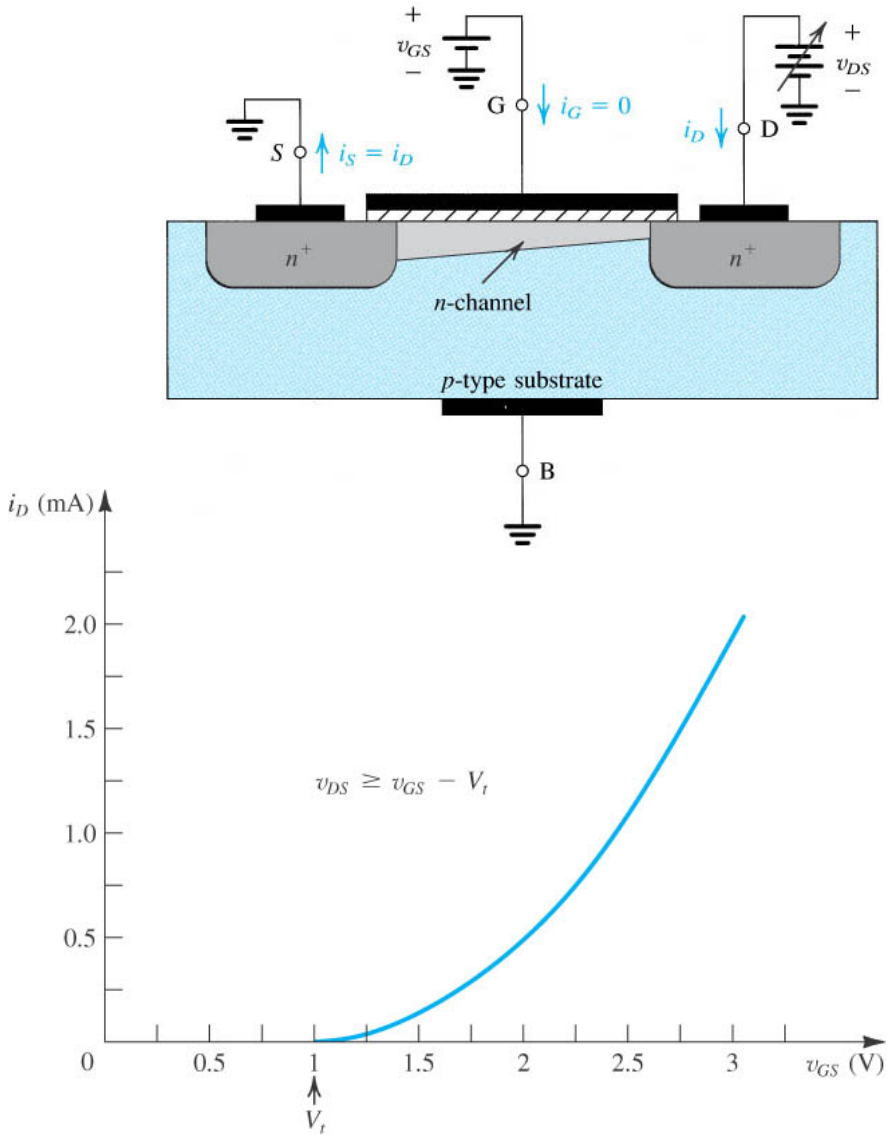
- In an enhancement mode NMOS device
  - heavily doped N-type source and drain regions, at the two ends of the device channel, are fabricated in a P-type substrate (often called the body)
  - a thin layer of silicon dioxide is grown over the substrate material and a conductive gate material (metal or polycrystalline silicon) covers the oxide between source and drain; during device operation, the gate-to-source voltage is used to control the current flowing between source and drain; this control can be used to provide gain in analog circuits and switching characteristics in the case of digital circuits
  - in general, the minimum value of the channel length L which can be achieved in a given technology is used to provide a measure of the lithographic limitations of the fabrication process





Operation of the MOSFET transistor

- In an enhancement mode NMOS device
  - if a positive voltage is applied to the gate terminal, at first free holes will be repelled from the region of the substrate under the gate, leaving behind a depleted region populated with bound negative charges (ionized acceptor atoms)
  - if the gate voltage is further increased, electrons from the n+ source and drain regions are attracted into the channel region; when a sufficient number of electrons has accumulated near the surface of the substrate under the gate, an N region is created, connecting the source and drain regions
  - if a voltage is applied between the drain and source, a current flows through this induced N region (also called inversion layer), carried by mobile electrons
  - the value of V_{GS} at which a sufficient number of mobile electrons accumulates to form a conducting channel is called **threshold voltage** and is usually denoted V_t



Total ionizing dose effects in MOSFET structures

- An MOS device exposed to an ionizing radiation environment typically suffers degradation in one or more of its parameters (threshold voltage, gate voltage to drain current gain, or transconductance, channel leakage, noise); changes may not be constant with time after irradiation and may depend on the dose rate

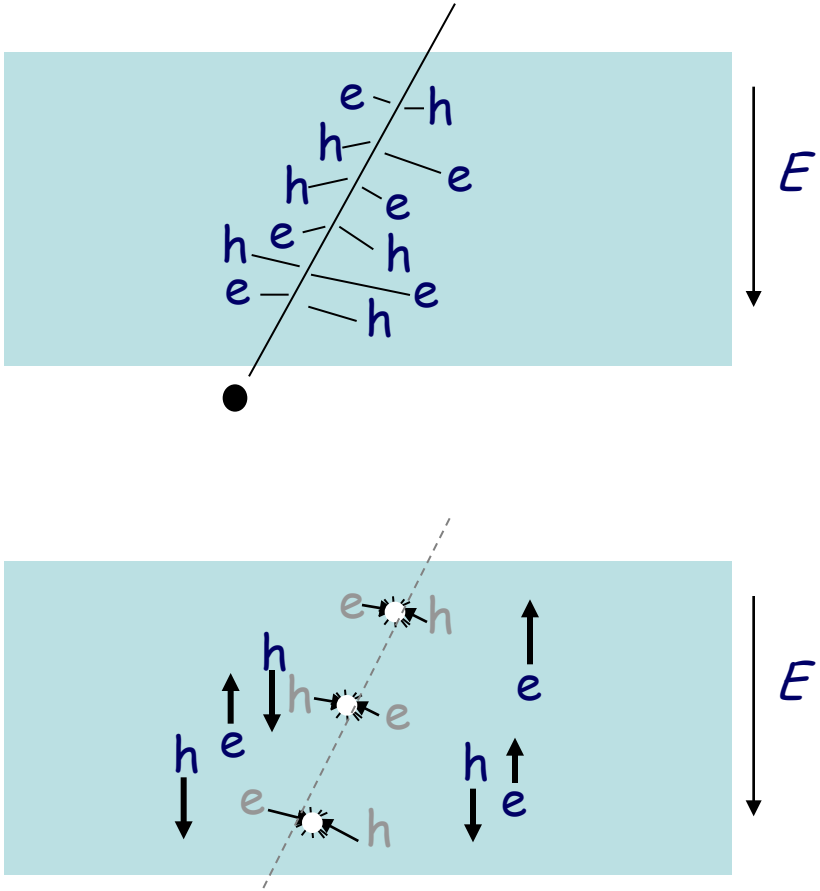
- An integrated CMOS circuit may slow down, show higher leakage (parasitic) currents, or even cease functioning properly (catastrophic failure)

- Damage responsible for these total dose effects occurs in the insulating layers (SiO_2) of the device structures and at the interface between the silicon substrate of the device and the oxide, and consists of three components:

  1. buildup of (positive) charge trapped in the oxide (the gate oxide and/or the field oxide, used to isolate devices from each other)
  2. increase in the number of interface traps
  3. increase in the number of traps in the oxide bulk

Carrier generation and transport in the oxide

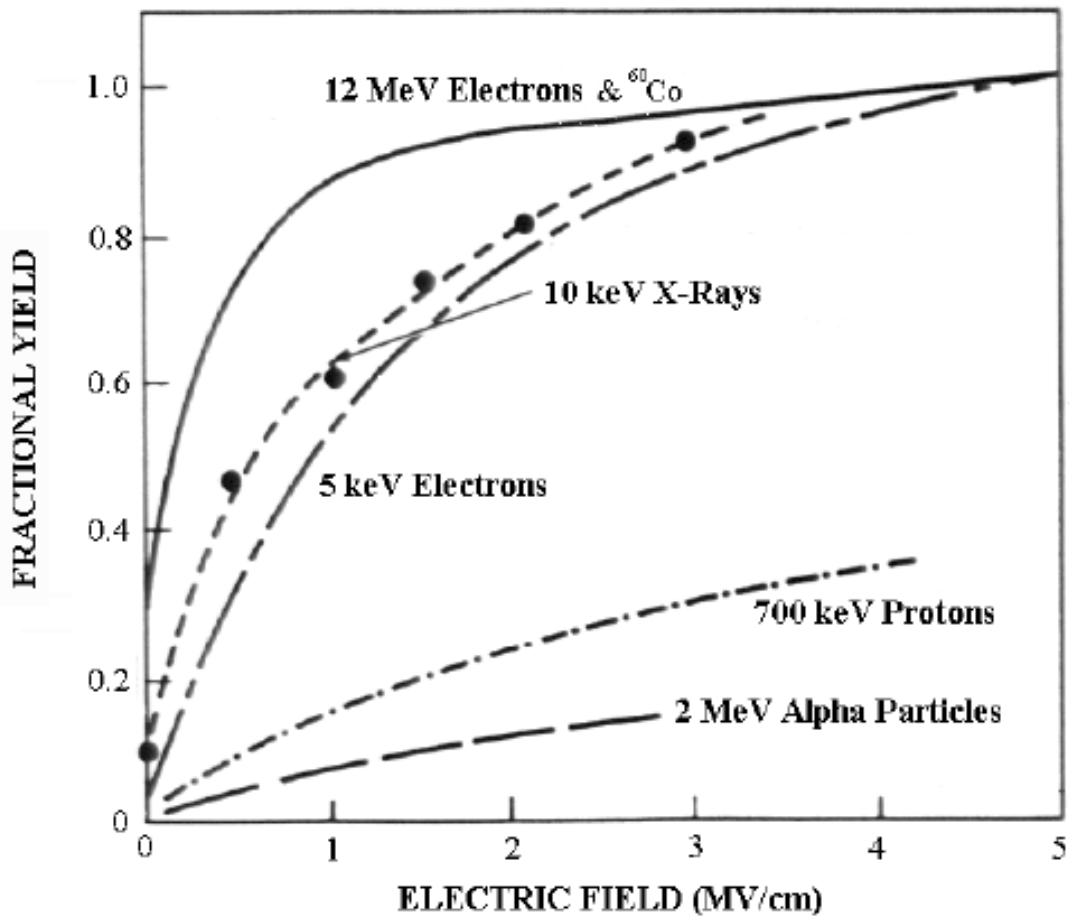
- When a particle passes through the MOS structure, it ionizes the lattice atoms, leaving behind free electron-hole pairs along its track
- In the gate oxide, part of the pairs recombines; the remaining electrons and holes are separated by the applied electric field; in the case of an NMOS device, assuming that a positive voltage is applied to the gate terminal,
  - **electrons** move towards the gate; electrons are very mobile in SiO_2 (μ_n=20 $cm^2V^{-1}s^{-1}$) and quickly get out of it through the gate contact
  - **holes** move towards the Si/SiO_2 interface; holes have a very low effective mobility (between 10^{-4} and 10^{-11} $cm^2V^{-1}s^{-1}$) and transfer via a complicated, stochastic trap-hopping mechanism



- Since the number of e-h pairs is proportional to the deposited energy, the total damage is also roughly proportional to the total absorbed dose

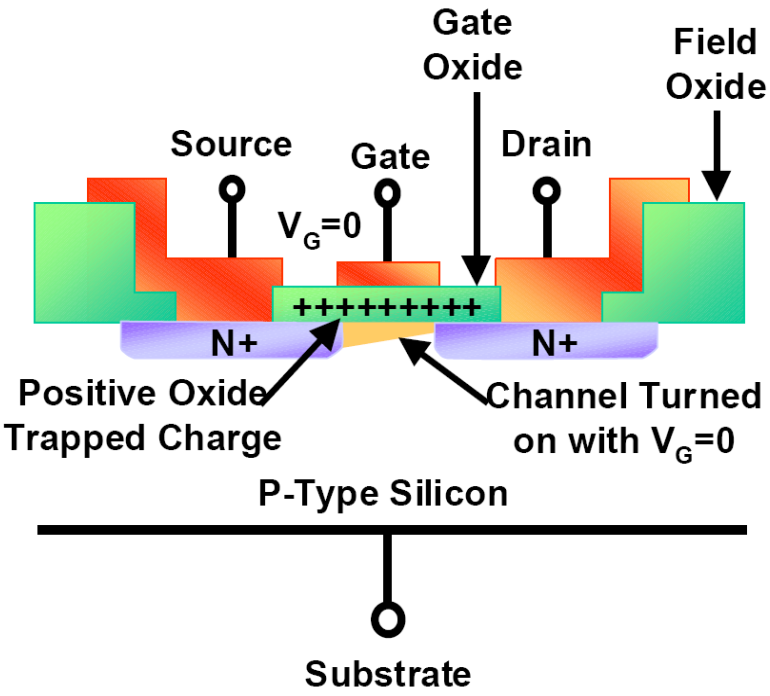
Fractional yield

- The amount of recombination depends on the fractional charge yield, which is a function of the applied electric field and on the type and energy of the incident radiation; the results shown in the figure are well established for thermally grown silicon dioxide, while much less is known for other dielectrics, like SiN, which are largely used in the microelectronic industry



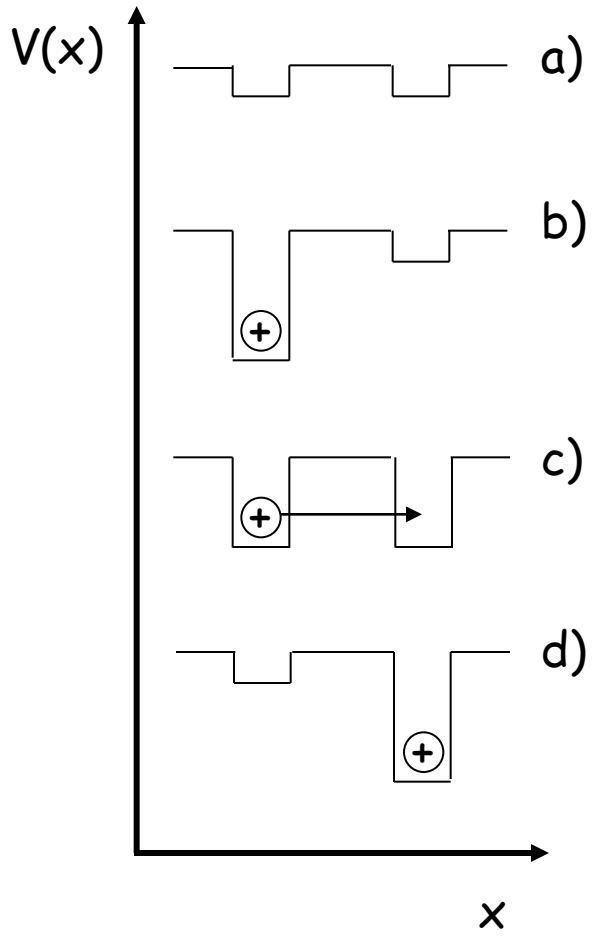
Carrier transport in the oxide

- Some of the holes may be trapped within the oxide, leading to a net positive charge (the ratio between trapped holes and trapped electrons is somewhere between 10^3 and 10^6); others may move to the Si/SiO_2 interface, where they can create an interface trap by capturing electrons
- Along with the electron-hole generation and/or hole transport processes, chemical bonds in the oxide structure may be broken; in particular, bonds associated with hydrogen and hydroxyl groups may release hydrogen ions (protons), which may migrate to the Si/SiO_2 interface and undergo a reaction resulting in the creation of interface traps; also defects created in the oxide bulk can migrate and form interface traps
- Generally, interface traps can trap both holes and electrons by capturing them from the device channel; their state depends on the bias conditions and type of the device



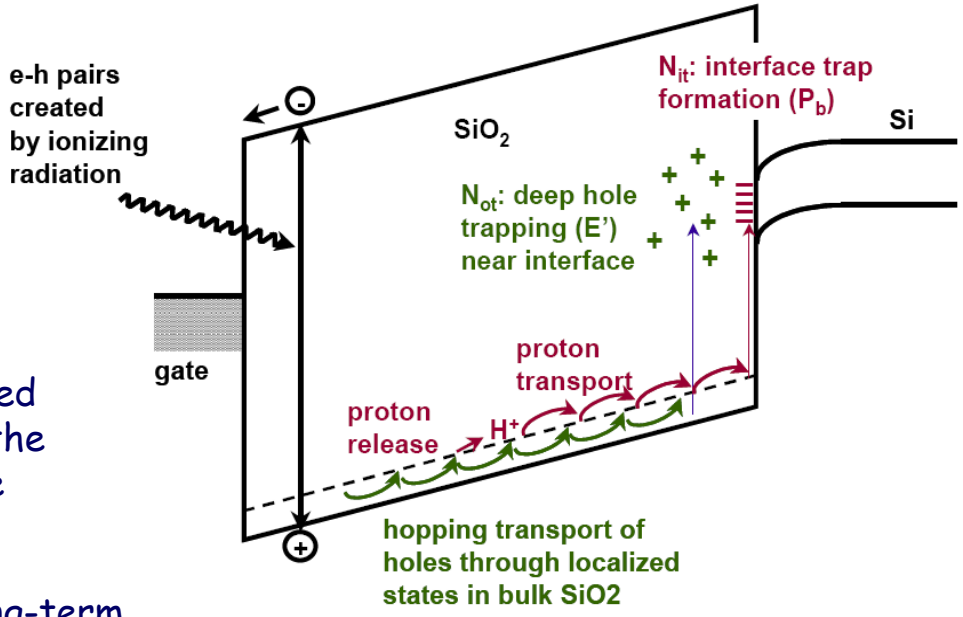
Hole transport mechanism (polaron hopping)

- Let us start with an initially empty localized trap a); when a hole, while moving through the oxide, gets stuck in it, the total energy of the system is lowered by a distortion of the lattice around the trap site b); the hole digs a potential well for itself, i.e. is self-trapped
- The transition of the trap between two nearby sites occurs via an intermediate thermally activated state c), for which thermal fluctuations of the system momentarily bring the electronic energy levels very close to each other; the hole tunnels from the first to the second site
- In the final state of the process, the hole resides in the second site d), the transition probability depending on the tunneling transition probability and on the probability that the intermediate state in c) is created



Hole trapping and interface state formation

- To summarize, in the gate oxide of an MOS structure
  - electron-hole pairs are created along the track of the impinging particle
  - the electric field quickly sweeps electrons out of the oxide, while holes migrate to the Si/SiO_2 interface with a peculiar hopping mechanism
  - under the effect of the field, also protons (released as a consequence of the generation process or of the hole motion in the lattice) may reach the interface and create traps there
  - holes get trapped in the oxide, some of them in long-term trapping sites close to the interface (a region relatively rich of lattice imperfections), building up a net positive charge



- While the net charge trapped in the oxide (oxide trapped charge) is always positive, charge balance at the interface (interface trapped charge) depends on the type of MOSFET, whether it is an N- or a PMOS; when the channel is formed (➔ gate-to-source voltage > threshold voltage) interface traps are mostly positively charged in PMOS, negatively in NMOS

Oxide trapped charge

- Oxide trapped charge is responsible for a negative variation ΔV_{OT} in the threshold voltage

$$\Delta V_{OT} = -\frac{q}{C_{OX}}\Delta N_{OT} = -\frac{q}{\varepsilon_{OX}} t_{OX}\Delta N_{OT}$$

- q=elementary charge (1.6×10^{-19} C)
- $C_{OX}=\varepsilon_{OX}/t_{OX}$ is the specific capacitance of the MOS capacitor (to be measured in F/m^2)
- t_{OX}=gate oxide thickness
- ε_{OX}=dielectric constant
- ΔN_{OT}=density of oxide trapped holes per area unit (to be measured in m^{-2})

- According to a very simple model, ΔV_{OT} is proportional to t^2_{OX}, ΔN_{OT} being proportional to t_{OX}; actually, the trapped hole concentration generally peaks close to the Si/SiO_2 interface

- If n_{ht} is the local density of trapped holes and x the coordinate along the direction perpendicular to the Si/SiO_2 interface (n_{ht} is assumed to be constant in any plane parallel to the interface)

$$\Delta N_{OT} = \int_0^{t_{OX}} n_{ht}(x)dx$$

Interface trapped charge

- The net charge residing in interface traps can either be positive, neutral or negative; based on their allowable charge states, interface traps are classified as either donors or acceptors
  - a donor trap level is in a neutral charge state when it is below the Fermi level, and becomes positive by donating an electron when it moves above the Fermi level
  - an acceptor trap level is in neutral charge state when it is above the Fermi level, and becomes negative by accepting an electron when it moves below Fermi level
- When a voltage is applied to the gate of an MOS device, the interface trap levels move up or down relative to the Fermi level; experimental data show that interface traps in NMOS are predominantly acceptor-like (can be neutral or negatively charged), predominantly donor-like (neutral or positively charged) in PMOS
- Depending on the device bias condition, interface trap charge is responsible for a change ΔV_{IT} in the threshold voltage, given by

$$\Delta V_{IT} = -\frac{\Delta Q_{IT}}{C_{OX}}$$

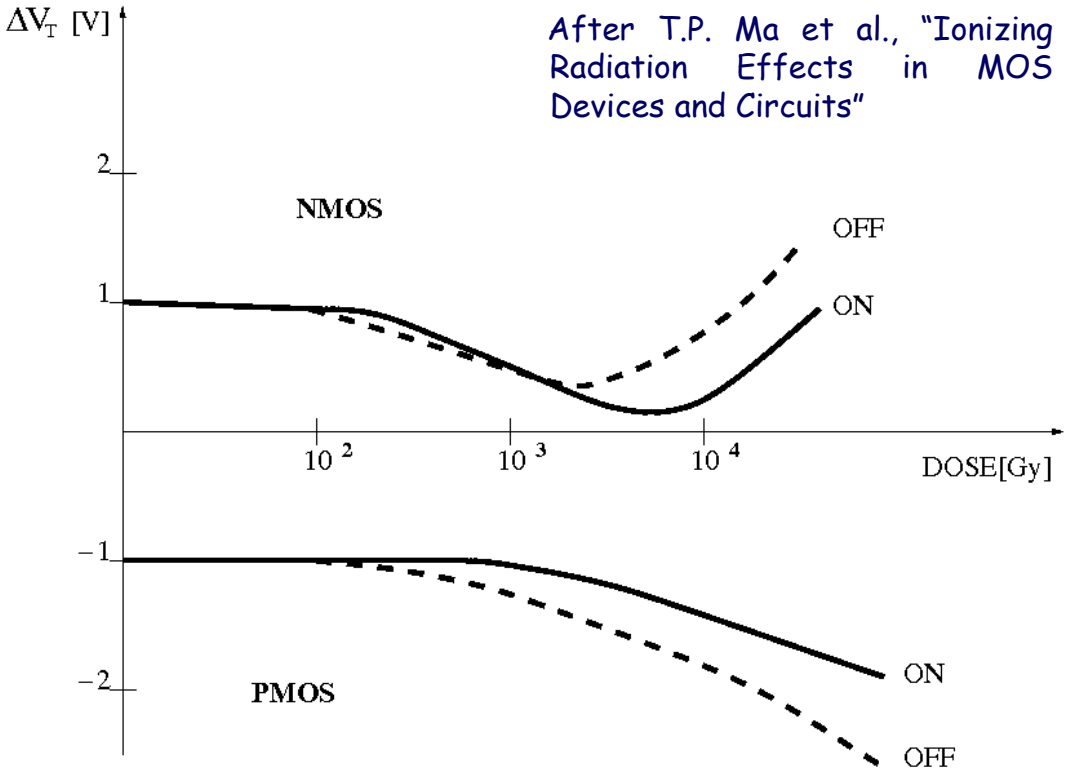
where ΔQ_{IT} is the interface trapped charge

Threshold shift

- The overall effect of oxide trapped charge and interface trapped charge can be written as

$$\Delta V_t = \Delta V_{OT} + \Delta V_{IT} = -\frac{1}{C_{OX}}\left(\Delta Q_{OT} + \Delta Q_{IT}\right)$$

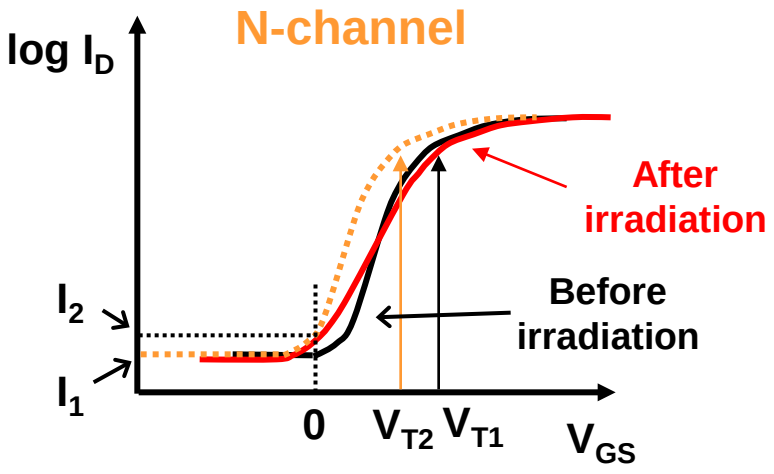
- In NMOS transistors
  - at low doses, V_t decreases since its behavior is dominated by positive charge trapping in the oxide
  - at high doses, V_t increases since its behavior is dominated by negative charge trapping at the Si/SiO_2 interface
- In PMOS transistors
  - both at low and high doses, V_t decreases as both oxide and interface traps can only be positively charged (or neutral, if not charged)

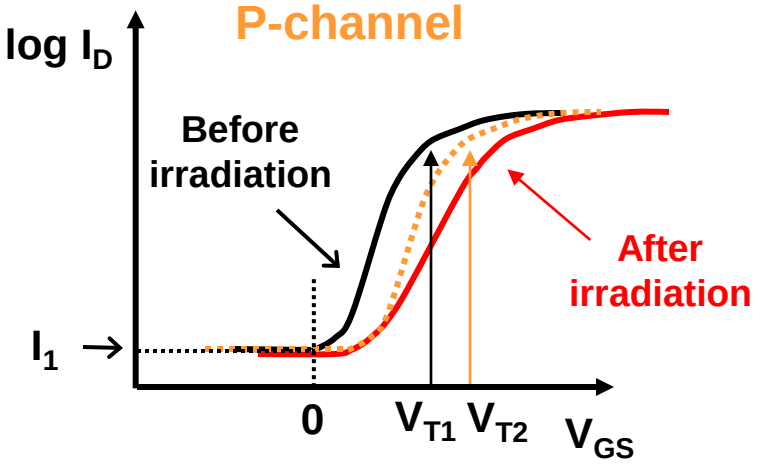


After T.P. Ma et al., "Ionizing Radiation Effects in MOS Devices and Circuits"

Subthreshold current change

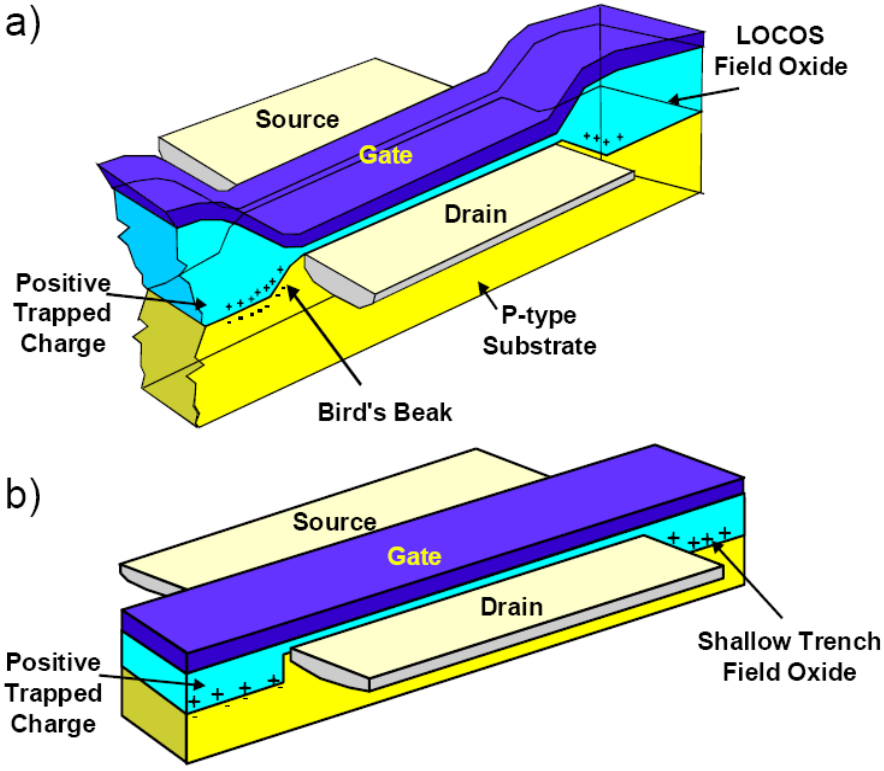
- Oxide charge trapping and interface trap buildup induced by ionizing radiation also are responsible for a remarkable change in the I_D-V_{GS} curves in MOSFETs
- Two different effects can be distinguished:
  - a shift of the curve along the voltage axes (towards negative values for NMOS, towards positive values for PMOS transistors) due to threshold voltage shift
  - a decrease in the subthreshold curve slope (curve stretch-out) for both device types, which was experimentally found to be correlated to interface trap buildup
- As a consequence of these effects, a net increase in the NMOS drain current is observed at V_{GS}=0, while no increase (if not a decrease) can be detected in the PMOS





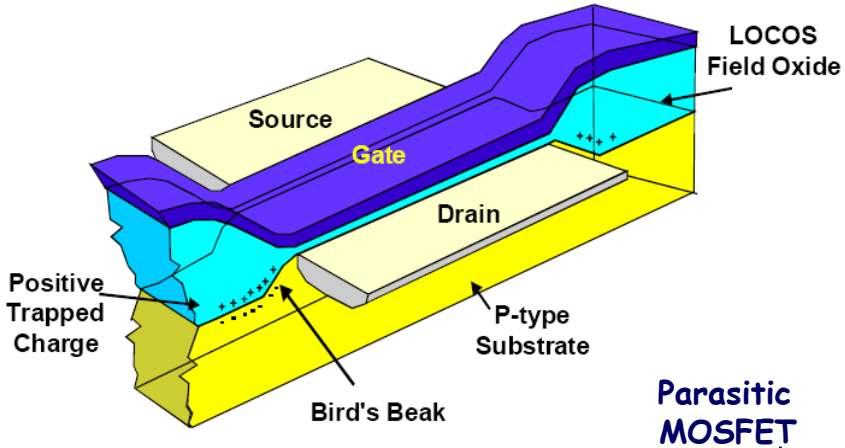
Leakage currents due to field oxides

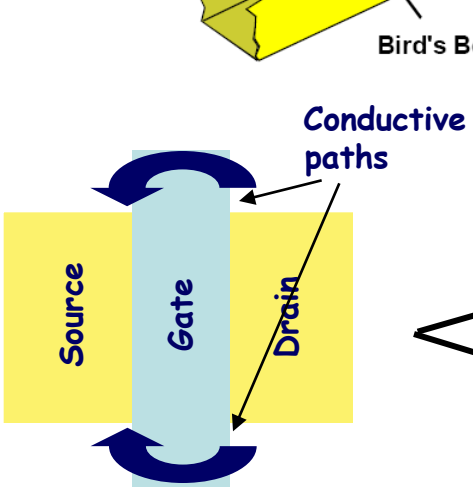
- The trend to device scaling in the modern microelectronic industry has brought along a progressive reduction of the gate oxide (2 nm in 130 nm CMOS technology) and an ever higher degree of tolerance to ionizing radiation
- On the other hand, the field oxide used to electrically isolate devices from each other features a thickness ranging between 100 and 1000 nm
- Two different kinds of isolating oxides are used in CMOS processes
  - a) LOCOS, local oxidation of silicon (actually progressively abandoned in modern CMOS technologies)
  - b) STI, shallow trench isolation
- In an NMOS device, positive charge trapping in the field oxide due to ionizing radiation can invert the underlying P doped region and form an N-type conducting channel between the source and drain terminals, therefore increasing the drain leakage current

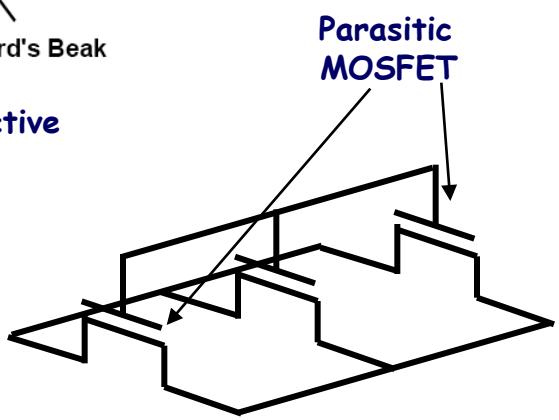


Leakage currents due to field oxides

- Positive charge trapped in the field oxide may create a parasitic channel between the source and drain terminals under the bird's beak region
- The oxide thickness in the bird's beak region is larger than in the gate oxide and the accumulated positive charge can be such that the underlying P substrate is inverted and an N-type channel is created
- The radiation induced channel can be modeled with a parasitic transistor in parallel with the main device and featuring a different width W but the same length L
- This effect can be observed only in NMOS transistors, since in PMOS devices the charge in the channel is carried by holes and the N-type substrate cannot be inverted by the positive trapped charge

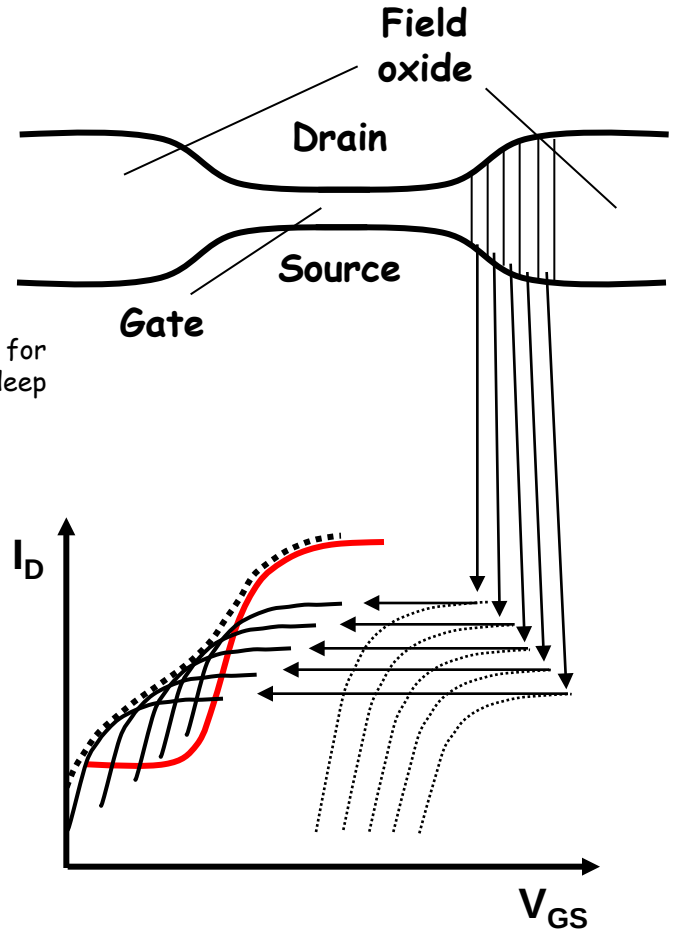




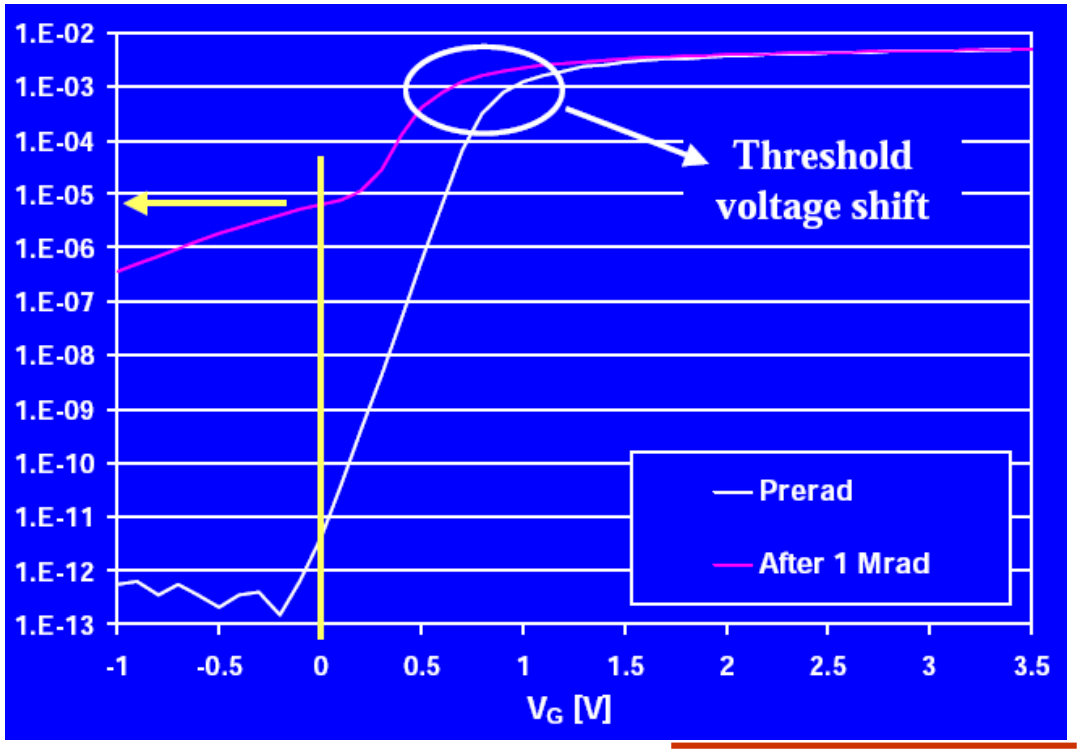


Leakage currents due to field oxides

- The radiation induced increase in the drain current results from the superposition of the current contributions from several, small parasitic transistors in parallel; subthreshold current may increase of several orders of magnitude after irradiation



After G. Anelli, "Techniques for radiation tolerant design in deep submicron CMOS technology"



Radiation effects on an NMOS transistor from a 0.7 μm CMOS process (t_{OX}=17 nm)

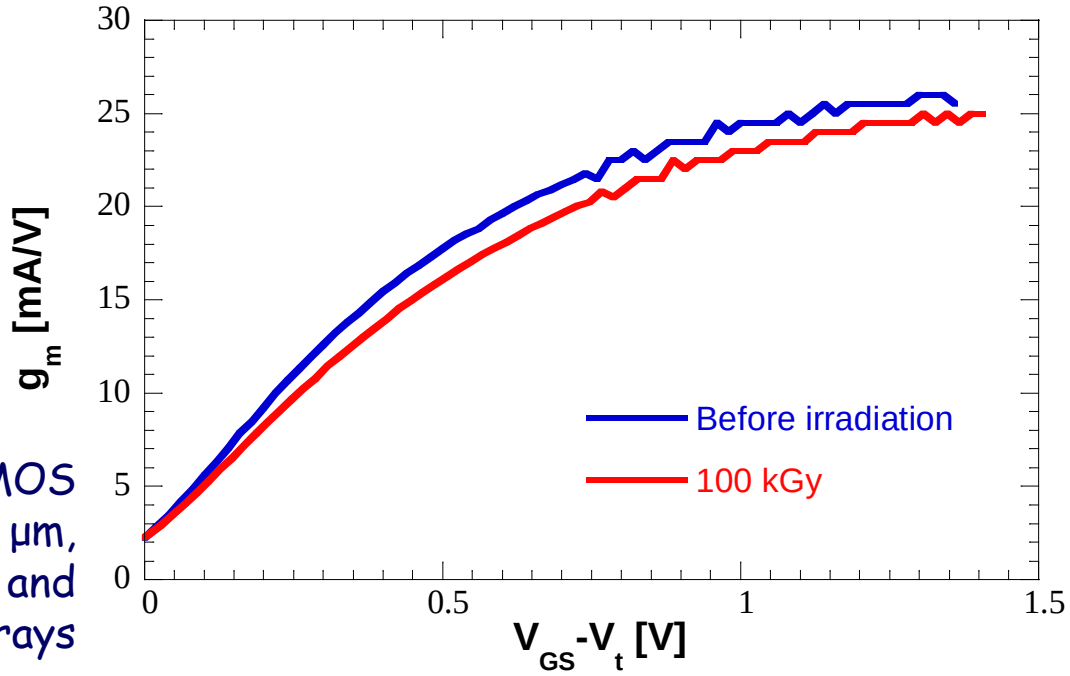
Mobility degradation

- Increase of interface traps is also responsible for a degradation in the carrier mobility μ according to the following relationship

$$\mu = \frac{\mu_0}{1 + \alpha \cdot \Delta N_{IT}}$$

- μ_0=pre-irradiation mobility
- α=mobility degradation parameter (≈10^{-12} cm^2)
- ΔN_{IT}=interface trap increase

- The change in the mobility has a direct effect on the device transconductance (defined as the derivative of the drain current with respect to the gate-to-source voltage)



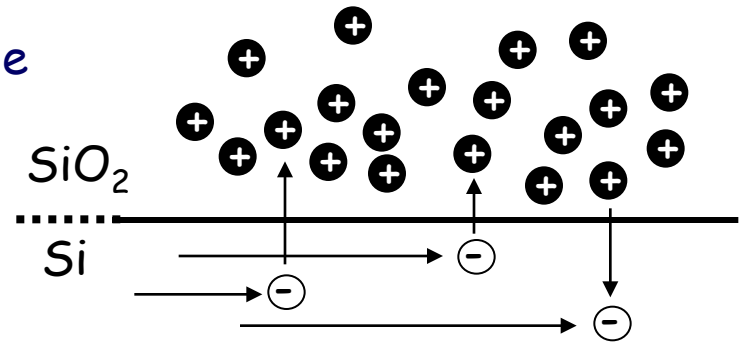
Transconductance g_m in an NMOS device with W/L=200 μm/0.7 μm, from a 0.35 μm process before and after exposure to ^{60}Co γ-rays

Annealing

- Holes trapped in the SiO_2 of an MOS structure are not truly permanently trapped; actually, they are observed to disappear from the oxide over times from milliseconds to years; this discharge of the hole traps, commonly observed near room temperature, is the major contributor to the so-called long-term annealing of radiation damage in MOS devices
- Annealing of trapped holes has two manifestations, which may reflect different hole removal processes
- A slow bias-dependent recovery of ΔV_{OT} typically observed at normal device operating temperatures (-55° to 125°C); such a process has been described through a **tunneling** model
- A relatively rapid and strong temperature-dependent removal or recombination of the holes observed when MOS structures are deliberately subjected to thermal annealing cycles at elevated temperature (150° to 350°C); this process has been described through a **thermal detrapping** model

Tunnel annealing

- The tunneling model assume that electrons from the silicon tunnel to and recombine with the trapped holes in the distribution of traps near the SiO_2 interface (or holes tunnel from the traps to the silicon valence band)



- As a consequence of the exponential decay of the tunneling probability with the distance into the SiO_2, at a given time **t** the hole traps are emptying at a depth $X_m(t)$ from the silicon according to the following equation, valid under the assumption of uniform trap distribution in the oxide

$$X_m(t) = \left(\frac{1}{2\beta}\right)\ln\left(\frac{t}{t_0}\right)$$

- β=tunneling barrier height parameter
- t_0=time scale parameter

- It was experimentally observed that applying a positive (with a higher potential on the metal side in the MOS structure) electric field has the effect of increasing the annealing rate; this can be explained by the fact that a positive electric field lowers the barrier to tunneling

Thermal annealing

- Electrons in SiO_2 valence band can acquire enough energy to jump into the conduction band and recombine with trapped holes; this process can be modeled with an emission probability $\mathbf{p_{em}}$ of an electron from the valence band of the silicon dioxide to the traps where holes are located

$$p_{em}(T) = AT^2 \cdot \exp\left(-\frac{q\varphi}{k_B T}\right)$$

- A=constant depending on trap cross section
- T=absolute temperature
- φ=energy difference between the trap level and the valence band

- The emission probability is strongly temperature dependent

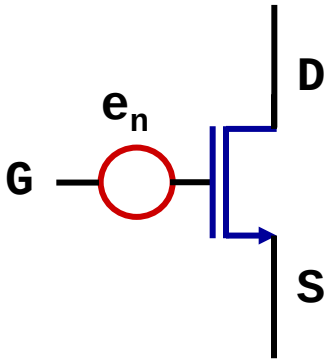
- A couple of different annealing techniques are used to study the nature and distribution of SiO_2 bulk traps
  - In **isochronal annealing** tests, the device is subjected to temperature increments and parameter measurements at regular time intervals
  - In **isothermal annealing** tests, the sample is heated at a constant temperature for a given duration of time

Electronic noise

- The word "noise" is used to indicate spontaneous fluctuations of electric variables taking place in passive and active electronic devices
- Electronic noise originates from the fundamental physical phenomena which underlay the operation of electronic components (e.g., thermal agitation of charge carriers, granularity of electric charge); such phenomena cannot be eliminated without denying fundamental physical laws
- Noise has a different nature from that of other disturbances coming from the environment (e.g., 50/60 Hz harmonics from the power supply, electromagnetic induction from other circuits), which, at least theoretically, can be suppressed by shielding or filtering techniques.
- Noise may impair the capability of a circuit to accurately measure the amplitude of a signal and represents the unavoidable, final limitation to the performance of an electronic system
- Since noise is a random process, its properties can be described only through statistical tools and quantities (e.g. mean square value, root mean square, or rms, value, power spectral density)

Noise in field-effect transistors

- Noise in a MOSFET can be circuitally described by means of a voltage source e_n in series to the gate terminal of the device; this source, formally represented by means of its power spectral density, includes two terms
  - a frequency independent one (S_W), dominated by the channel thermal noise, which originates from thermal agitation of carriers in the device channel (the white noise component may include contributions from parasitic resistors, not considered here)
  - a term which is inversely proportional to the frequency, also called 1/f or flicker noise, which arises from continuous, random capture and release of carriers by border (very close to the Si/SiO_2 interface) traps in the oxide



$$\frac{\overline{de_n^2}}{df} = S_w + \frac{A_f}{f}$$

- f=frequency

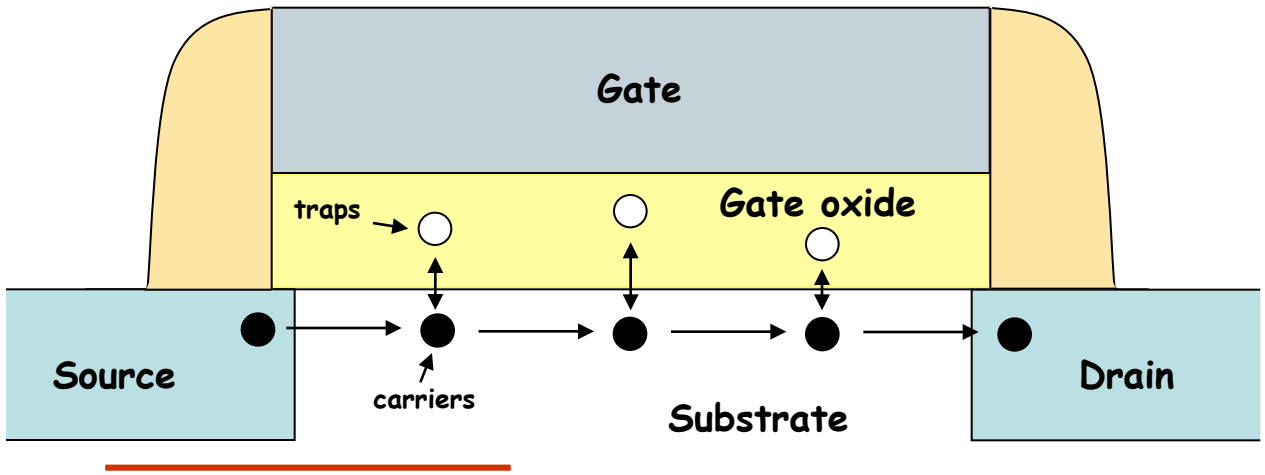
$$S_w = \frac{4k_B T\Gamma}{g_m}$$

$$A_f = \frac{K_f}{C_{OX} WL}$$

- k_B=Boltzmann's constant
- T=absolute temperature
- Γ=channel thermal noise coefficient
- g_m=channel transconductance
- K_f=1/f noise parameter
- W, L=channel width and length

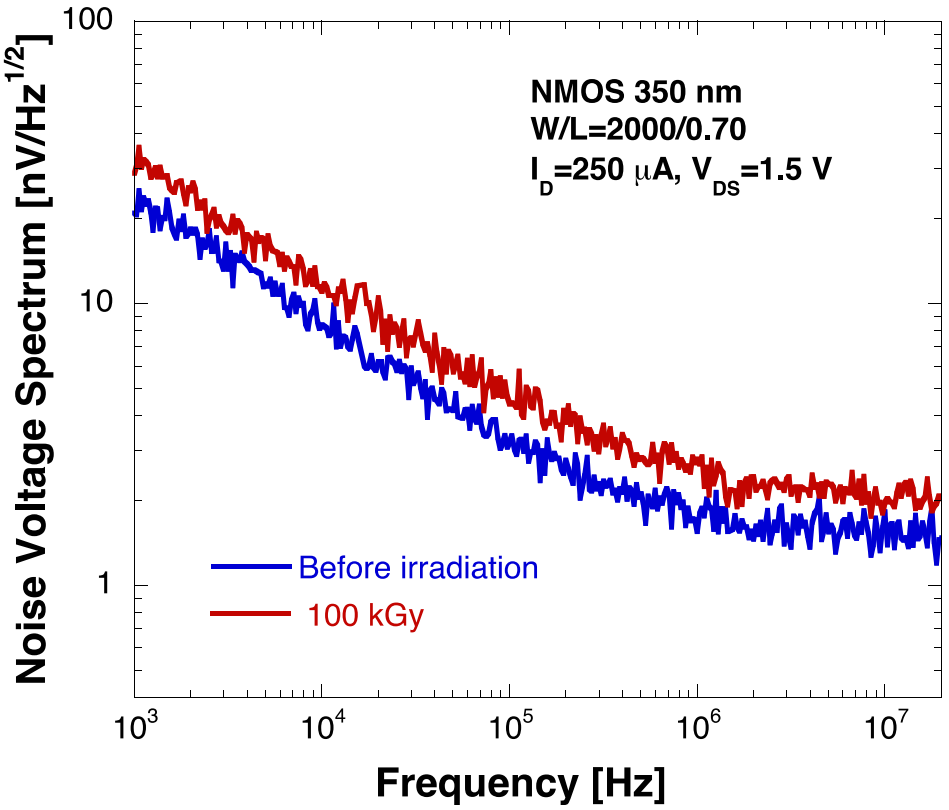
1/f noise in MOSFETs

- In MOSFET devices, 1/f noise is due to the interaction between carriers in the channel and traps in the gate oxide; the process of random capture and emission of carriers is responsible for a fluctuation in the number and mobility of carriers, resulting in a stochastic fluctuation of the drain current
- Experimental investigations show that 1/f noise is almost entirely due to the so-called border traps, traps in the oxide located within 3 nm of the Si/SiO_2 interface, which can exchange charge with the underlying channel with characteristic times of the same order of an electrical measurement
- Border traps exchange charge with the channel with a probability exponentially decreasing with the trap distance from the Si/SiO_2 interface
- The definition of a trap as a border trap depends also on the operating conditions (in particular on the gate-to-source voltage, V_{GS})



Noise increase in irradiated MOSFETs

- Exposure to ionizing radiation also affects the noise performance in MOSFET devices
- As far as white noise is concerned, the gate referred power spectral density (the noise voltage spectrum is the square root of the power spectral density) increases due to the radiation induced reduction of the channel transconductance g_m
- Flicker noise increase is correlated with the increase in positive trapped charge close to the interface and with the increase in the number of border traps



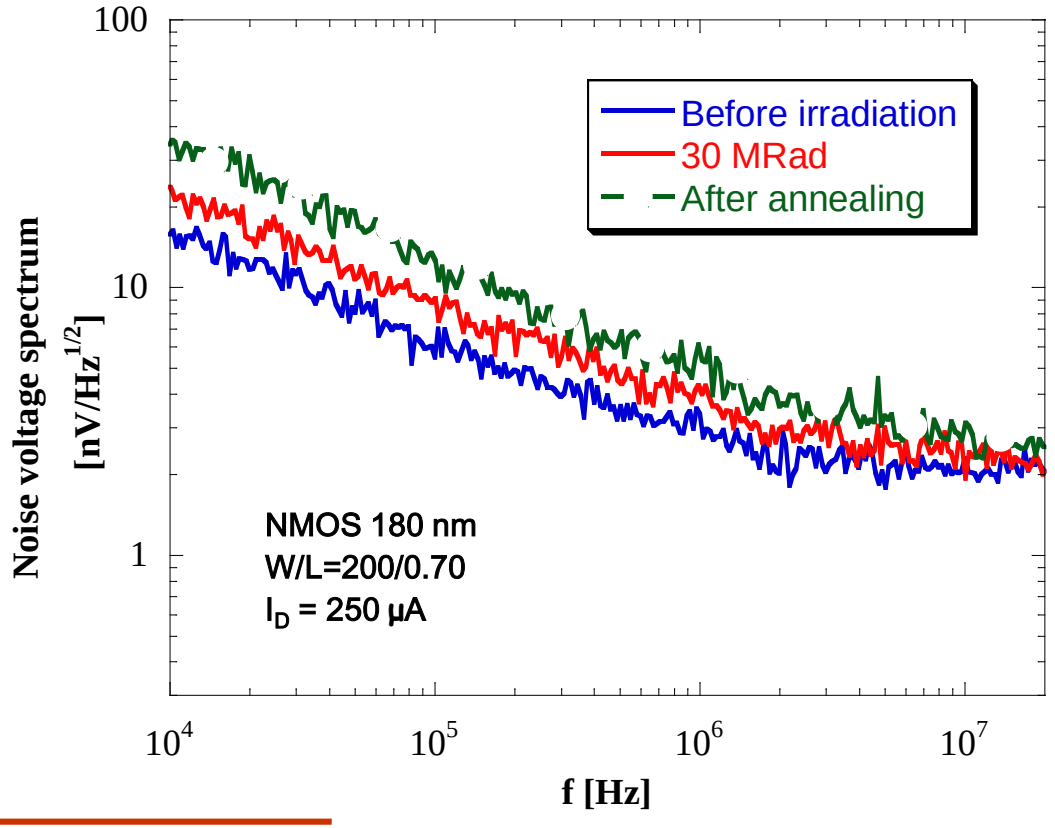
Gate referred noise voltage spectrum in an NMOS device with W/L=2000 μm/0.7 μm, from a 0.35 μm process before and after exposure to ^{60}Co γ-rays

Effects of bias conditions during annealing

- Going from 350 nm to 180 nm minimum channel length, CMOS technologies have become radiation-harder from the standpoint of channel thermal noise; this trend is preserved in the subsequent CMOS generations and is correlated to technology scaling (more on the subject in the following); a sizable degradation in flicker noise can still be detected

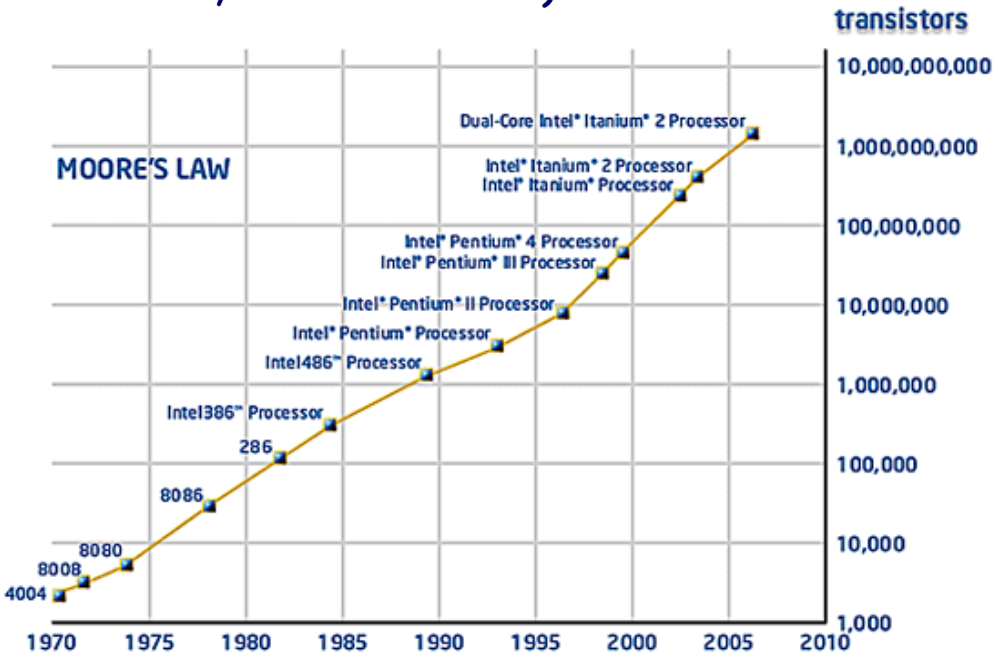
- Further degradation is detected after annealing with all the device terminals grounded (no field across the oxide); this effect has been correlated with an increase in the oxide trapped charge

Gate referred noise voltage spectrum in an NMOS with W/L=200 μm/0.70 μm, from a 180 nm process before and after exposure to ^{60}Co γ-rays under worst case bias conditions (V_G=1.8 V, all other terminals grounded) and after annealing with all terminals grounded



CMOS roadmap

- While fundamental physical processes of radiation damage remain the same, CMOS processes, following Moore's law, are rapidly evolving yielding ever larger scale of integration and processing speed
- Power and speed performance optimization is obtained by progressively reducing the bias voltage (VDD) and the horizontal device dimensions (i.e., the device channel length); this leads to the so-called short channel effects, which may result in a deviation from the expected behavior of the transistor (e.g., excess high frequency noise, carrier mobility saturation, hot electrons)
- In order to alleviate short channel effects, also vertical dimensions of the device (gate oxide thickness, source and drain junction depth) are reduced

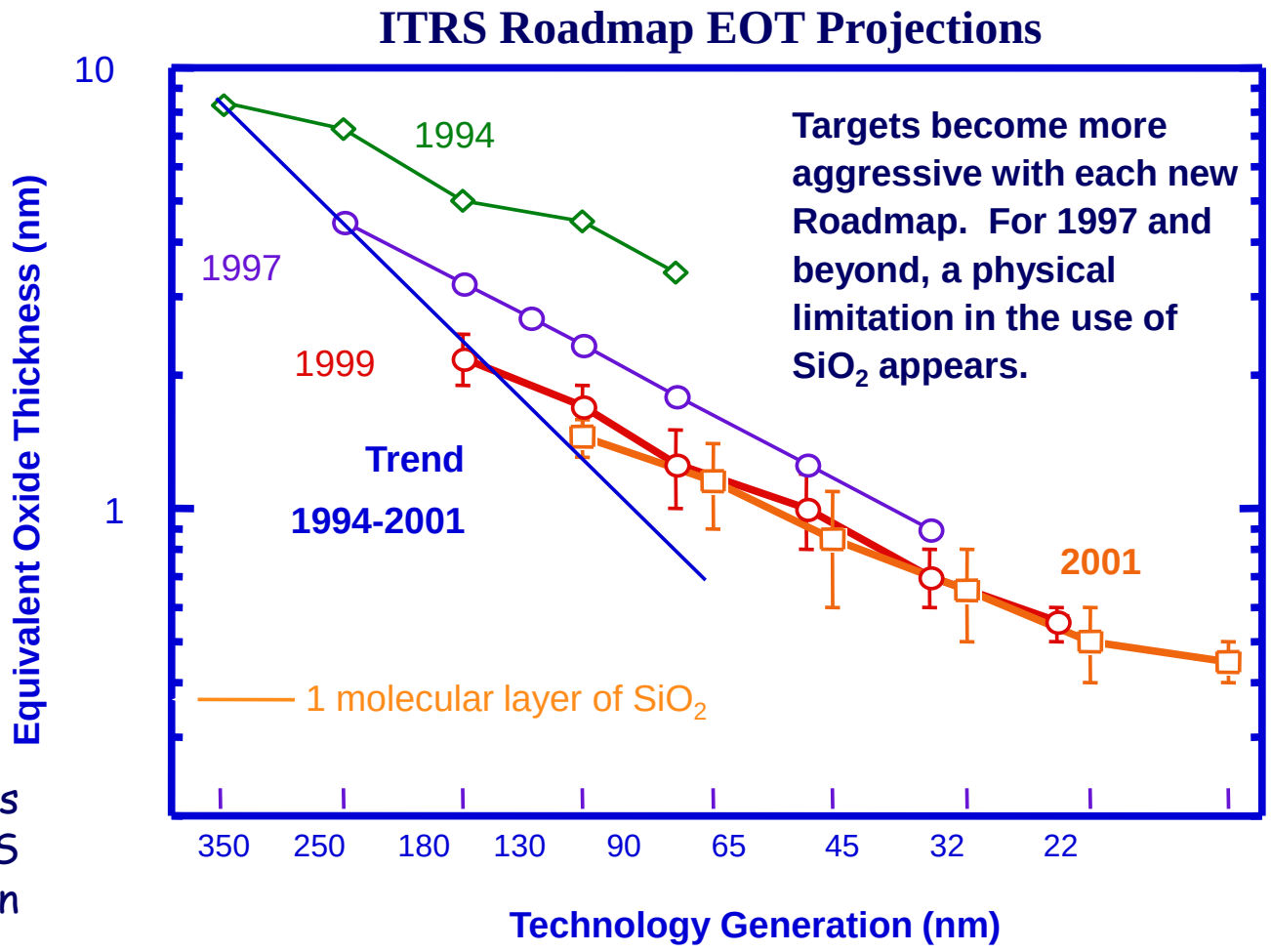


CMOS roadmap

Oxide scaling and radiation effects

- Device scaling (increase in speed and circuit complexity per unit of chip area) requires decreasing the oxide thickness

- Change in the geometrical features of the transistor may result (and actually does result) in a change of the impact of radiation damage processes on the devices fabricated with the new technologies

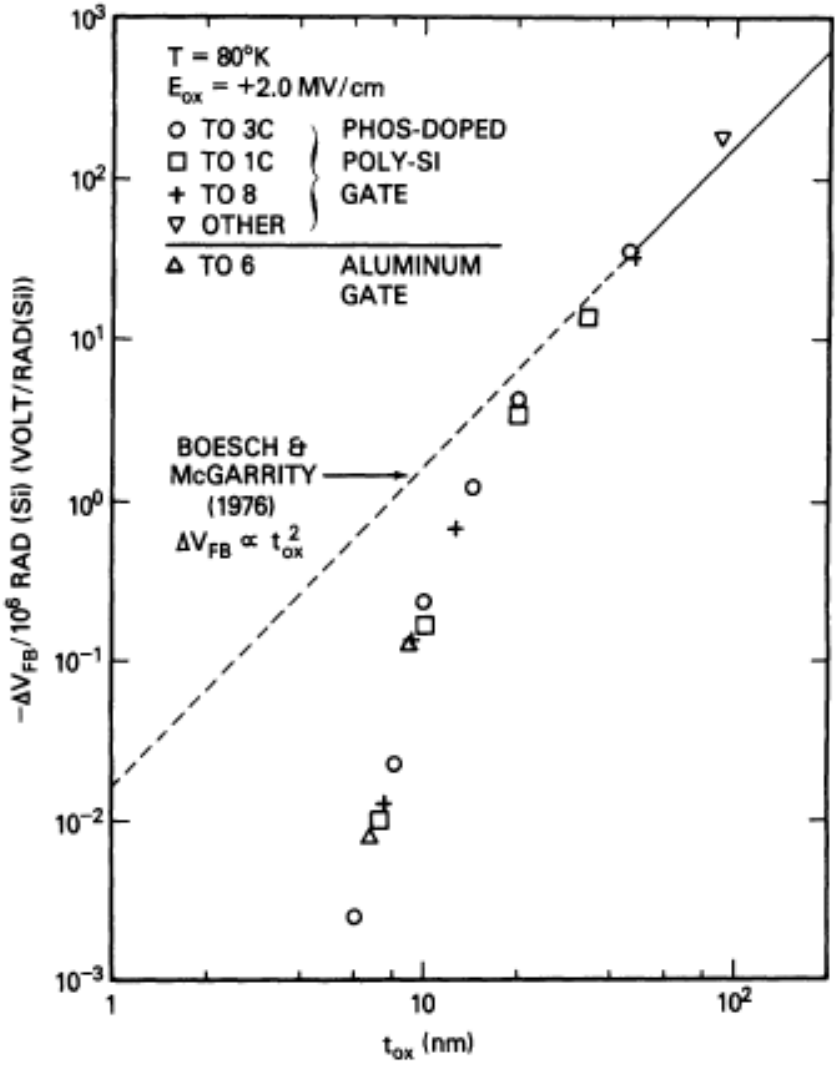


Trend of the oxide thickness as a function of the CMOS generation

Oxide scaling and radiation effects

- For t_{OX} values above 30 nm, as t_{OX} decreases, variation of flat-band voltage in ^{60}Co irradiated MOS capacitors is found to decrease with the square of the oxide thickness, in good agreement with the theoretical behavior; for t_{OX}<20 nm considerable discrepancy between experimental data and expected behavior is observed; these results were found to be independent of the way the oxide was processed

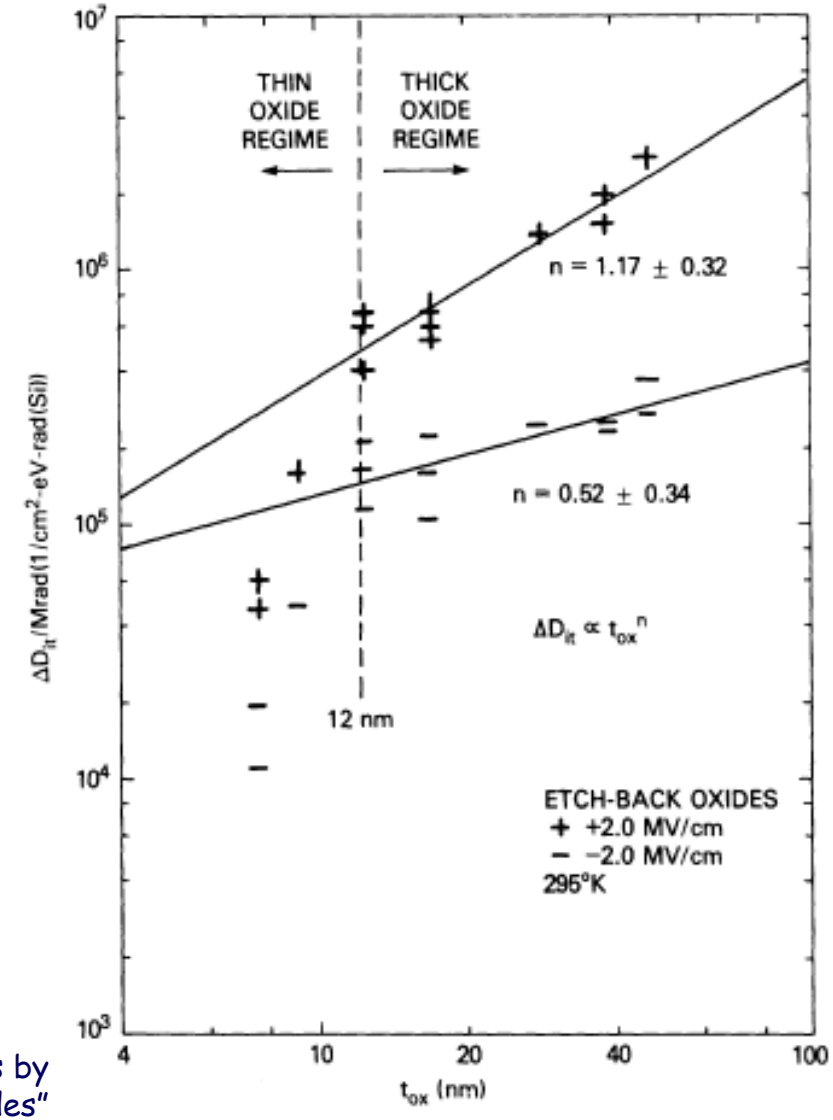
After N.S. Saks et al., "Radiation effects in MOS capacitors with very thin oxides at 80°K"



Flat-band voltage variation per Mrad dose (^{60}Co) for MOS capacitors, biased with a 2MV/cm field, as a function of oxide thickness; the plot also shows the anticipated proportionality to t^2_{OX}

Oxide scaling and radiation effects

- As t_{OX} decreases, the density of radiation-induced interface traps, D_{it}, in MOS structures tends to decrease with a given power **n** of the oxide thickness; however, for thin oxides (t_{OX}<12 nm), the rate of decrease of D_{it} is much larger than extrapolated from the power law behavior for thicker oxides

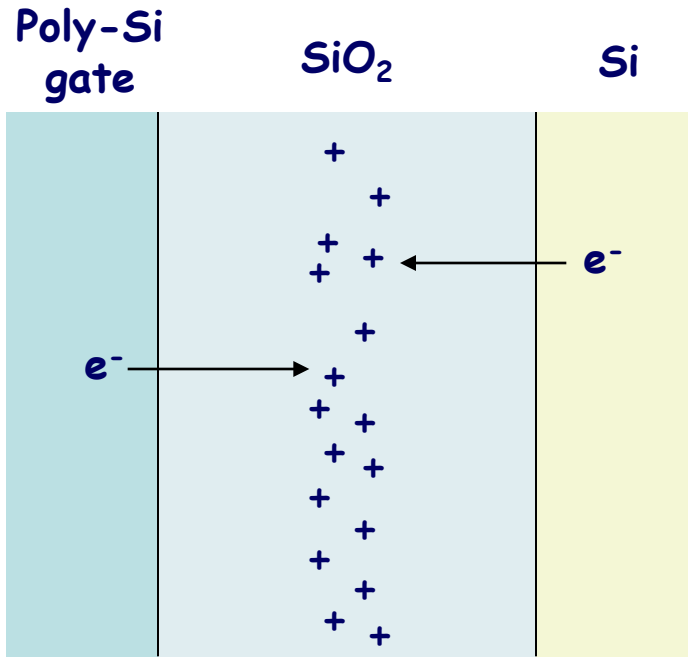


Dependence of interface trap density (D_{it}) on the oxide thickness in etchback oxides

After N.S. Saks et al., "Generation of interface states by ionizing radiation in very thin MOS oxides"

Oxide scaling and radiation effects

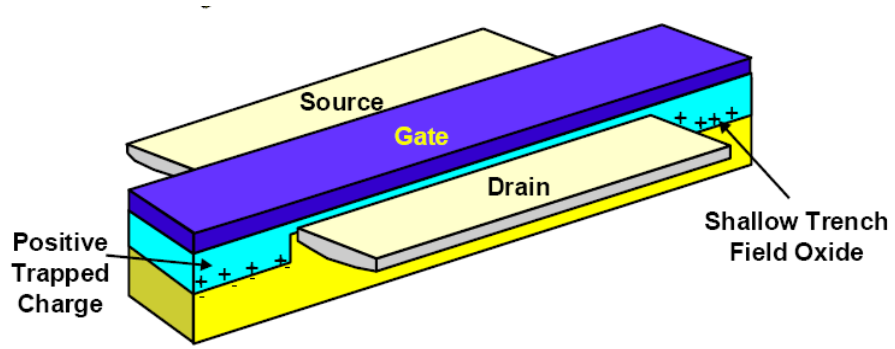
- Hole removal from the gate oxide proceeds via a "tunneling front" which moves into the oxide with a "velocity" of about 0.2 nm per decade in time
- The time-dependent tunneling distance $X_m(t)$ lies in the range from 2 to 4 nm for practical time of interest, say from 1 ms to 10^6 s; hence, for oxides less than 10 nm in thickness, one could expect enhanced hole removal to occur by electrons tunneling into the oxide also from the gate electrode
- Device scaling brings about an improved radiation-tolerance due to the enhanced recovery by trapped hole recombination with tunneling electrons from both the gate and the transistor channel

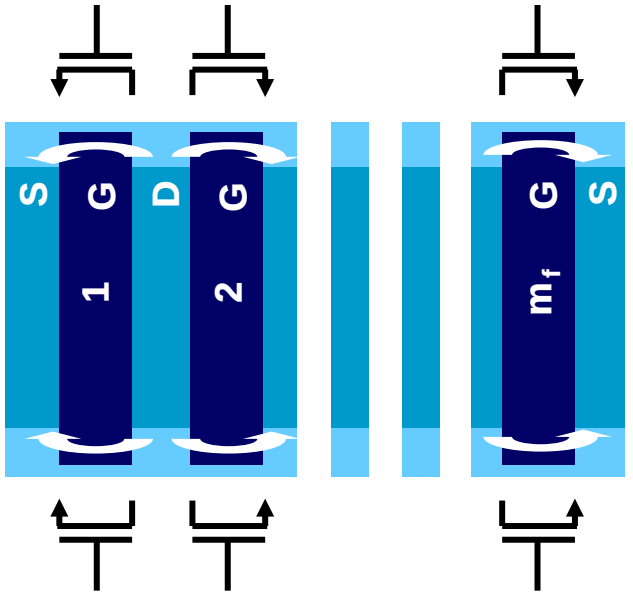


MOS structure and trapped charge tunnel annealing

Deep submicron and nanoscale technologies

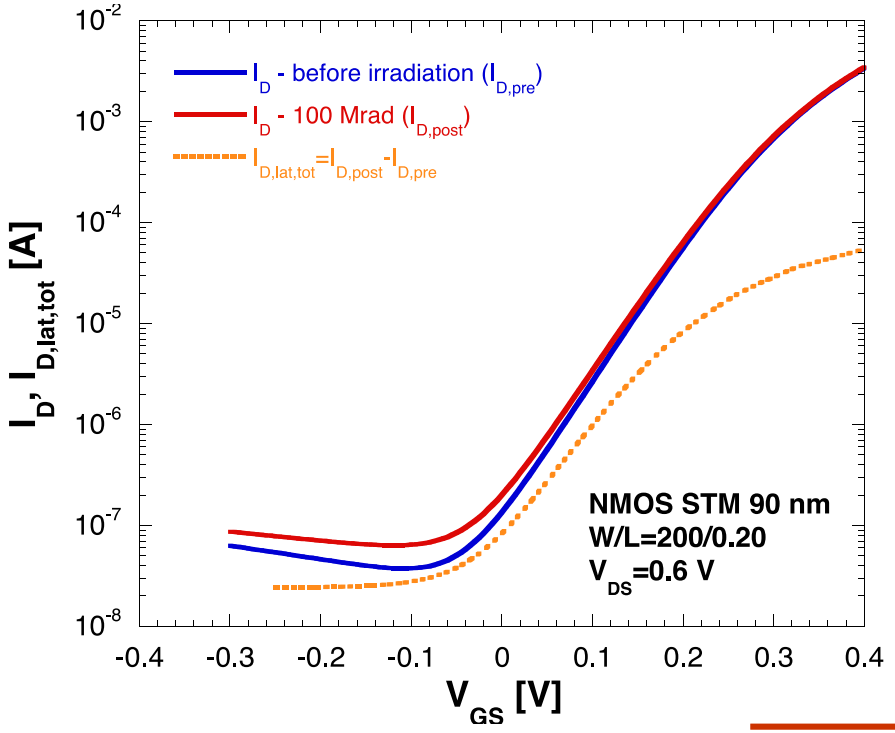
- At smaller integration scales (starting from the 130 nm process) the parasitic devices switched on by charge accumulation in the shallow trench isolation oxides (STI) affects electronic noise and static properties of NMOS transistors
- In a stacked NMOSFET including $\mathbf{m_f}$ fingers, radiation may create 2 x m_f theoretically identical parasitic transistors sharing the same channel length **L** with the main device
- Each parasitic device turned on by charge build-up in the STI oxide contributes to the overall noise of the transistor, particularly in the low frequency range and at low current densities (i.e., low I_D/W)

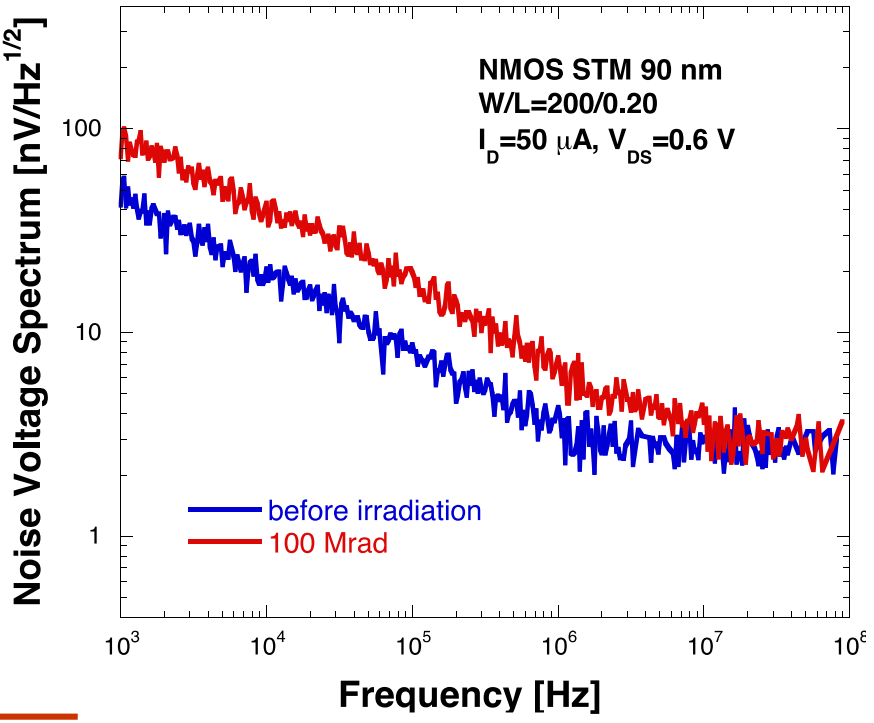




STI effects on static and noise properties

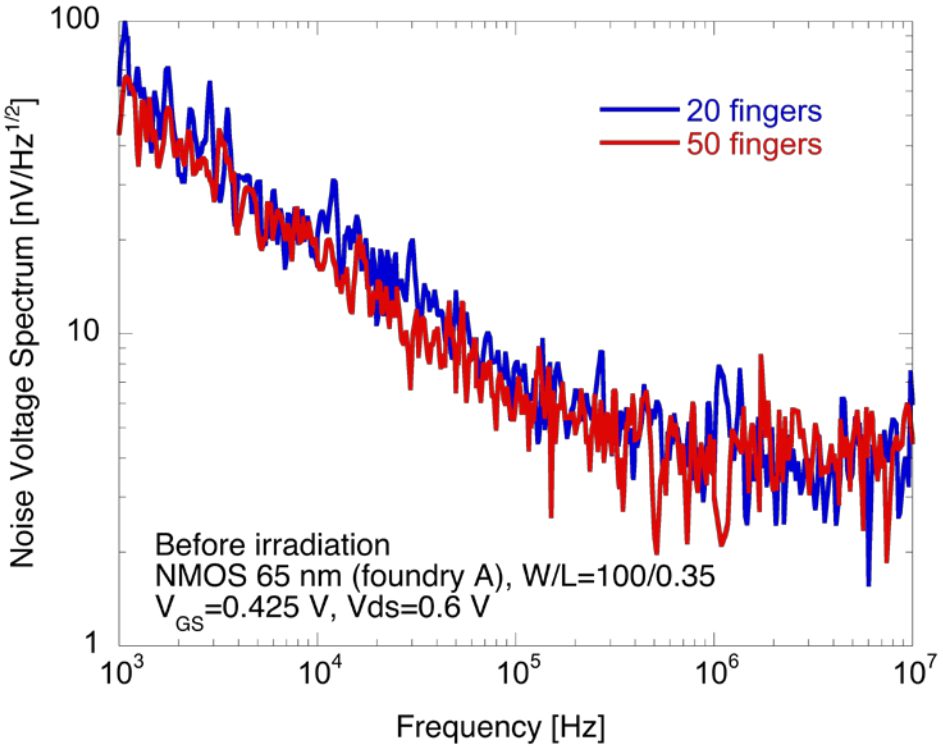
- Due to radiation-induced charge accumulation in the STI field oxide
  - a small change in the drain current, relatively high at small drain current values, can be detected
  - a significant change in low frequency (1/f) noise can be observed, in particular at low current densities
- No significant changes, even at extremely high doses, can be detected in the threshold voltage of wide channel devices (confirming the high degree of radiation-tolerance of the gate oxide)

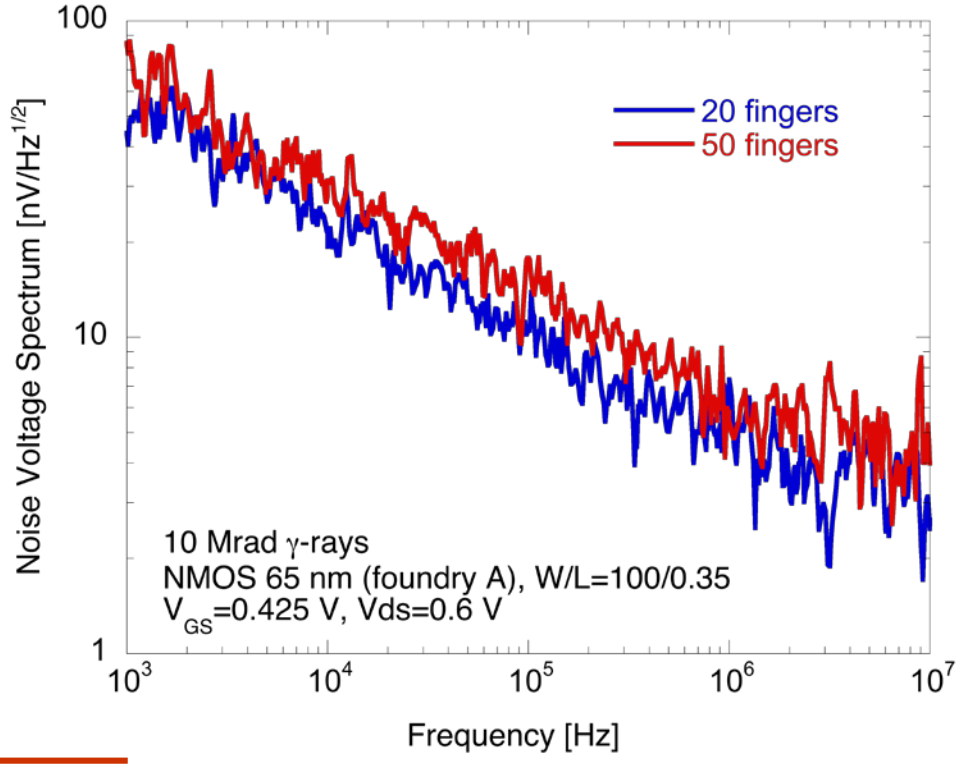




Dependence on the number of fingers

- A larger low frequency noise increase is detected in irradiated devices with larger number of fingers (remember, two parasitic devices are created for each finger)
- For radiation hardness performance purposes, m_f should be as small as possible; on the other hand, a small number of fingers may dangerously increase the distributed gate resistance (and the relevant noise contribution)

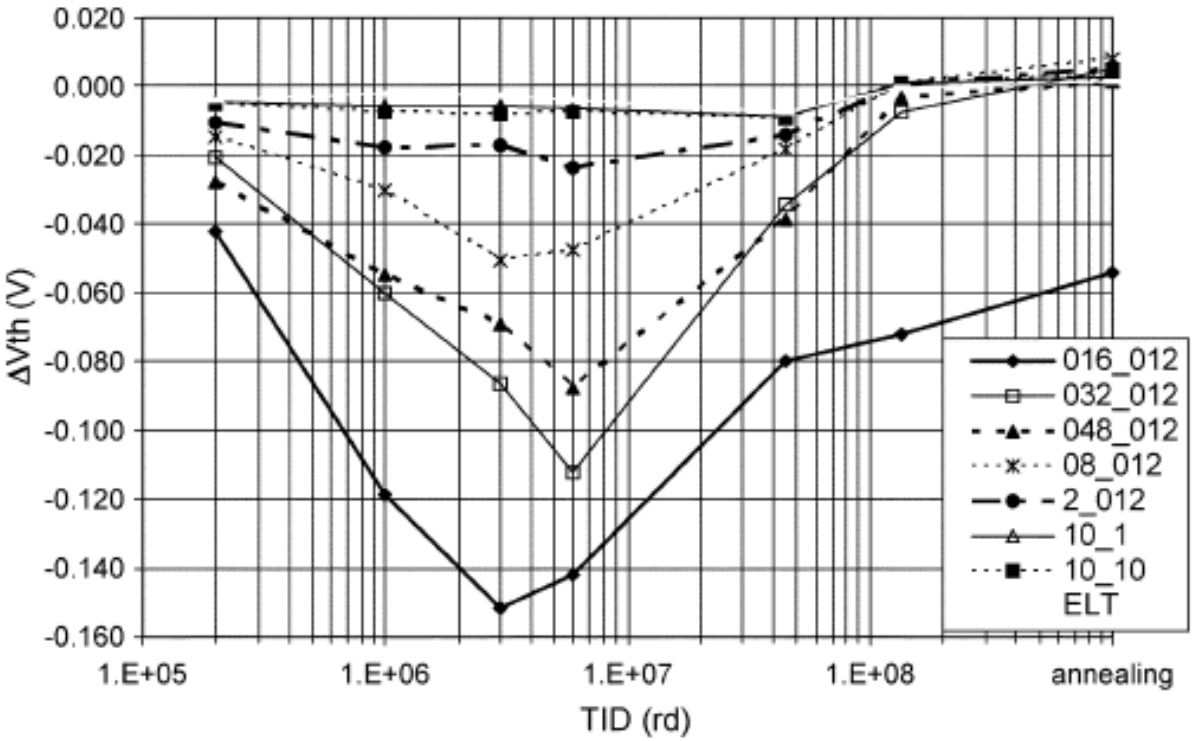




Radiation induced narrow channel effect (RINCE)

- While no change in the threshold voltage can be detected in MOSFET devices with large channel width, narrow channel devices were found to feature a peculiar behavior
- Positive charge trapped in the lateral STI oxide influences the electric field in the main transistor (narrow channel effect); it decreases the threshold of sufficiently narrow NMOS transistors, while increasing it (in absolute value) for PMOS transistors
- Also drain leakage current is affected by radiation-induced narrow channel effect

After F. Faccio et al., "Radiation-induced edge effects in deep submicron CMOS transistors"



Change in the threshold voltage as a function of the total ionizing dose in narrow channel transistors from a 130 nm CMOS technology

Evolution of radiation effects in MOSFET

- Radiation-induced threshold voltage shift has been gradually eliminated by the natural evolution of advanced microelectronic technologies, where the gate oxide thickness has been reduced generation after generation

- Now the main radiation hardness issues in microelectronic circuits are those relevant to the isolating structures (radiation induced leakage currents, positive charge build-up in the field oxide, in particular the shallow trench isolations), affecting both static and noise properties of MOSFET devices, together with single event effects

- Gate oxides with dielectric constant larger than in SiO_2 (High-K oxides) will be used to reduce the gate leakage current and alleviate some reliability issues; on the other hand, such new dielectric materials still need to be appropriately tested from the standpoint of radiation-tolerance

Radiation resistant technologies and hardening techniques

Radiation hardening techniques

- In some cases, mainstream market forces, which drive the evolution of microelectronic technologies, may indirectly improve the radiation resistance of electronic devices (e.g., device speed in bipolar transistors, device scaling in complementary MOSFETs)
- Whenever a device is not sufficiently radiation hard for the foreseen application, some measures can be taken to make it harder; this can be obtained by
  - modifying the device geometrical layout (**hardening by layout**)
  - modifying one or more steps of the fabrication process (**hardening by process**)
  - suitably designing the overall circuit or system (**hardening by design**)

Radiation hard technologies

- Commercial technologies for integrated circuits commonly evolve by improving on speed, scale of integration, complexity and power dissipation; many of the technology developments needed to achieve these results have been beneficial in terms of radiation-tolerance

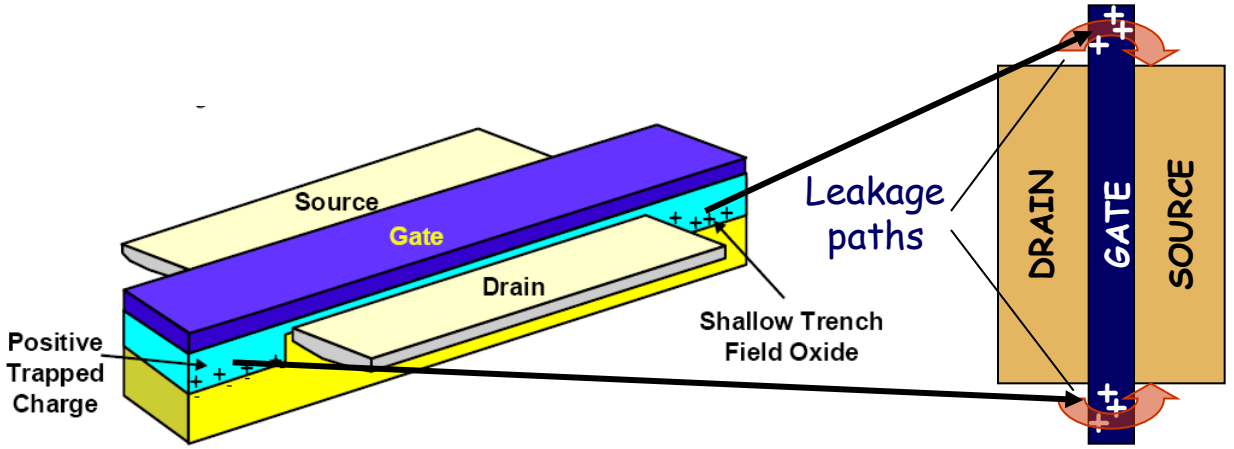
- Commercial deep submicron CMOS technologies can already provide total ionizing dose hardness levels in the range of several units up to several tens of megarad; use of ultra-thin (a few nm) oxides limits the effects of oxide trapped charge; use of thin epitaxial layers, retrograde wells and shallow trench isolation improve hardness against latch-up

- SOI technology is of significant commercial interest because of the advantages it offers in terms of speed, power and integration density; the fact that it also offers total device isolation is an advantage in terms of radiation effects; because of the insulating layer, the technology is immune to destructive latch-up

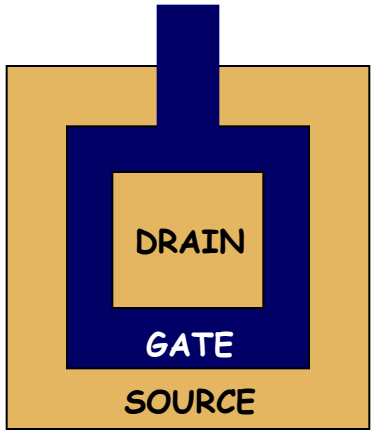
Hardening by layout

- In irradiated NMOS devices, positive charge trapped in the shallow trench isolation oxides is responsible for the formation of conductive paths along the STI sidewalls
- If an enclosed layout is used, no parasitic path can form between source and drain, because there is no thick oxide layer running along the main channel

Standard layout

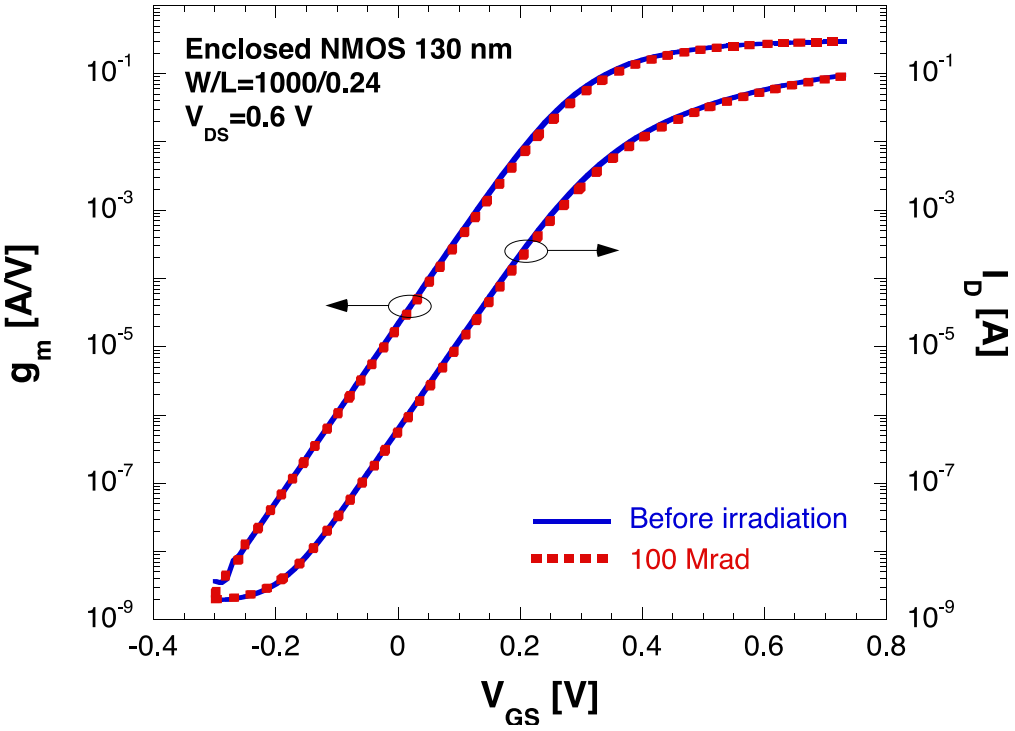


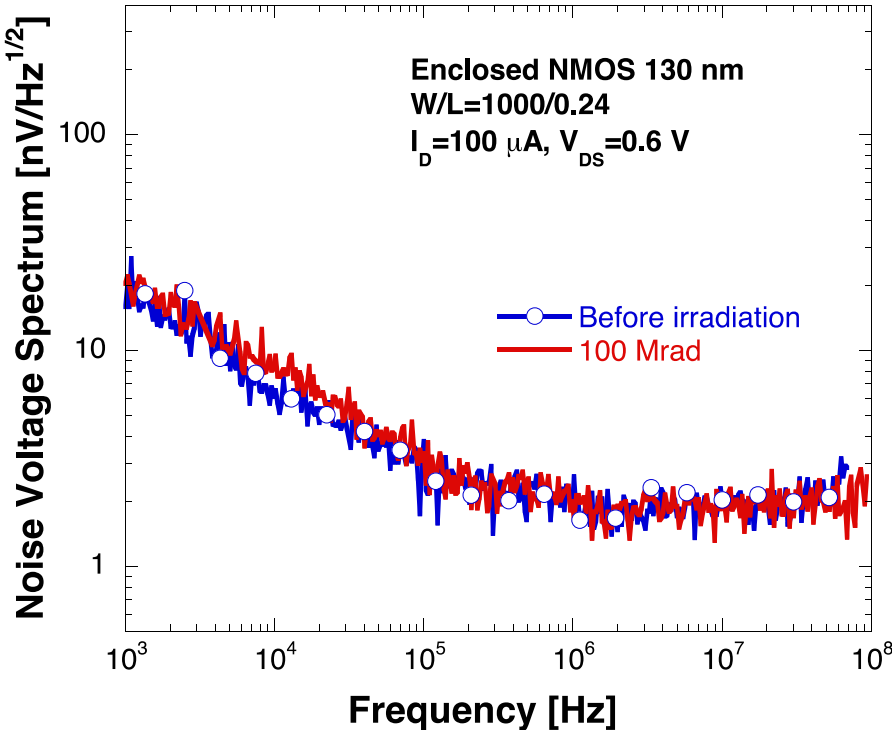
Enclosed layout



Hardening by layout

- In enclosed layout (also called edgeless) NMOS transistors, static and noise properties are affected by radiation to a very limited extent
- This radiation hardening technique has been exploited in the design of the front-end electronics for semiconductor detectors at the Large Hadron Collider experiments

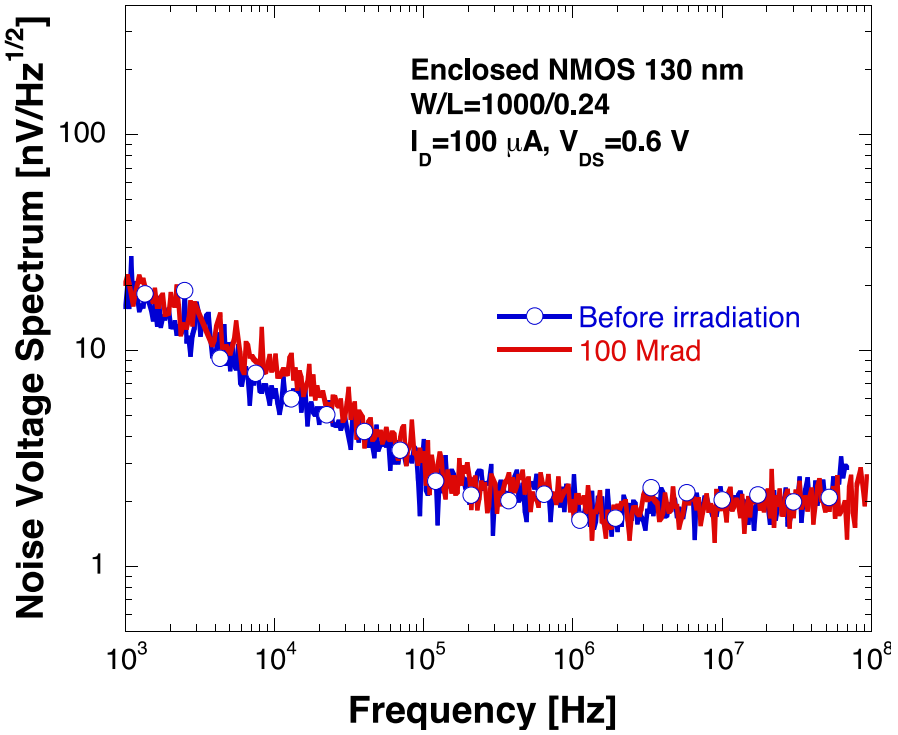




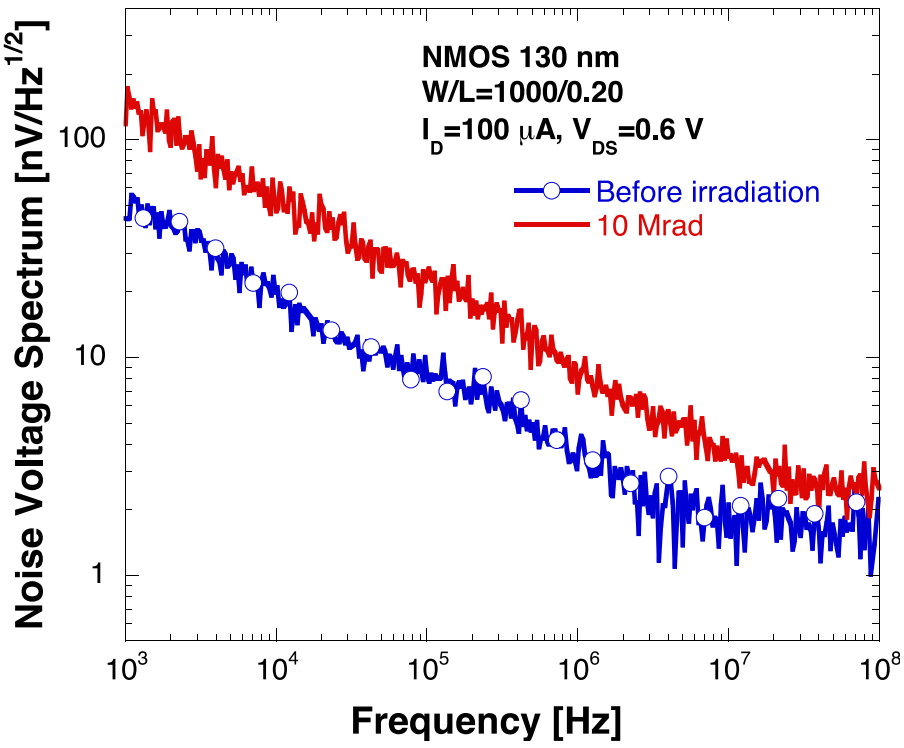
Hardening by layout

- Enclosed layout significantly improves NMOS radiation response with respect to standard interdigitated layout

NMOS 130 nm
Enclosed layout
Dose: 100 Mrad (1 MGy)



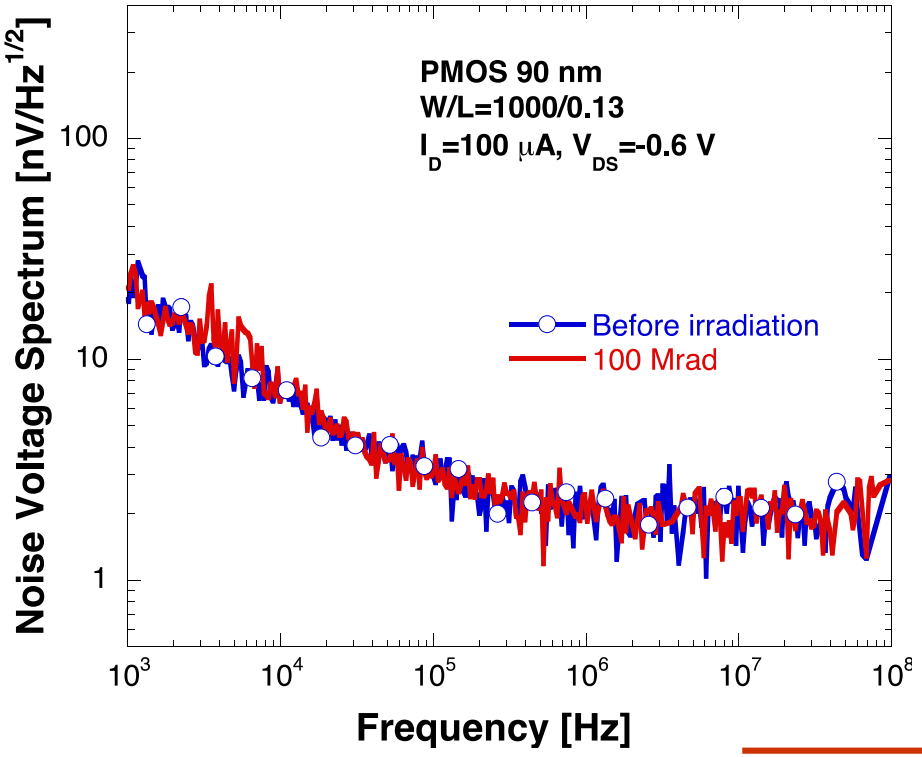
NMOS 130 nm
Standard interdigitated layout
Dose: 10 Mrad (100 kGy)



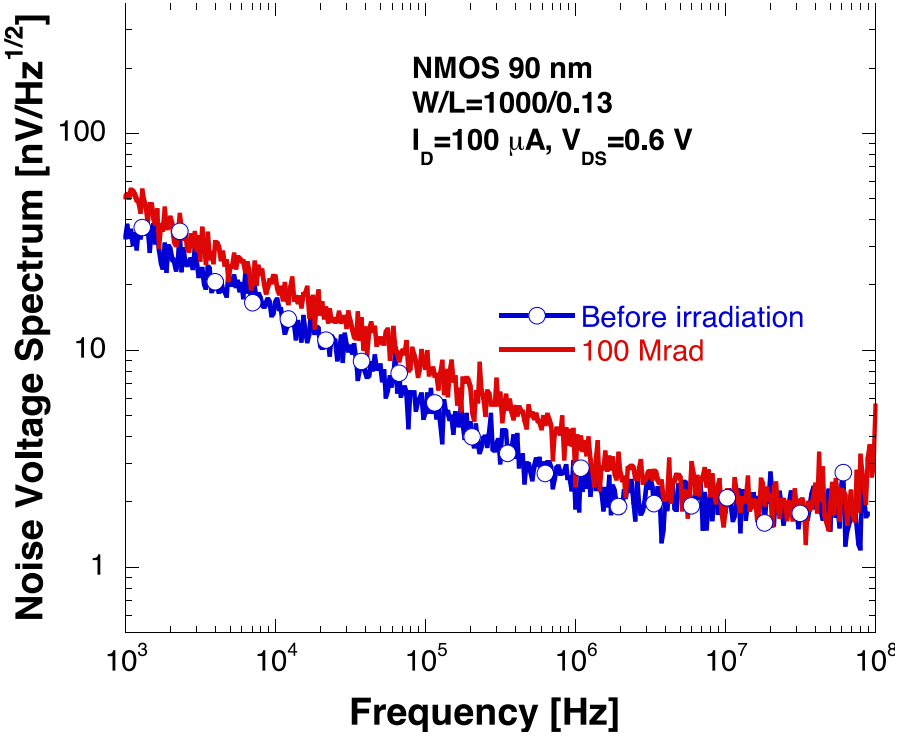
Hardening by choice of the polarity

- PMOS transistors are much harder than NMOS devices; positive charge trapped in the shallow trench isolation oxides has no effect because the substrate is N-type (as a consequence, silicon underneath the STI is accumulated instead of being inverted)

PMOS 90 nm
Standard interdigitated layout
Dose: 100 Mrad (1 MGy)



NMOS 90 nm
Standard interdigitated layout
Dose: 100 Mrad (1 MGy)



Hardening by process and by design

- A large number of steps are involved in the fabrication of a typical MOS integrated circuit and many of these steps can influence the radiation hardness of a device; the most important factors are those which affect the charge trapping characteristics of the oxides (gate oxide, field oxide, intermetal oxide) and the relevant interfaces

- Deep submicron technologies are generally more sensitive to single event upset than older technologies; however, tolerance to SEU can be improved by means of design techniques; in the case of digital circuits, a typical solution involves using logic redundancy, which may consist, for instance, in the triplication of the digital processing chain integrated in a majority voting system (in this case, a radiation-induced error in one bit may be outvoted by the other two, not affected components)

Single event effects in devices and circuits

Single event (transient) effects

- Single event effects are due to a single particle crossing the sensitive area of a device or circuit; some of these events are classified as soft, since they do not induce any physical damage, but only loss of information, such as a bit flip in a memory array; other events, such as the gate oxide rupture following the strike of a heavy ion, are termed hard, because they do induce permanent damage
- The main classes of soft effects are:
  - single event upset (SEU), the corruption of a single bit in a memory array
  - multiple bit upset (MBU), the corruption of multiple bits due to a single particle
  - single event transient (SET), a transient signal induced by an ionizing particle in a combinatorial or analog part of a circuit
- The main classes of hard effects are:
  - single event gate rupture (SEGR), rupture of gate oxide occurring especially in power MOSFETs
  - single event burnout (SEB), burnout of a power device
  - single event latch-up (SEL), the activation of parasitic bipolar structures, leading to a sudden increase of the supply current

Single event (transient) effects

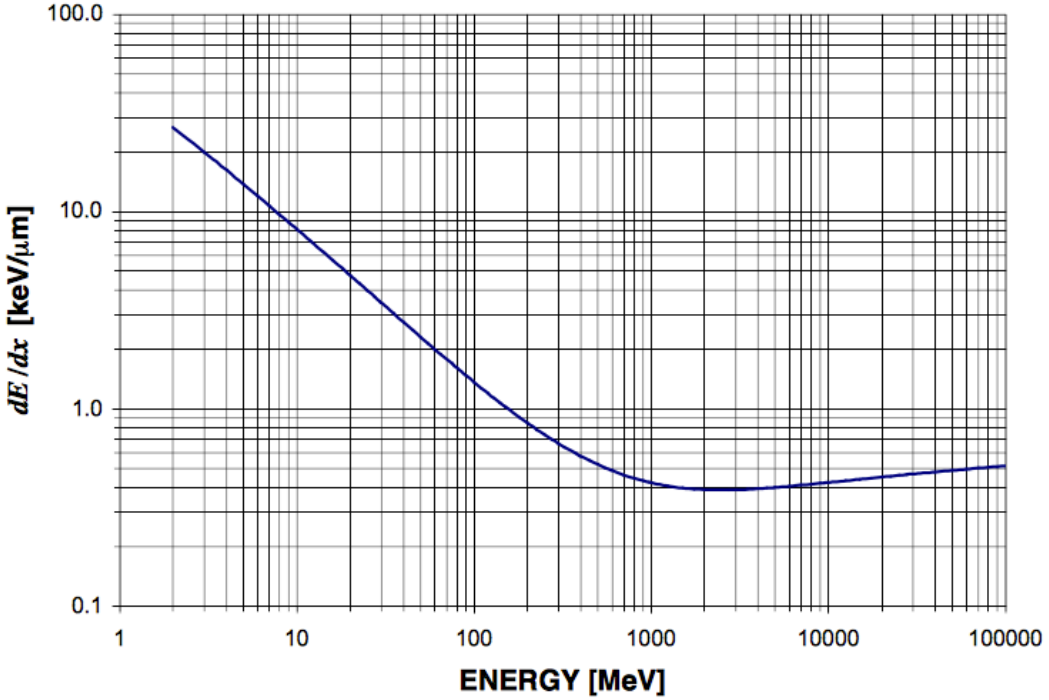
- Single event effects may be generated
  - directly by heavy ions (Z>1)
  - indirectly by recoil fragments due to the collision of protons or neutrons with silicon, oxygen or doping atoms, or with atoms of other species present in the device
- Note that
  - neutrons cannot induce SEEs directly, because they are neutral particles
  - protons generally do not induce SEEs directly, because their LET is too small
  - electrons cannot induce SEEs neither directly, because their LET is too small, nor indirectly, because they cannot determine nuclear reactions (the same holds true for other charged particles such as muons and pions)

Linear energy transfer

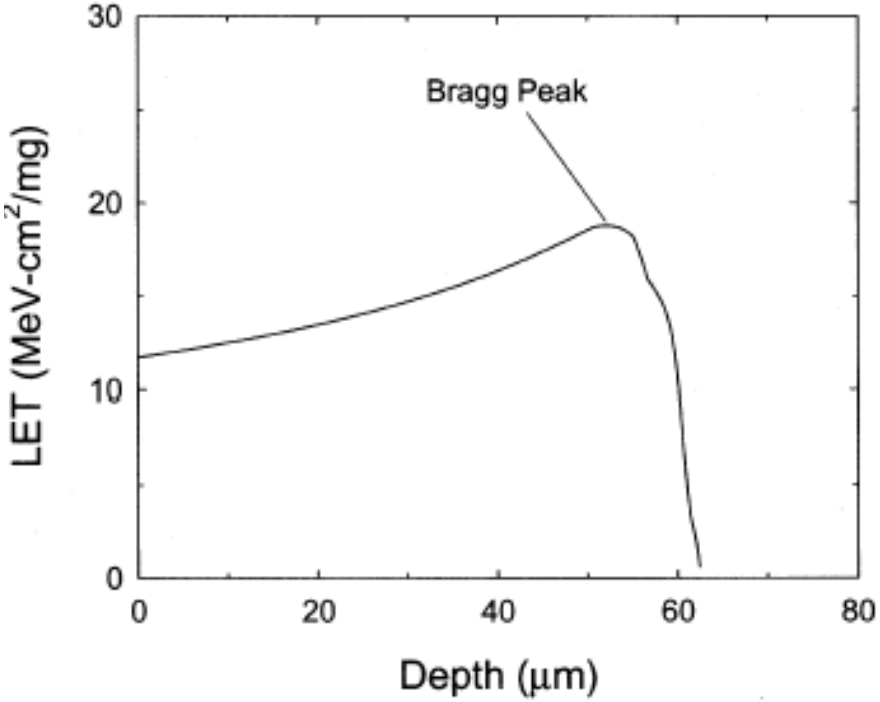
$$\text{LET=linear energy transfer}=\frac{1}{\rho}\frac{dE}{dx}$$

Energy loss due to interaction with the electrons in the target material; depends on

- impinging particle and its kinetic energy
- target material



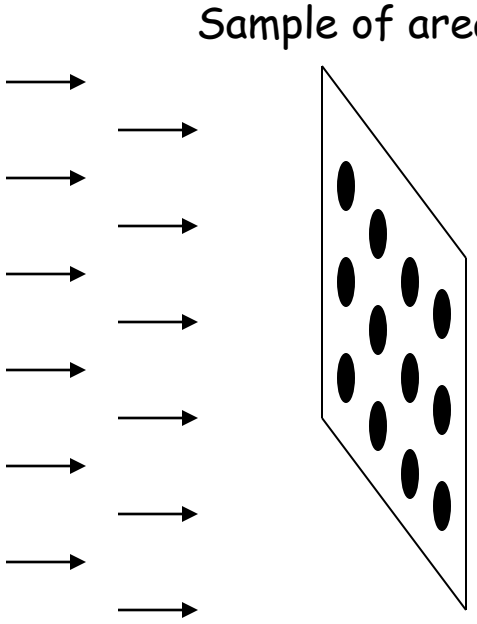
Proton



Chlorine ion@210 MeV

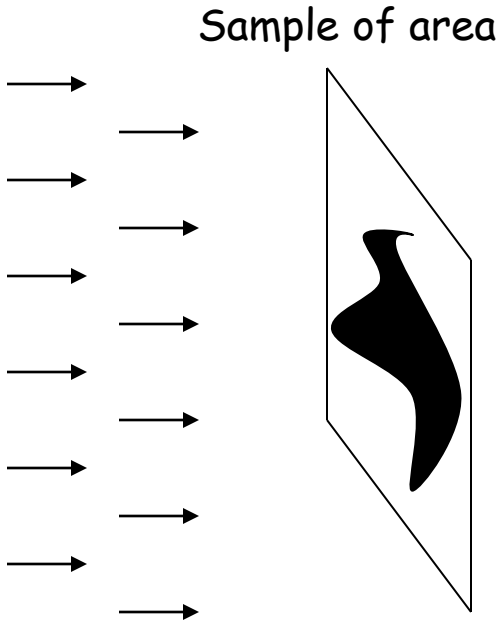
SEE cross section

The cross section is the total area of the sample sensitive to the considered physics effect, independently on how such area is distributed on the sample



N impinging particles uniformly distributed on area A

The cross section σ in the two figures is the total black area of the sample



N impinging particles uniformly distributed on area A

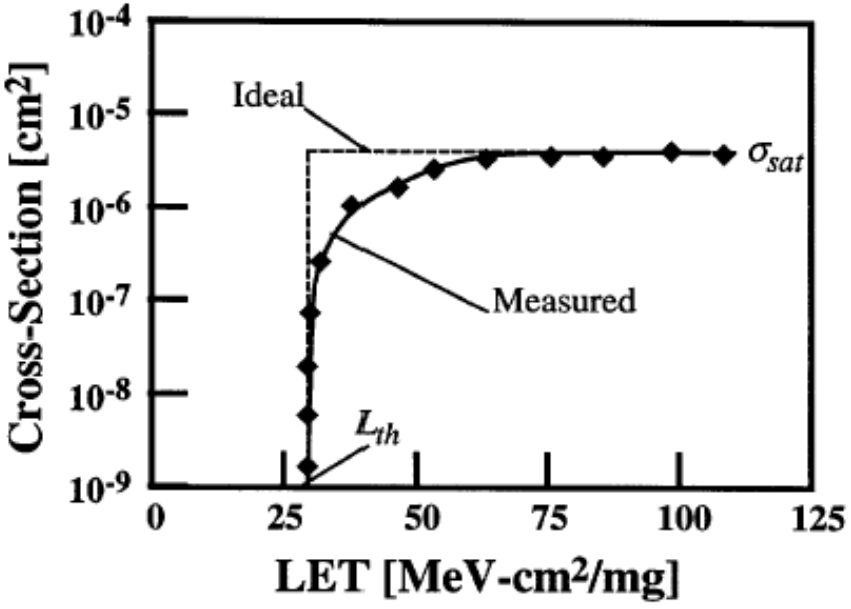
$$N_{Counts} = N \cdot \frac{\sigma}{A} = \frac{N}{A} \cdot \sigma = \Phi \cdot \sigma$$

SEE cross section

- SEEs are generally characterized in terms of their cross section, expressed as

$$\sigma_{SEE} = \frac{\text{number of events}}{\text{particle fluence}} = \frac{N_{Counts}}{\Phi}$$

- Cross section varies as a function of the impinging particle LET (linear energy transfer, giving a measure of the energy deposited by the particle); a particle produces an observable effect if its LET is larger than the threshold LET



Weibull curve

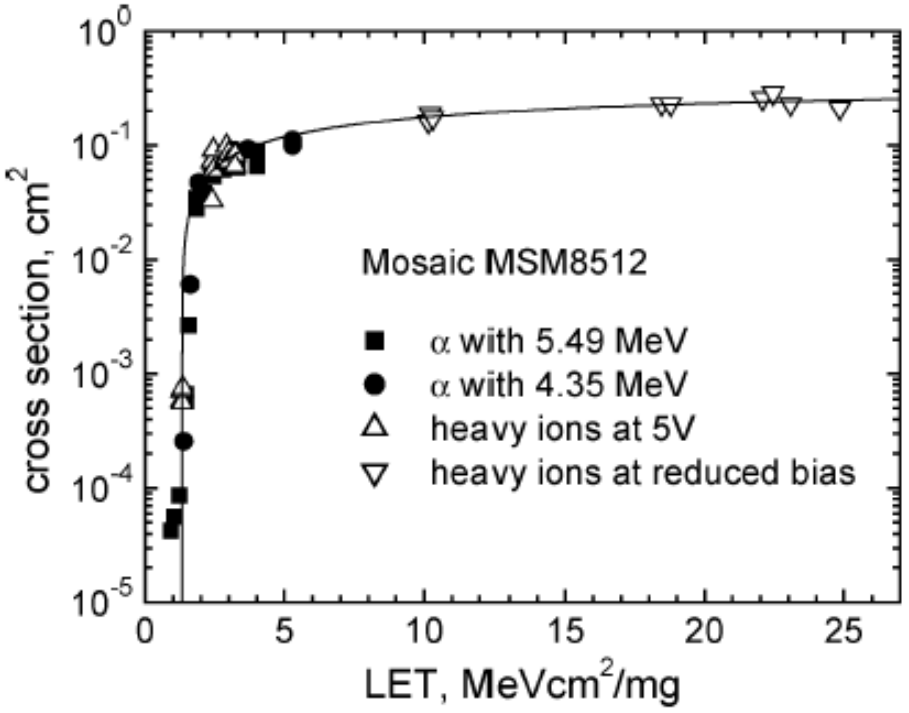
$$\sigma = \sigma_{sat} \cdot \left[1\text{-}e^{-\left(\frac{\text{LET-LET}_{th}}{W}\right)^{s}}\right]$$

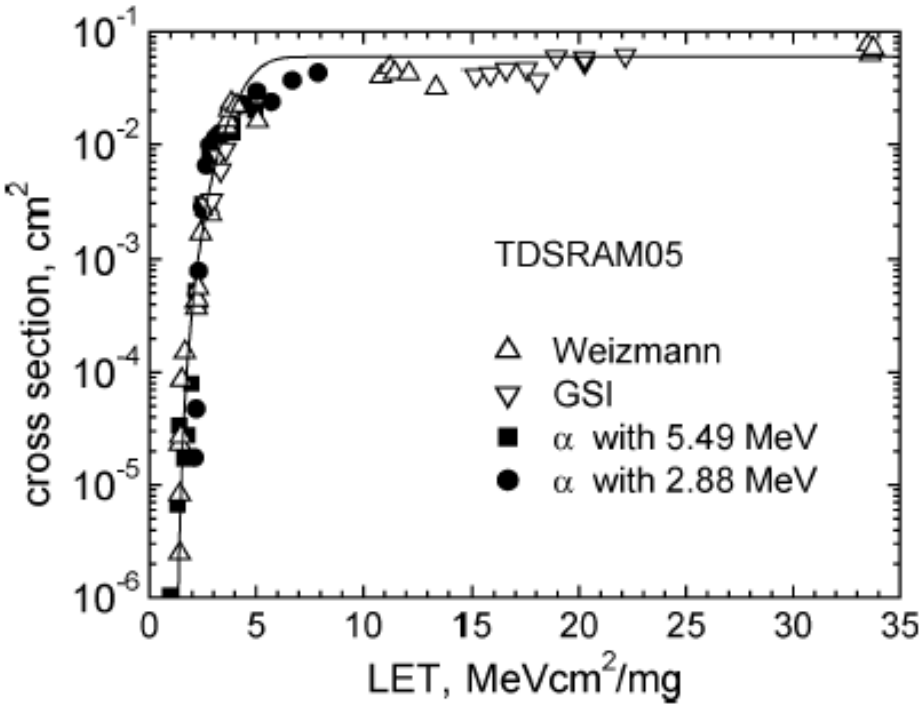
σ_{sat}=saturation σ

LET_{th}=threshold LET

W, s=fit parameters

SEE cross section vs LET curve





σ_{SEU} for MSM8512 SRAM vs LET:
- LET_{th}=1.32 MeV·cm/mg
- σ_{sat}=0.31 cm^2
- W=11.4 MeV·cm/mg
- s=0.65

σ_{SEU} for TDSRAM05 SRAM vs LET:
- LET_{th}=1.2 MeV·cm/mg
- σ_{sat}=0.06 cm^2
- W=3.5 MeV·cm/mg
- s=3.5

J. Barak et al., Use of Light-ion-Induced SEU in Devices Under Reduced Bias to Evaluate their Cross-Section, IEEE TNS., vol.51, n.6, Dec. 2004, pp. 3486-3493.

Threshold LET and threshold charge for SEE

- When LET ≤ LET_{th}, then $\sigma=0$
- σ_{sat} is the device area sensitive to the considered single event effect
- If the sensitive thickness d of the device is known and the impinging ion has a more or less constant LET along that thickness, a critical charge Q_{crit} can be defined for the considered SEE; in general

$$Q=\left(\frac{dQ}{dx}\right)\cdot d=\left(\frac{\frac{dE}{dx}}{E_{e/h}}\right)\cdot d\cdot q=\frac{LET\cdot\rho_{Si}}{E_{e\text{-}h}}\cdot d\cdot q$$

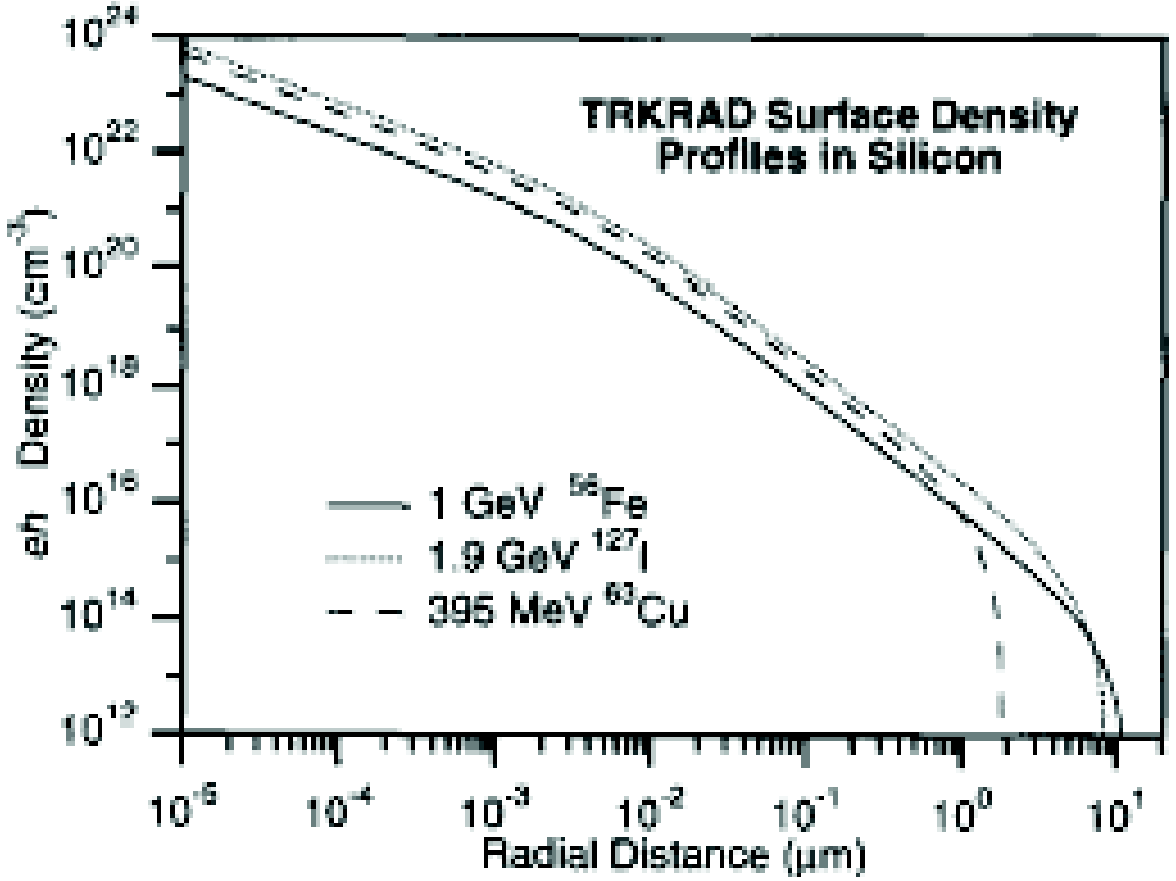
The critical charge will correspond to LET_{th}; so

$$Q_{crit}=\frac{LET_{th}\cdot\rho_{Si}}{E_{e\text{-}h}}\cdot d\cdot q$$

Fundamental SEE mechanisms

- Generally, reverse biased p-n junctions are the most SEE sensitive regions in an electronic device
- In the first approximation
  - if the impinging particle strikes the device in a region where an electric field is present (e.g., the depleted region of a p-n junction), the generated carriers are collected and a fast transient current is observed at the junction electrode
  - if the impinging particle strikes the device close to a reverse biased p-n junction, part of the generated carriers may diffuse towards the depleted region and be collected at the junction electrode, again resulting in a current transient
- The density of the generated charge is maximum very close to the particle track and decreases rapidly with the radial distance from it

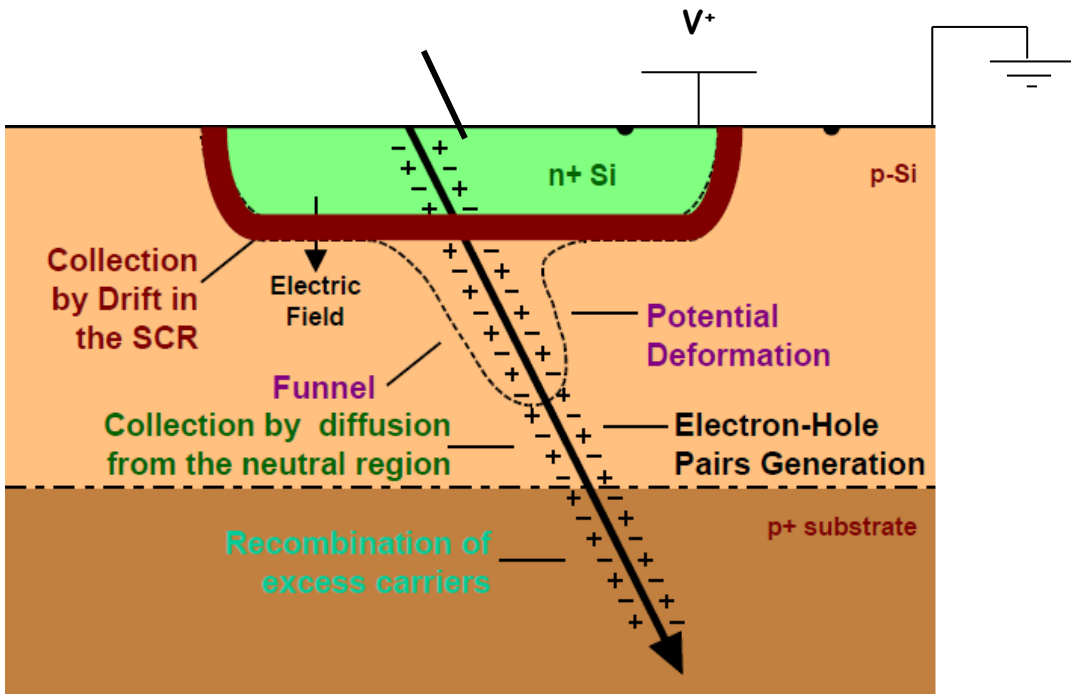
Fundamental SEE mechanisms

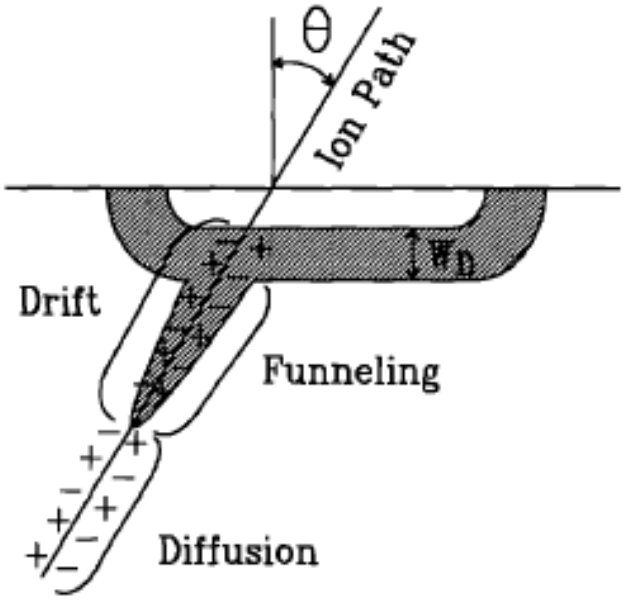


- Close to the ion track (0.1Å) , the e/h pair density may be in the order of 10^{23} - 10^{24} cm^{-3} (much larger than typical substrate doping concentration)
- Between 1 and 10 um from the ion track the density may fall down to 10^{12} – 10^{16} cm^{-3}

Funneling

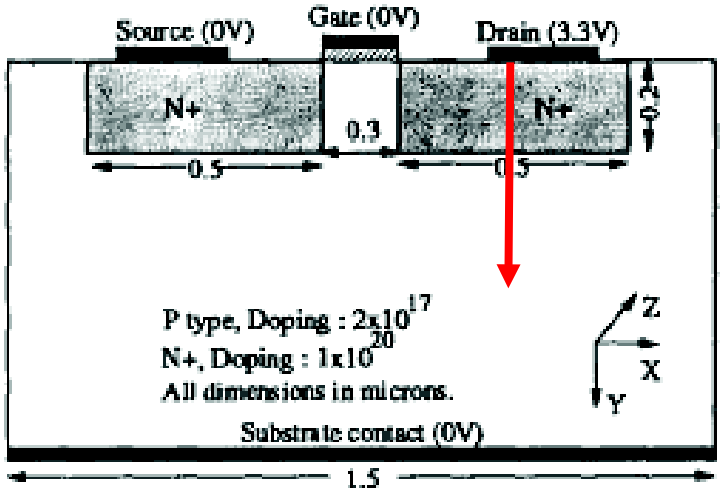
- The charge released by the impinging particle in an SEE event is collected through the so-called funneling mechanism; most of the charge is sucked in at the struck junction through a deformation of the junction potential, which extends into the substrate; the remaining charge diffuses in the substrate and may be collected or not at the same junction

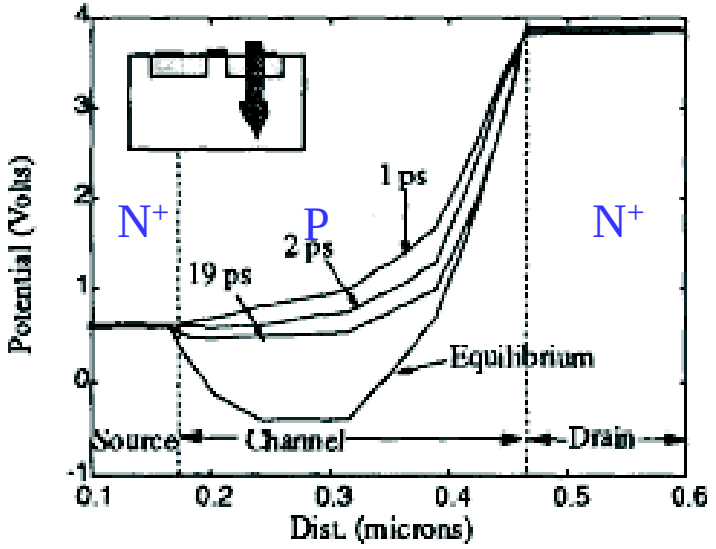




Ion triggered channeling in MOSFETs

- An ion impinging on a MOSFET in OFF state may alter the internal device field and create a conductive channel between the source and drain terminals ➔ ion triggered channeling





- Due to funneling, the potential barrier between source and drain collapses ➔ transient short circuit current

S. Velacheri, L. W. Massengill and S. E. Kerns, "Single-Event-Induced Charge Collection and Direct Channel Conduction in Submicron MOSFETS", IEEE TNS, vol. 41, n. 6, Dec. 1994, pp. 2103-2111.

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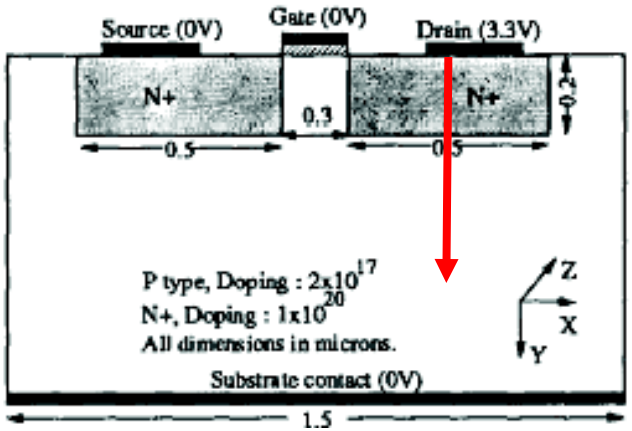
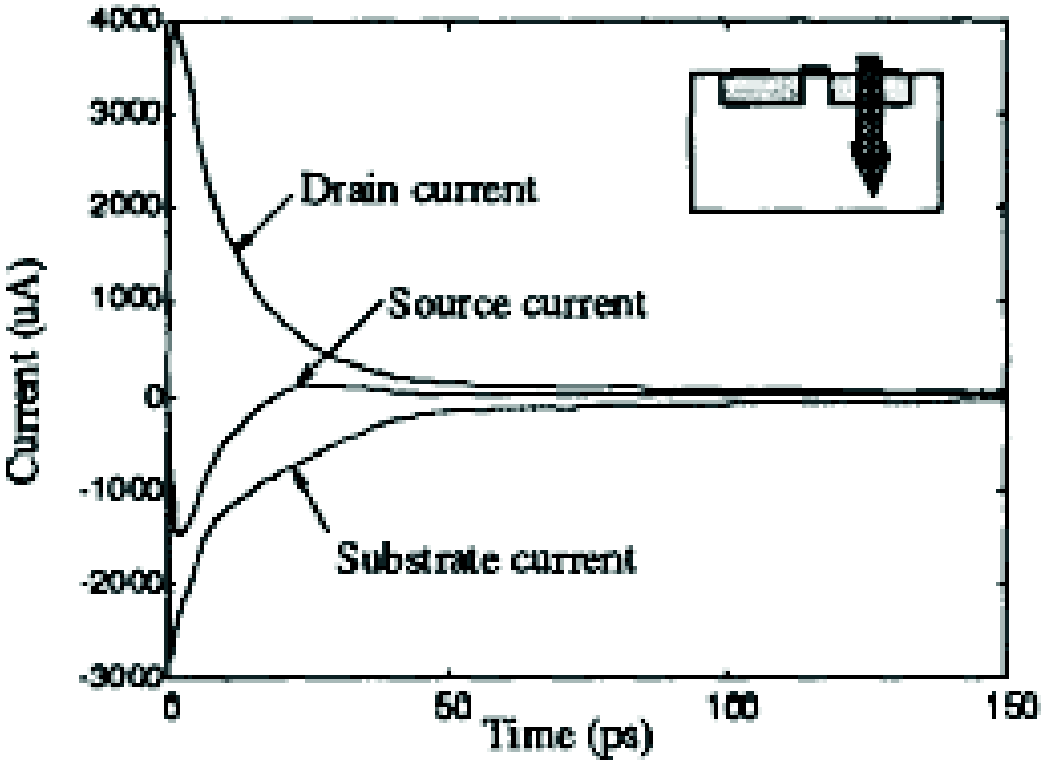


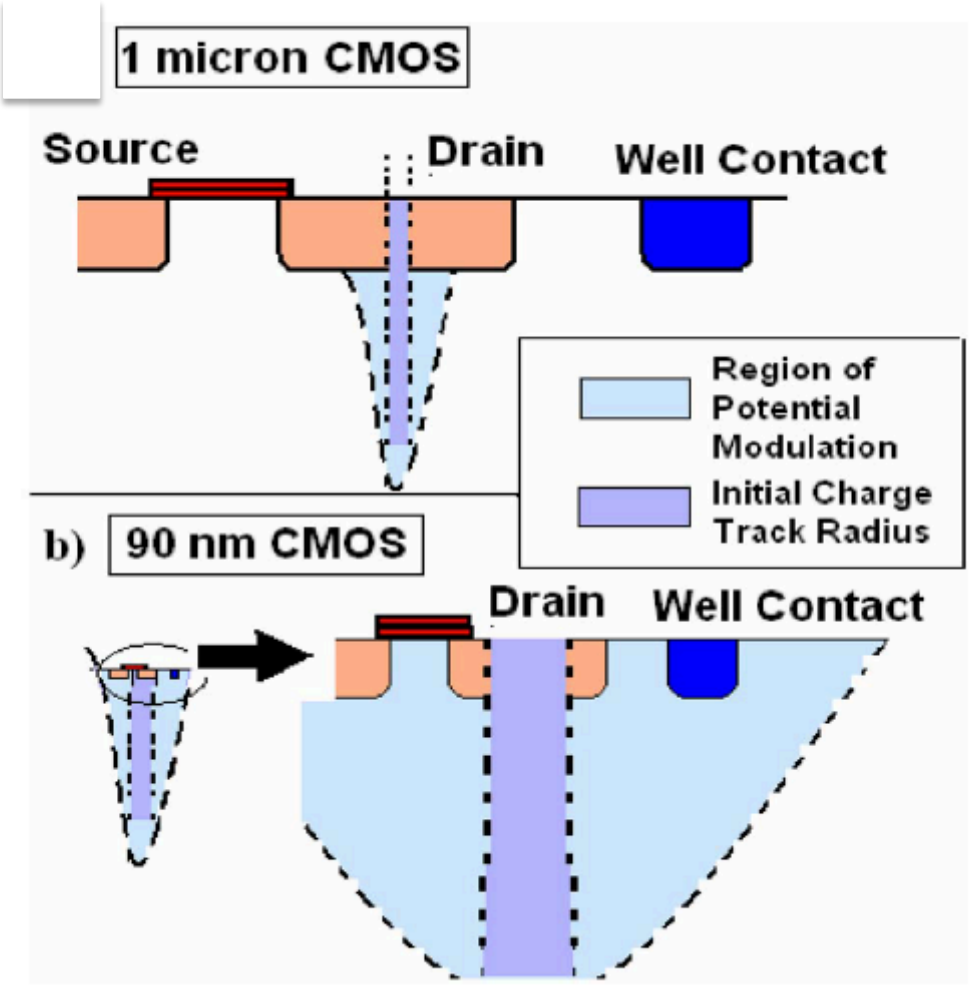


- current from the drain to the substrate (reverse biased junction)
- current from drain to source (potential barrier collapse)
- resulting current can discharge a floating drain node
- same effect if the particle strikes the device in the channel

- Potential barrier collapse takes place only in short channel devices; the effect is enhanced for larger incidence angles θ (effective LET=LET/cosθ)

Technology scaling effects

- MOSFET devices scale down with technology evolution, but funneling phenomena do not
- In advanced CMOS technologies, the perturbation of the potential due to an ion strike may cover source, drain and substrate contacts (or even more than a single transistor)



S. DasGupta et al., IEEE Trans. Nucl. Sci, vol.54, n. 6 Dec. 2007, "Effects of Well and Substrate Potential Modulation on Single Event Pulse Shape in Deep Submicron" CMOS.

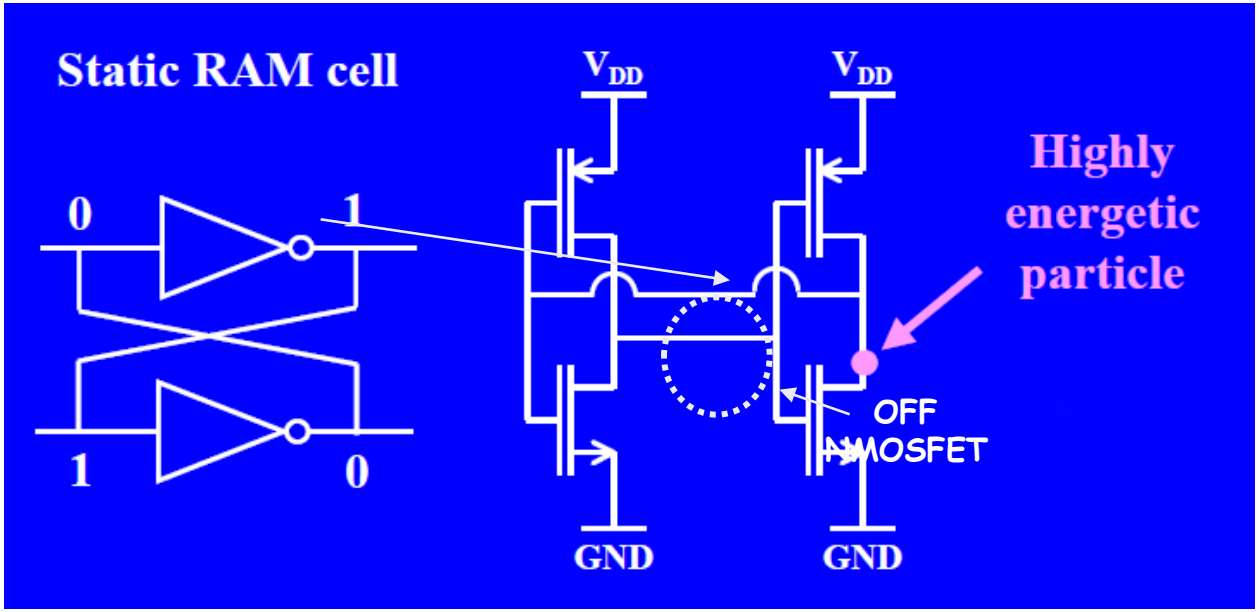
Single event upset (SEU)

- To cause disturbance in a circuit, the charge generated by a particle (a heavy ion) strike must be collected by a sensitive node
- Reverse biased p-n junctions are the most likely candidate to collect charge, since they feature a large depletion region and a strong electric field
- Single event upsets are soft, non-destructive errors consisting of the change in the state of a memory cell or register (bit-flips); they may appear as transient pulses in the logic and support circuitry

Single event upset (SEU)

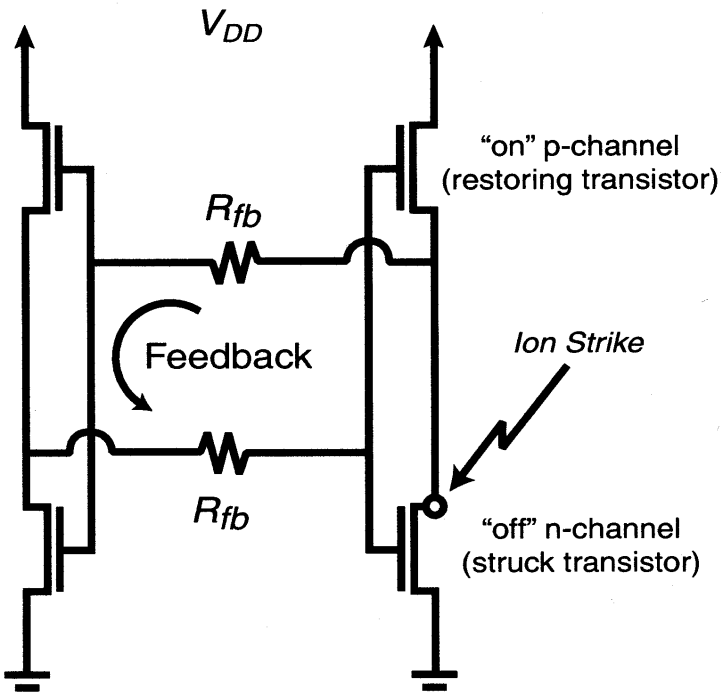
- In the case of a static RAM cell, the particle may strike the drain electrode of the OFF NMOSFET
  - the released charge is collected at the reverse-biased drain p-n junction
  - the current decreases the potential at the drain node, possibly below the cell switching voltage therefore changing the initial state

- The most sensitive part of a SRAM is represented by OFF devices
- NMOS transistors are more sensitive than PMOS



SEU: mitigation techniques

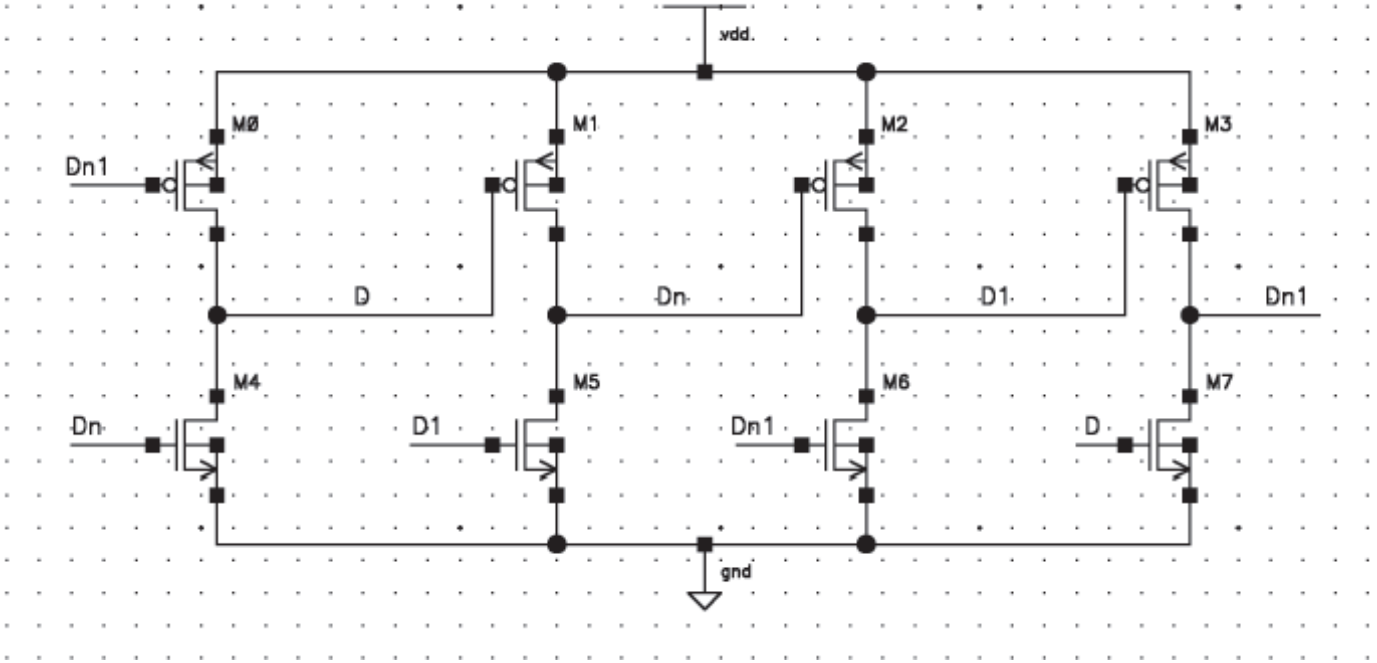
- Increase the threshold LET by increasing the size of the cell, i.e.,
  - increase the driving capability of the transistors, so that they are able to keep the initial cell state even after an ion strike
  - increase the parasitic capacitance at the sensitive nodes, so that voltage variation upon an ion strike are kept to a minimum
- Include resistors in the loop between the inverters in the cell, so that a delay is introduced in the feedback path
- These solutions go in the opposite direction with respect to the technology trend to miniaturization



SEU: mitigation techniques

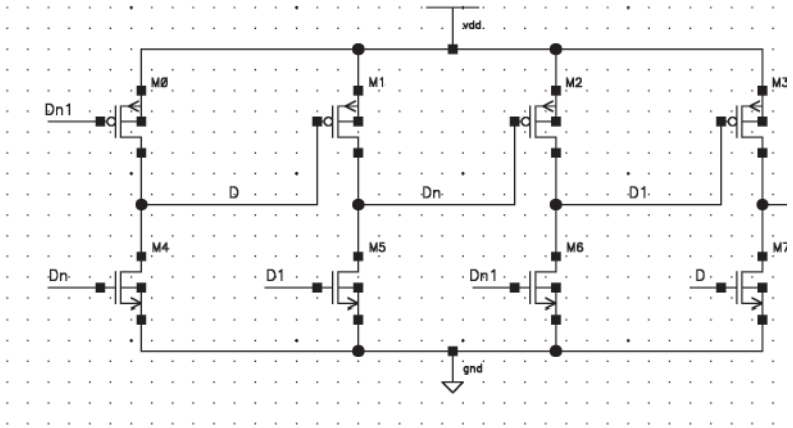
- A DICE (dual interlocked cell) takes advantage of circuit-level design techniques to prevent SEU

- a DICE contains duplicated data
- D and D1 are homologous nodes, as they (should) have the same logic value
- if upon an ion strike, only one of the two nodes changes state, then the cell does not exhibit SEU

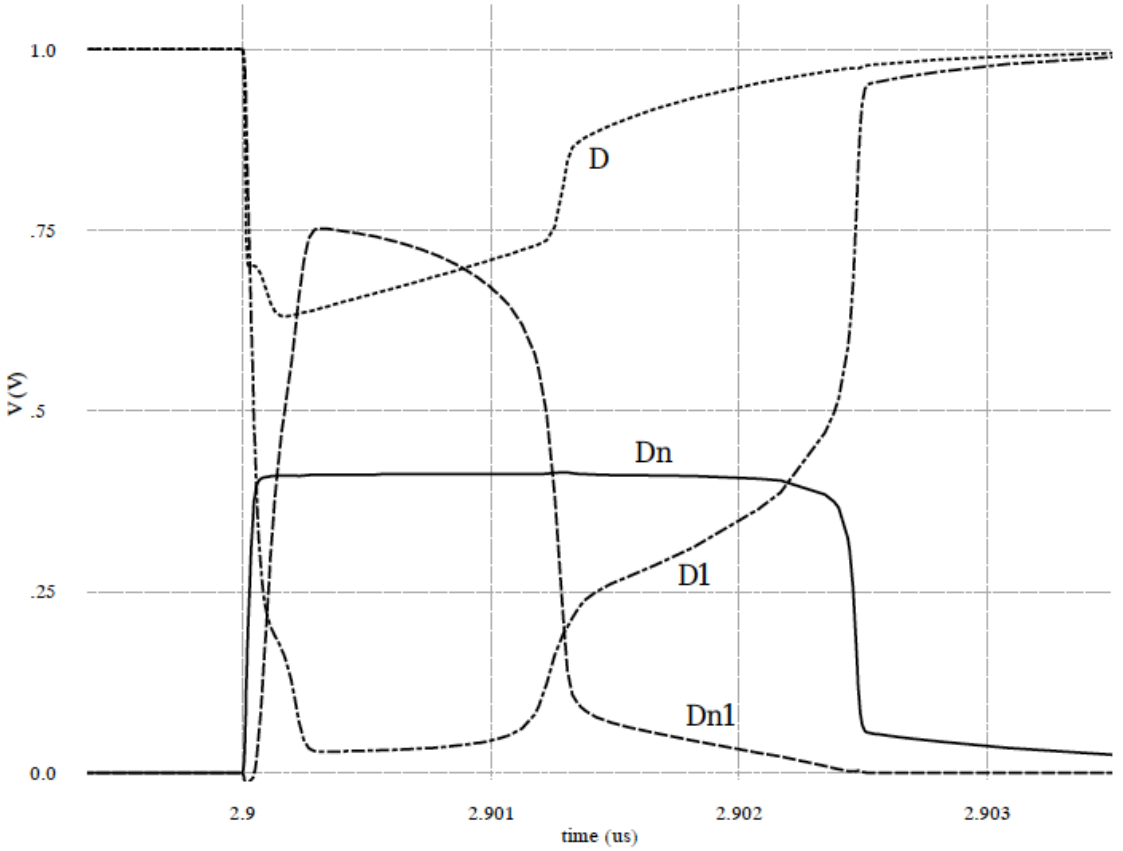


S. Shojaii, A. Stabile, V. Liberali, "A Radiation Hardened Static RAM for High-Energy Physics Experiments", PROC. 29th INTERNATIONAL CONFERENCE ON MICROELECTRONICS (MIEL 2014), BELGRADE, SERBIA, 12-14 MAY, 2014

SEU: mitigation techniques



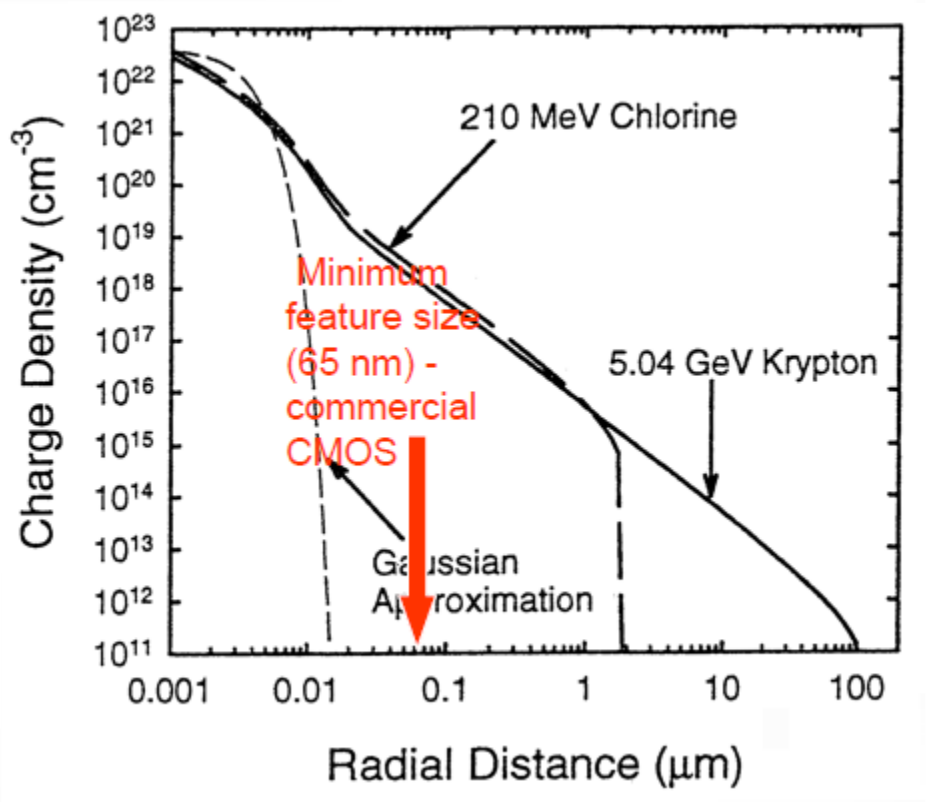
- PMOS and NMOS transistors in each branch are driven by different nodes
- PMOS M2 in the third branch is not switched OFF because Dn is not affects by the strike as Dn1



- Higher robustness can be achieved by physically separating homologous nodes of the single cell at enough distance to prevent a single particle to affect both of them ➔ interleave two or more cells

Multiple bit upset (MBU)

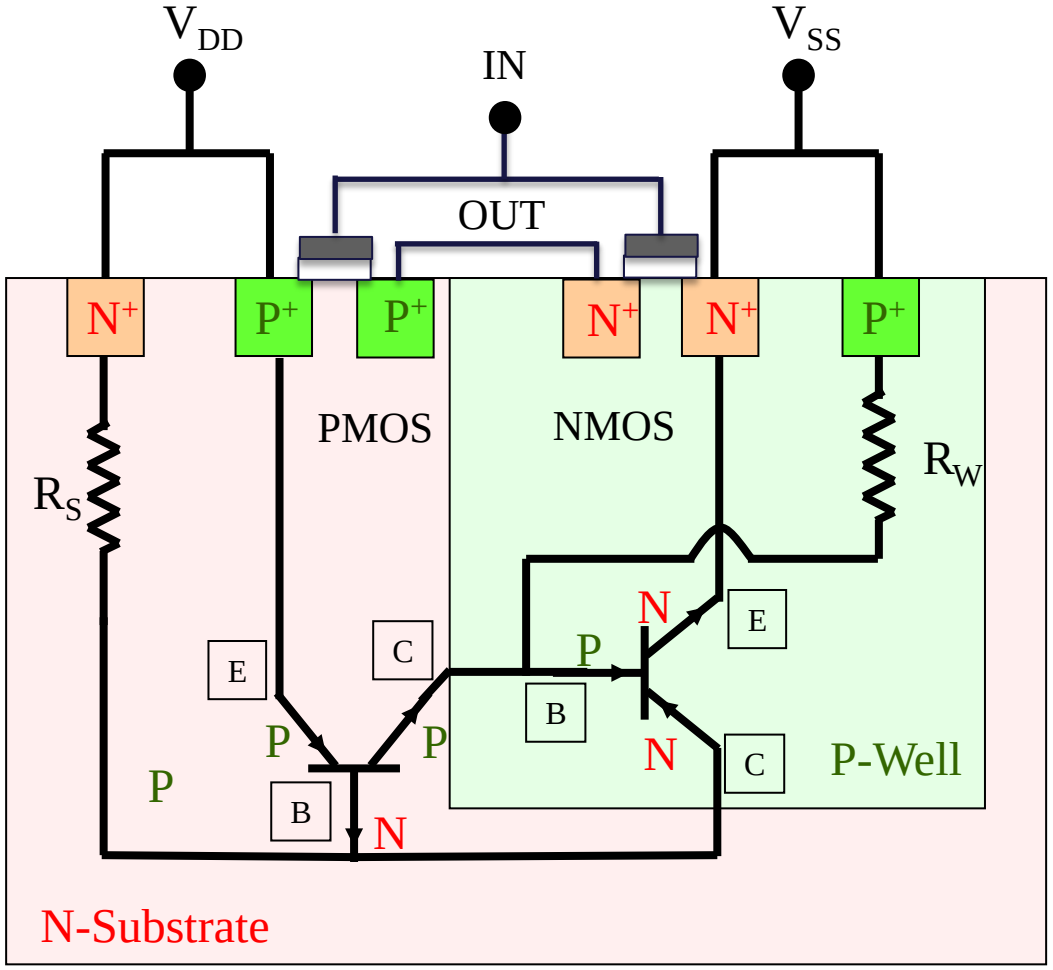
- Single event effects have become more complex to study as the feature size of CMOS processes (the minimum length that can be obtained by the lithography), has been scaled down to the submicron realm
- Indeed the size of the ion track has become comparable to the feature size of modern chips (see figure); therefore, phenomena that were confined to a single circuit node can now involve multiple nodes and charge sharing can occur
- The rate of occurrence of MBU phenomena is bound to rise as fabrication processes evolve

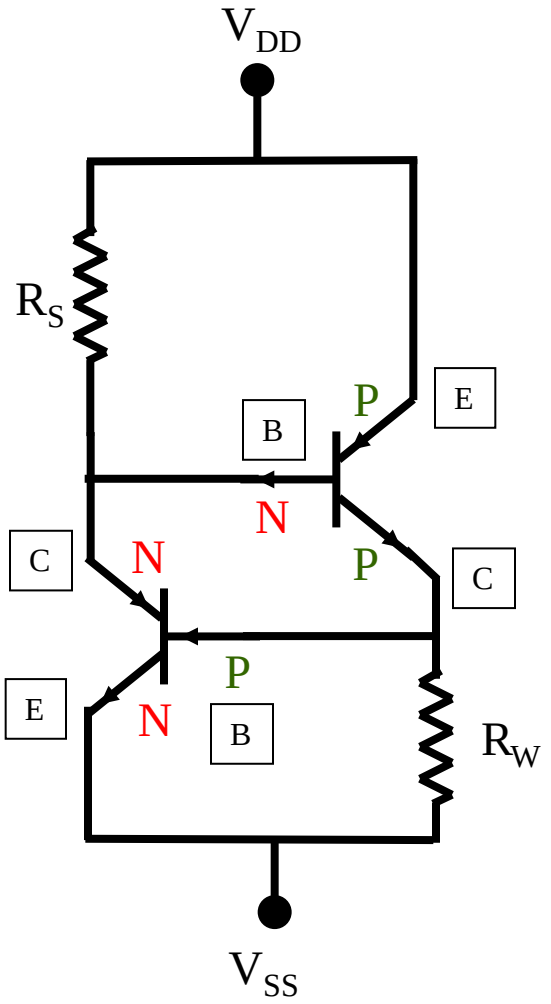


Charge density as a function of the distance from the center of the track for different ions

Radiation-induced latch-up

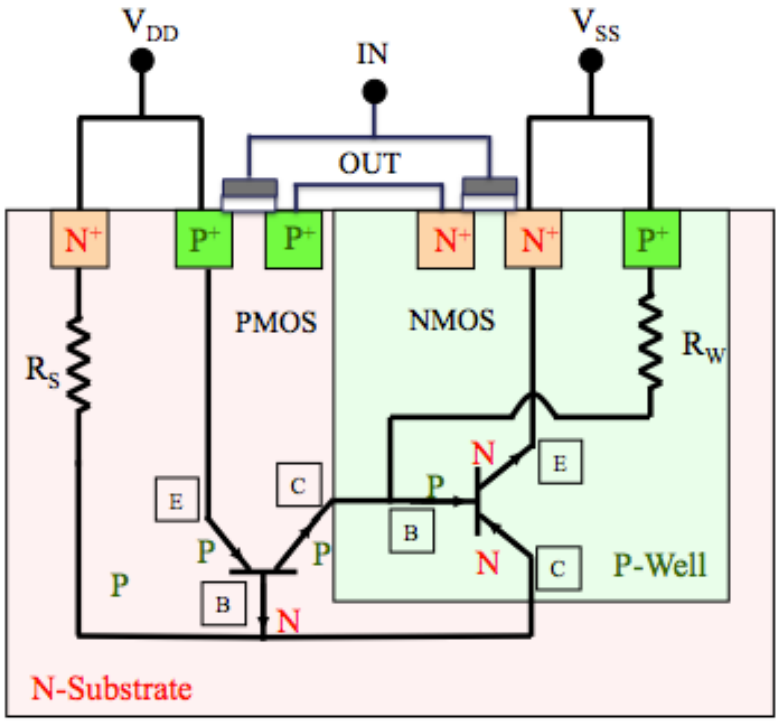
- Built in an inverter gate there are two parasitic bipolar transistors, an NPN and a PNP; they are cross-connected in such a way that the base-collector junctions are common, therefore forming an SCR (silicon-controlled rectifier)





Radiation-induced latch-up

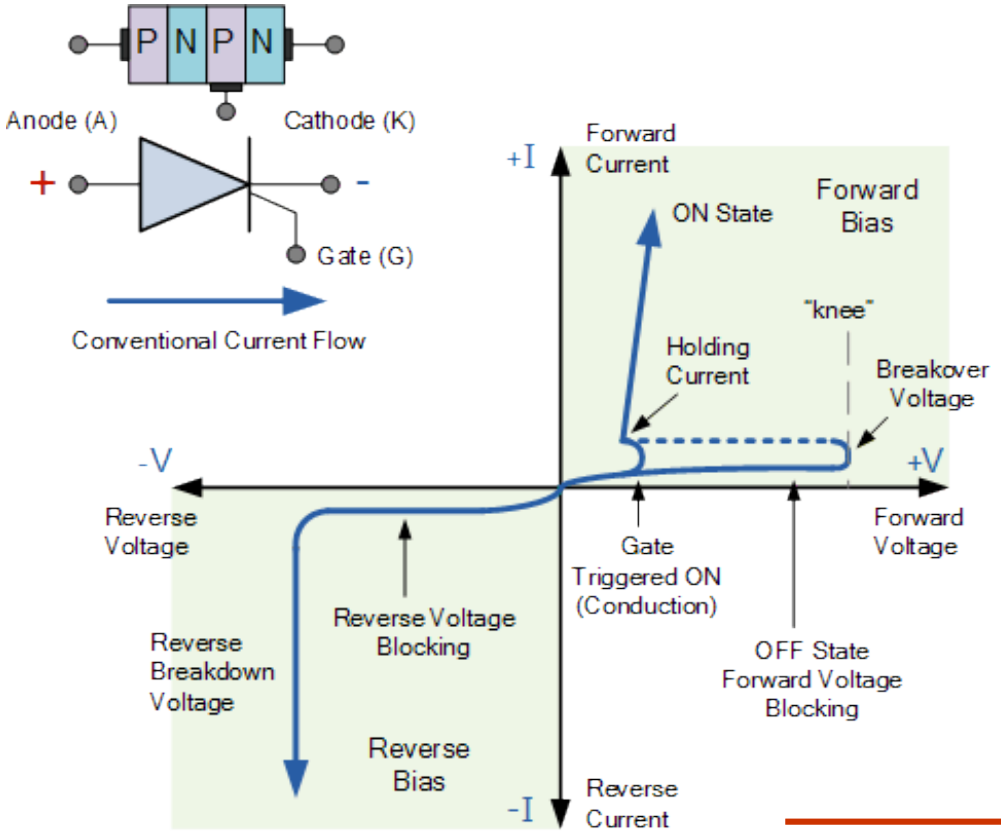
- During normal operation, the SCR is OFF (emitter and base in both BJTs are shorted ➔ both BJTs are in high impedance state)
- The collector of the first BJT is connected to the base of the second BJT and vice versa
- Under external excitation (electrical or radiation) one parasitic BJT may be forced into conduction activating the unstable loop condition.

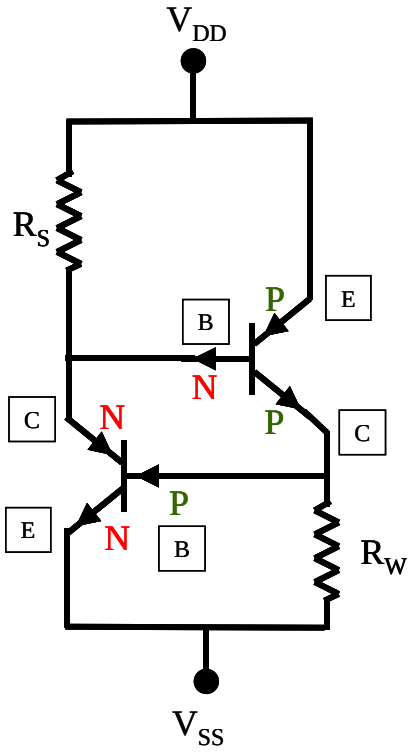


- A self-maintained low-impedance path is created between the supply terminal V_{DD} and V_{SS} that may be followed by a permanent thermal failure ➔ single event latch-up (SEL)
- If no protection mechanism has been implemented, the involved devices (and the circuit using them) may end up malfunctioning or even being destroyed due to overcurrent

Parasitic SCR operation

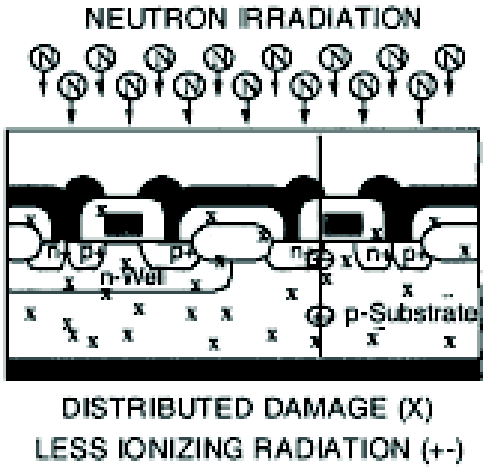
- Once the break-over voltage is exceeded, the device finds itself in the ON region
- If the operating point is such that I exceeds the holding current I_H and V is larger than the holding voltage V_H, then the latch-up condition is maintained
- To exit the latch-up condition, the current must be reduced below I_H, for instance by disconnecting the power supply

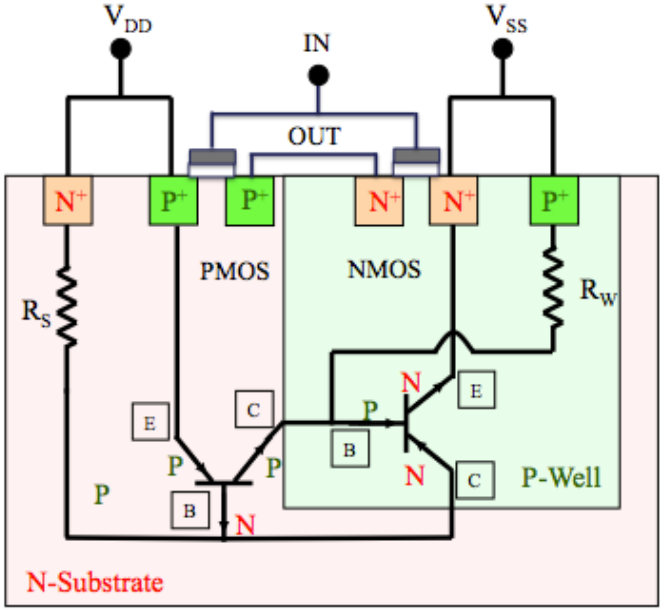




SEL mitigation techniques

- Reduce the gain current in the two parasitic BJTs in such a way that $\beta_{npn}\beta_{pnp}<1$; neutron irradiation of the substrate may actually result in a degradation of β in a bipolar transistor
- Minimize the spreading resistance in the well and in the substrate
- Instead of bulk CMOS, use a lightly doped epi-layer with heavily doped substrate

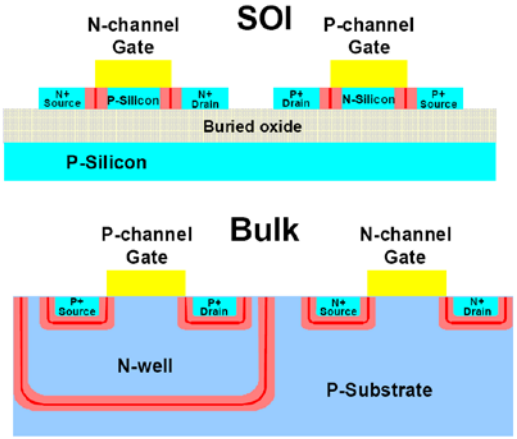


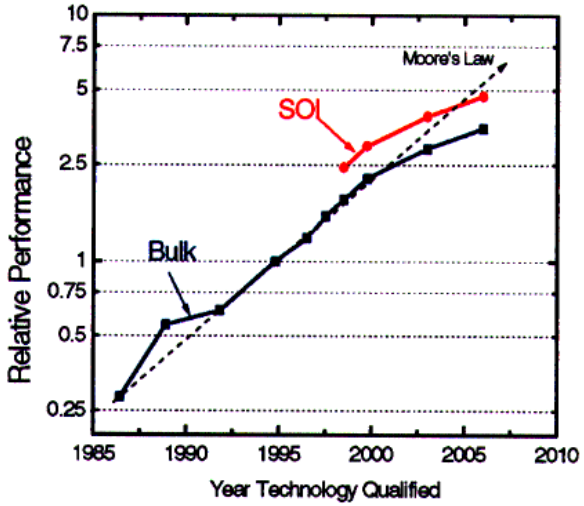


- Use deep N-wells (N^+ buried layers contacted through deep N^+ diffusions around the P-well) to reduce the pnp BJT gain
- Latch-up phenomena are expected to vanish for deep submicron CMOS, where VDD is around 1 V

Fully depleted SOI MOSFETs

- One of the limitations to processing speed in bulk CMOS transistors is given by the parasitic capacitance at the source/channel and drain/channel junctions
- This problem is overcome in the so-called SOI (silicon on insulator) CMOS technologies
  - In an SOI MOSFET, the device is fabricated in an ultra-thin (of the order of a few tens of nanometers) silicon layer on top of a thicker (several hundreds of nanometers) oxide layer (so-called buried oxide, or BOX)
  - In fully depleted (FD) SOI MOSFETs, the source and drain regions reach down to the buried oxide layer, reducing the parasitic capacitance, while the device region between source and drain, in normal operation, is fully depleted
- SOI technologies may provide high integration density, high speed and low power dissipation, and are widely used, for instance, in the design of microprocessor; their performance easily exceeds that of bulk CMOS

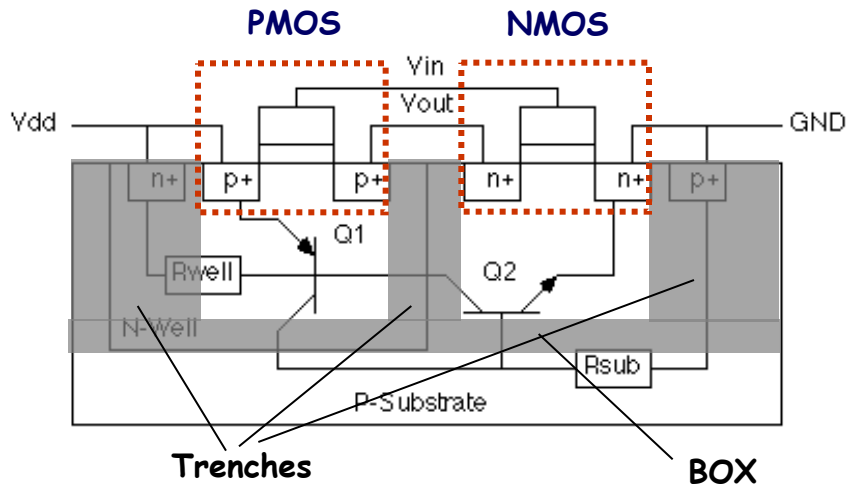




Relative performance of Bulk and SOI CMOS as a function of time (performance=1 for bulk CMOS process qualified in 1995)

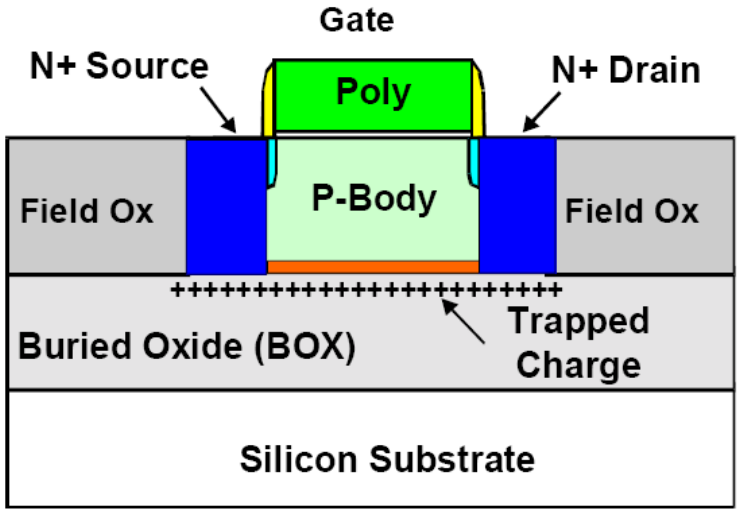
Radiation tolerance of FD SOI MOSFETs

- SOI technologies are inherently immune from latch-up effects (whether radiation-induced or not); P and N MOS parts in an SOI CMOS process are electrically isolated from each other by means of oxide trenches; therefore, no SCR, with its regenerative configuration, can be triggered by possible radiation-induced photocurrents
- SOI processes have in general the capability of reducing transient radiation-induced photocurrents and charge collection from the passage of a single ionizing particle



Radiation tolerance of FD SOI MOSFETs

- On the other hand, fully depleted SOI MOSFETs are more sensitive to total ionizing dose effects with respect to bulk CMOS transistors due to the presence of the buried oxide layer, where positive charge build-up can take place; accumulation of holes in the buried oxide may lead to
  - formation of a back-channel leakage path (a conductive path just in the silicon layer at the interface with the buried oxide); it depends on the quality of the back silicon/BOX interface and on the initial threshold voltage of the parasitic transistor between source and drain
  - threshold voltage shift due to electrical coupling between the front (actual) gate terminal and the back (parasitic) gate terminal (recall that the device silicon layer is extremely thin)



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