HV-CMOS Pixel Detector

Giovanni Darbo – INFN / Genova

24th February 2015

VI Scuola Nazionale "Rivelatori ed Elettronica per Fisica delle Alte Energie, Astrofisica, Applicazioni Spaziali e Fisica Medica

WEB link:

- *http://sirad.pd.infn.it/scuola_legnaro/ScuolaNazionaleLNL2015_ProgrammaPreliminare.pdf*

Outline

Requirements from experiments

Hybrid, Monolithic, HV-CMOS

- Noise, depletion width, resistivity, mobility
- Sideward depletion, DEPFET, MAPS, HV-CMOS

CCPD

HV/HR-CMOS & CCPD Chips

Technology implementation

Experimental results

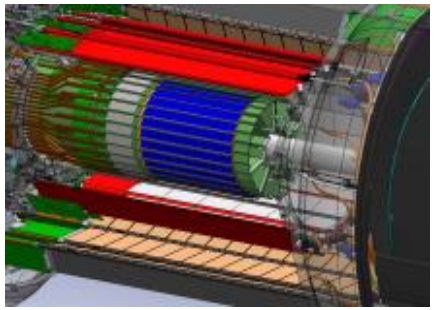
Conclusions

Reeferences

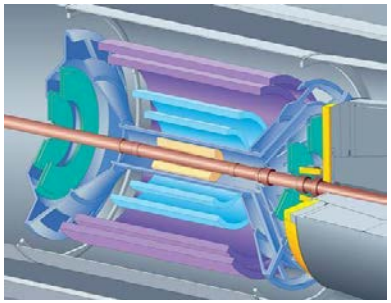
REQUIREMENTS FROM EXPERIMENTS

Collider Experiments – Some Parameters

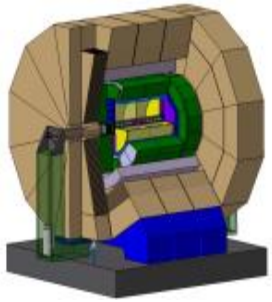
STAR at RICH



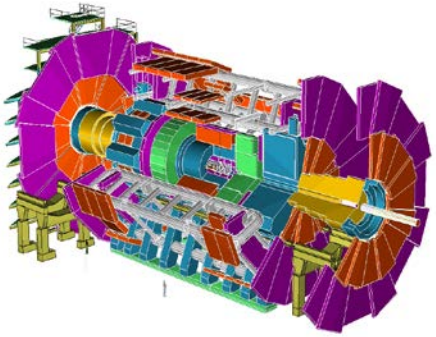
ALICE-LHC



ILC



ATLAS



Requirements for inner pixel layers

	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	25	25
Particle Rate [kHz/mm^2]	100	15	250	1 000	10 000
Fluence [n_{eq}/cm^2]	10^{12}	10^{13}	10^{12}	$1x10^{15}$	$2x10^{16}$
Ion. Dose [Mrad]	0.3	0.7	0.4	80	1000

Collider Experiments – Requirement Implications

Timing:

- *Long timing between events*
- *Charge can be collected in 0.1 ÷ 10 ms: collection by diffusion*
- *Slow shaping time, low power*
- *All events can be R/O, simpler trigger / readout architecture*

Requirements for inner pixel layers

	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	**200 000**	**20 000**	**350**	**25**	**25**
Particle Rate [kHz/mm^2]	100	15	250	1 000	10 000
Fluence [n_{eq}/cm^2]	10^{12}	10^{13}	10^{12}	$1x10^{15}$	$2x10^{16}$
Ion. Dose [Mrad]	0.3	0.7	0.4	80	1000

Collider Experiments – Requirement Implications

Timing:

- *Short timing between – high time resolution to timestamp events*
- *Fast charge collection: charge collected by drift*
- *Local memory inside the pixels, high traffic in the chip*

Requirements for inner pixel layers

	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	25	25
Particle Rate [kHz/mm^2]	100	15	250	1 000	10 000
Fluence [n_{eq}/cm^2]	10^{12}	10^{13}	10^{12}	$1x10^{15}$	$2x10^{16}$
Ion. Dose [Mrad]	0.3	0.7	0.4	80	1000

Collider Experiments – Requirement Implications

Particle rate:

- *Low pixel occupancy: no dead time from charge collection / amply shaping*
- *Simpler R/O architecture – for ex. rolling shutter*

Requirements for inner pixel layers

	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	25	25
Particle Rate [kHz/mm^2]	100	15	250	1 000	10 000
Fluence [n_{eq}/cm^2]	10^{12}	10^{13}	10^{12}	$1x10^{15}$	$2x10^{16}$
Ion. Dose [Mrad]	0.3	0.7	0.4	80	1000

Collider Experiments – Requirement Implications

Particle rate:

- *High pixel occupancy: need fast charge collection / shaping*
- *Not all hit can be transferred out of the chip: trigger, buffering and traffic inside the chip are highly demanding.*

Requirements for inner pixel layers

	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	25	25
Particle Rate [kHz/mm^2]	**100**	**15**	**250**	**1 000**	**10 000**
Fluence [n_{eq}/cm^2]	10^{12}	10^{13}	10^{12}	$1x10^{15}$	$2x10^{16}$
Ion. Dose [Mrad]	0.3	0.7	0.4	80	1000

Collider Experiments – Requirement Implications

NIEL and TID:

- *Silicon bulk damage (NIEL) is limited: charge trapping (minority carrier lifetime) does not strongly affect collection by diffusion*
- *Total ionizing dose (TID) has limited impact on electronics (V_{th} shift due to charge trapping in oxide): deep submicron and annular gate design are not mandatory*

Requirements for inner pixel layers

	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	25	25
Particle Rate [kHz/mm^2]	100	15	250	1 000	10 000
Fluence [n_{eq}/cm^2]	10^{12}	10^{13}	10^{12}	$1x10^{15}$	$2x10^{16}$
Ion. Dose [Mrad]	0.3	0.7	0.4	80	1000

Collider Experiments – Requirement Implications

NIEL and TID:

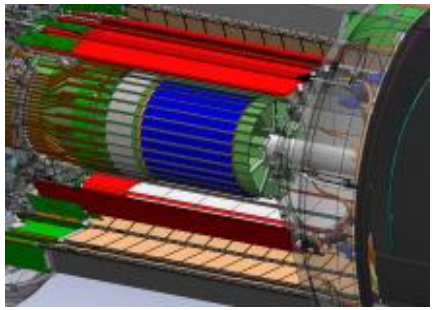
- *Charge collection by diffusion is not possible due to trapping, need E-field to move charge fast.*
- *Deep Sub-Micron (DSM) technology for high dose (TID) requirements:*
  - Gate oxide < 3.5 nm; minimum CMOS transistor feature <0.25 µm

Requirements for inner pixel layers

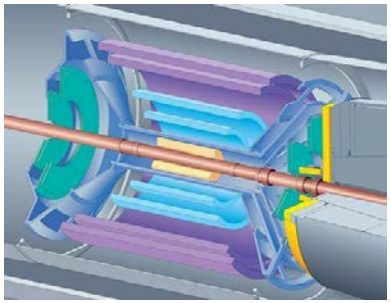
	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	25	25
Particle Rate [kHz/mm^2]	100	15	250	1 000	10 000
Fluence [n_{eq}/cm^2]	**10^{12}**	**10^{13}**	**10^{12}**	**$1x10^{15}$**	**$2x10^{16}$**
Ion. Dose [Mrad]	**0.3**	**0.7**	**0.4**	**80**	**1000**

Pixel Detector Technologies

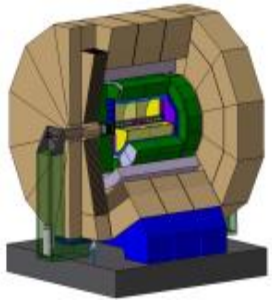
STAR at RICH



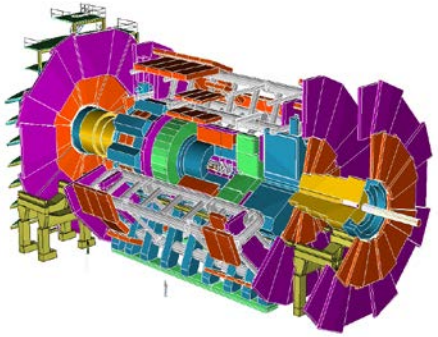
ALICE-LHC



ILC



ATLAS



Requirements for inner pixel layers

	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	25	25
Particle Rate [kHz/mm^2]	100	10	250	1000	10 000
Fluence [n_{eq}/cm^2]	10^{12}	10^{13}	10^{12}	$1x10^{15}$	$2x10^{16}$
Ion. Dose [Mrad]	0.3	0.7	0.4	80	1000

MAPS

Hybrid

?

HV-CMOS

The path to HV-CMOS, HV/HR-CMOS, CCPD

HYBRID, MONOLITHIC, CCPD

Hybrid Pixel Detector

Hybrid pixels

- Signal is collected by drift
- n-type (fig) or p-type detectors
- Every pixel connected to one channel

Origin

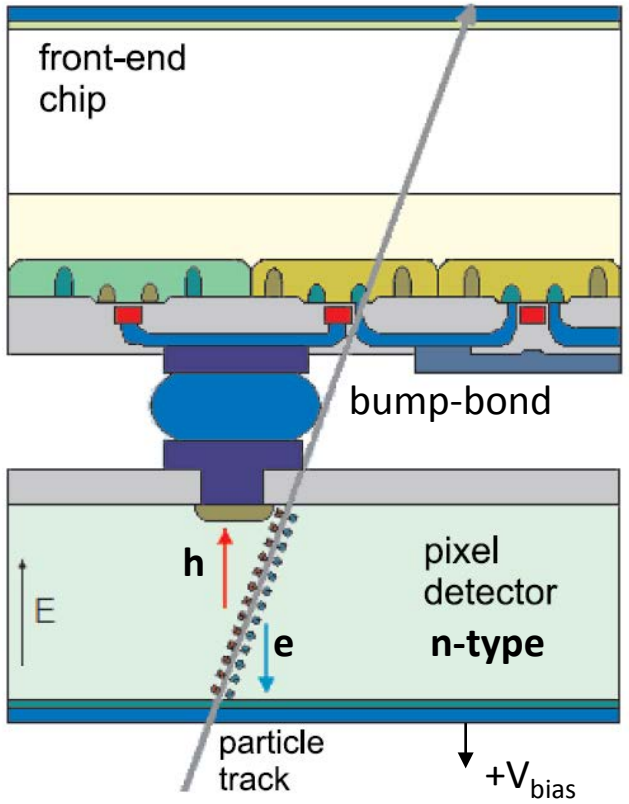
- Birth tracked back to IEEE-NSS 1984
- Fixed target: CERN WA84 – early 1990^{ths}
- At colliders: LEP – DELPHI – 1996 (installed)

Advantages

- Sensor and electronics use best materials and technologies
- Collected charge (signal) defined by sensor thickness
- Usually fully depleted sensors
- Radiation hardness profits of sensor and electronics best options

Disadvantages

- Costly interconnection between sensor and electronics (bump-bonding) process
- Material: sensor usually 200÷250 µm, electronics 100÷200 µm
- Spatial resolution: sensor thickness and pixel size

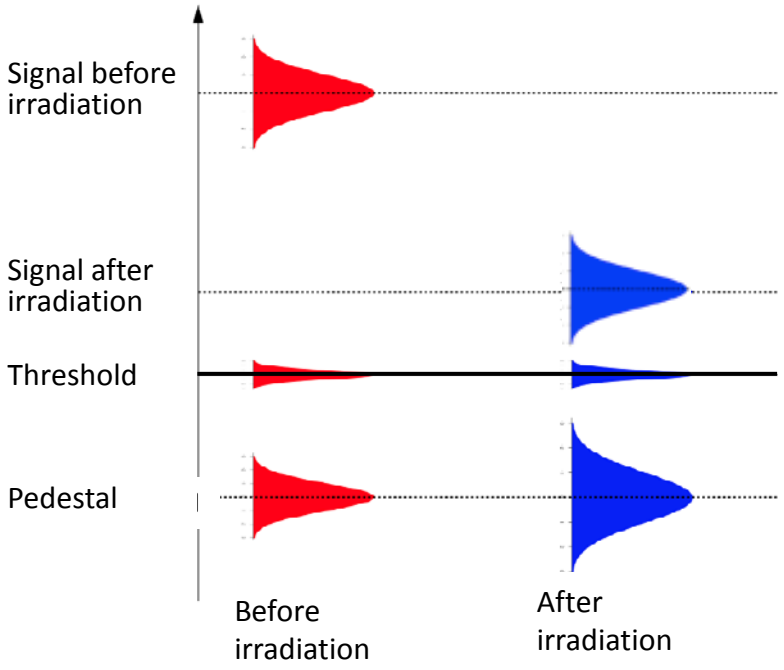


© T. Hemperek, Bonn, DE

Pixel Detector: Design Parameters

Parameters to consider

- Preamplifier noise
  - Pedestal + signal
- Input signal: charge
  - Wrt to ENC → depletion width
- Threshold
  - Uniformity → single pix tune
- Radiation
  - Reduction of charge → signal
  - I_{leak} increase → noise
  - Effect on electronics: noise increase & amplifier gain reduction



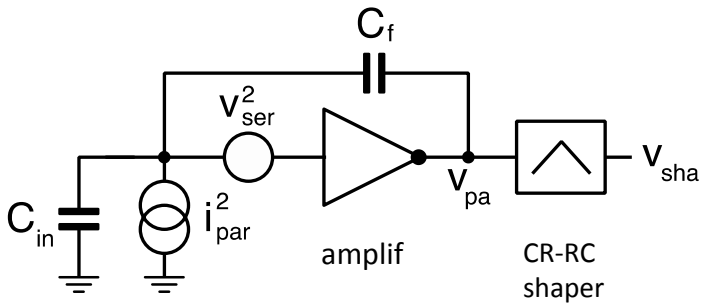
Charge Amplifier - Noise Analysis 1/3

Noise analysis [ref. a,b] for a pixel amplifier with RC-CR shaper and MOS input

- Charge-sensitive preamplifier and shaper with input noise sources and capacitive input load
- Simplified analysis [ref. a] gives:

$$ENC^2 = \frac{e^2}{4q^2}\left(\frac{\tau}{2} I_0 + \frac{1}{2\tau} V_0 C_{in}^2 + 2 V_{-1} C_{in}^2\right)$$

- **ENC:** equivalent noise charge, i.e. the signal charge that yields a signal-to-noise ratio of one (S/N = 1).
- **q** = 1.602 × 10^{-19} C ; **e** = 2.718 ; **τ** : time constant of RC and CR filter (assumed the same) ; $\mathbf{C_{in}}$: total input capacitance (C_{det} + C_{amp})
- Noise sources:
  - $\mathbf{I_0}$: from detector leakage current
  - $\mathbf{V_0}$: From transistor channel noise
  - $\mathbf{V_{-1}}$: From 1/f excess flicker noise



Charge Amplifier - Noise Analysis 2/3

- Replacing noise sources:

$$I_0 = 2qI_{leak}$$ from detector leakage current

$$V_0 = \frac{8}{3}\frac{kT}{g_m}$$ from transistor channel noise

$$V_{-1} = \frac{K_f}{C_{OX}WL}$$ from 1/f excess flicker noise

- For a typical 250 nm technology, with $\mathbf{C_{OX}}$ = 0.4 fF/µm^2; $\mathbf{K_f}$ = 33 x 10^{-25} J and a typical NMOS input device with length **L** = 0.5 µm and width **W** = 20 µm, the ENC becomes [ref.2]:

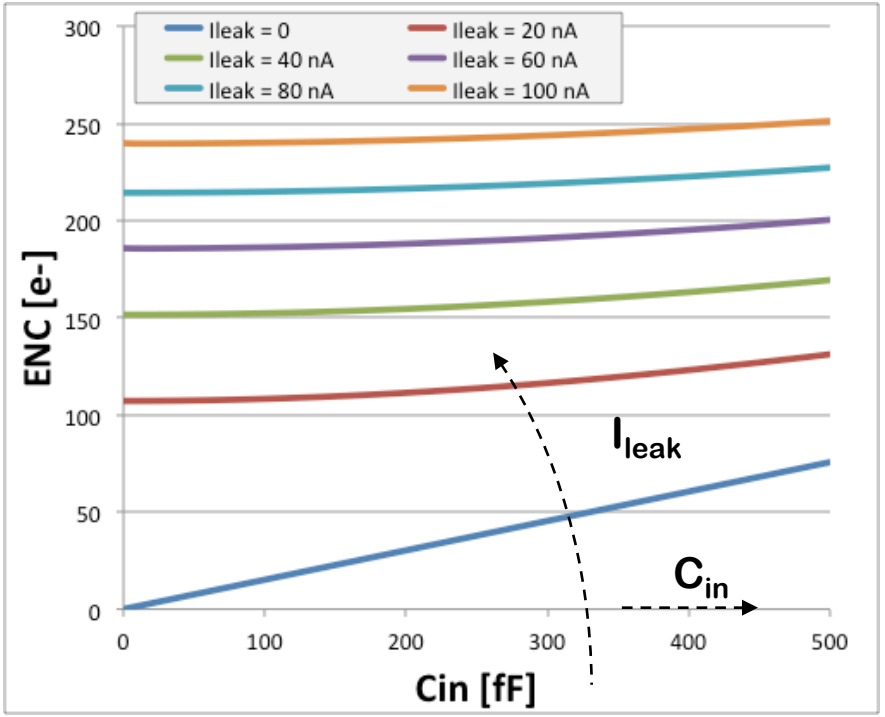
$$\left(\frac{ENC}{e^-}\right)^2 = 115\frac{\tau}{10ns}\frac{I_{leak}}{1nA} + 388\frac{10ns}{\tau}\frac{mS}{g_m}\left(\frac{C_{in}}{100\,fF}\right)^2 + 74\left(\frac{C_{in}}{100\,fF}\right)^2$$

Charge Amplifier - Noise Analysis 3/3

Typical values:

- τ = 50 ns ; C_{in} = 100 ÷ 300 fF ; I_{leak} = 1 ÷ 100 nA (before/after heavy irradiation) ; g_m = 0.5 nS
- Term (2) is dominant for typical detector capacitance (200 nF) and leakage current of 1 nA.
- With increasing shaping time (τ) the current noise (1) increases and voltage white noise (2) decreases,while 1/f voltage noise is independent of shaping time.

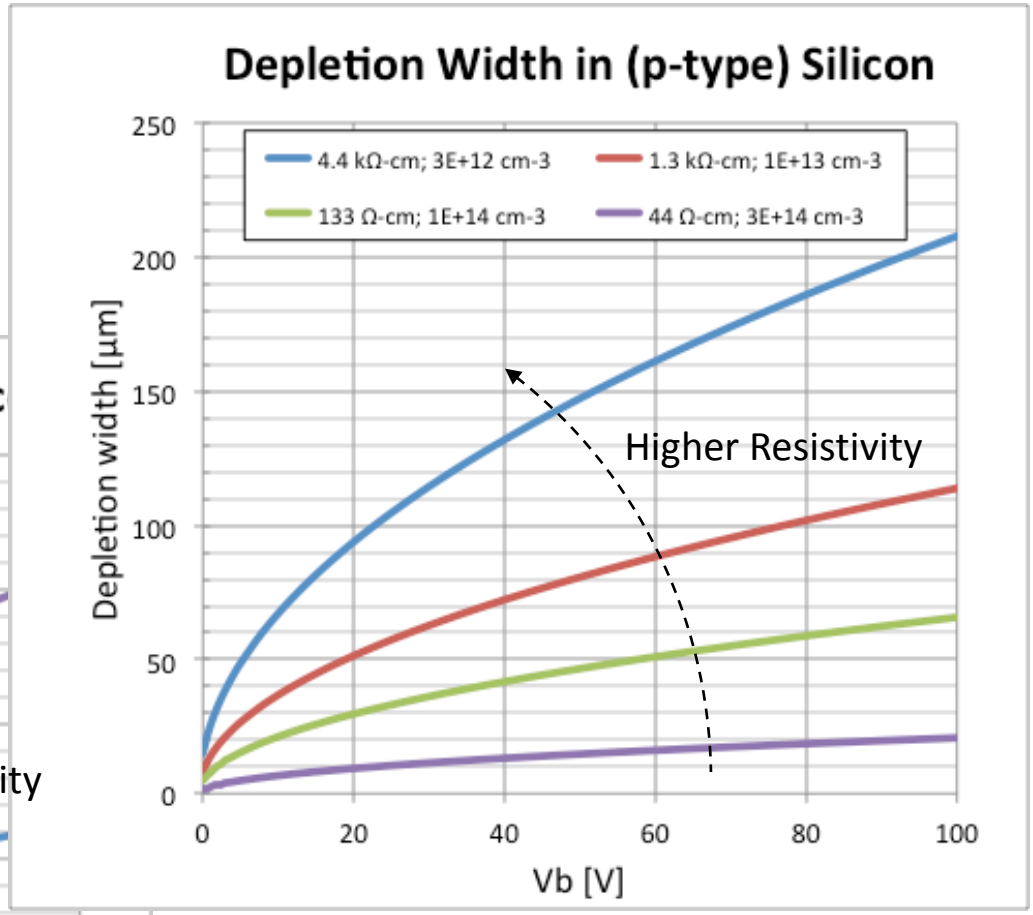
ENC vs C_{in} and I_{leak}

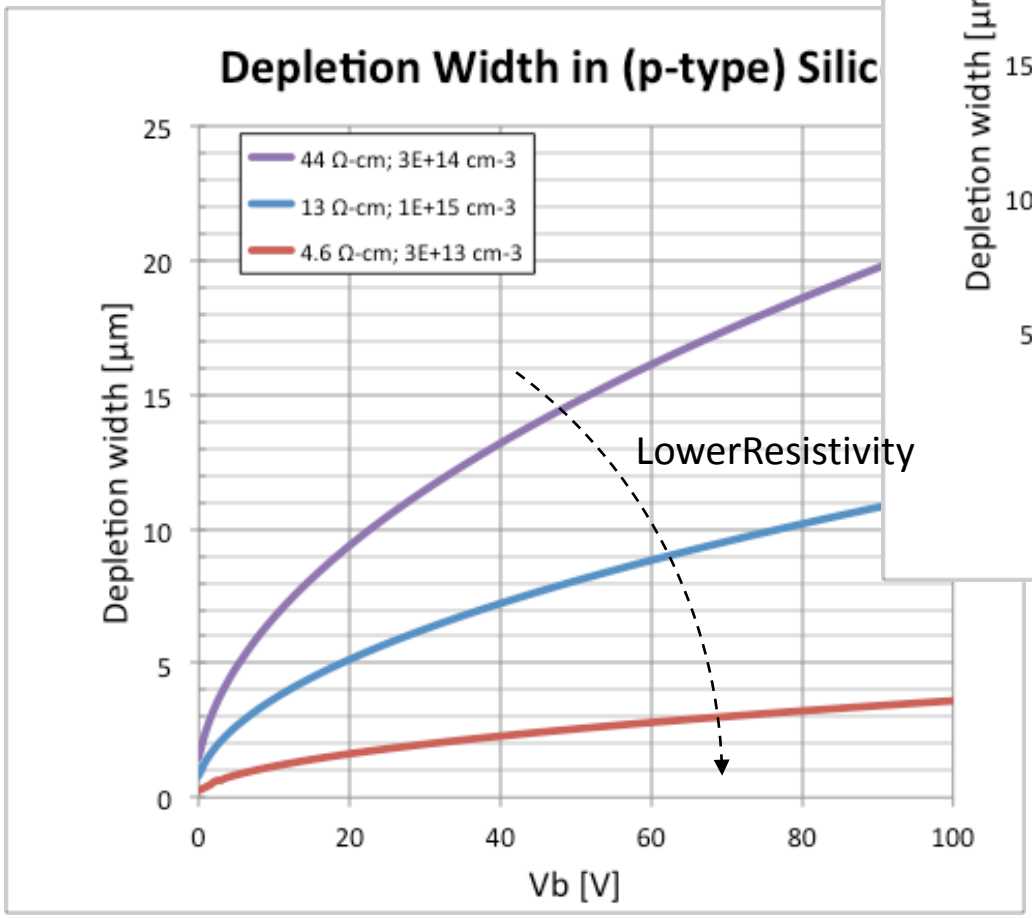


$$\left(\frac{ENC}{e^-}\right)^2 = \textcircled{1}\ 115\frac{\tau}{10ns}\frac{I_{leak}}{1nA} + \textcircled{2}\ 388\frac{10ns}{\tau}\frac{mS}{g_m}\left(\frac{C_{in}}{100\,fF}\right)^2 + \textcircled{3}\ 74\left(\frac{C_{in}}{100\,fF}\right)^2$$

Depletion Width (w_d)

$$w_d = \sqrt{\frac{2\varepsilon(V_b + V_{bi})}{eN}} \approx \sqrt{\frac{2\varepsilon V_b}{eN}}$$





w_d [m]: *depletion width*

V_{bi} [V]: *Voltage built-in (typ. 0.5 V)*

V_b [V]: *Voltage bias*

N [cm^{-3}]: *Impurity concentration (N_a for p-type and N_d for n-type)*

Resistivity

Resistivity (ρ_p, ρ_n) is given by

- for p-type:

$$\rho_p = (q\mu_p N_a)^{-1}$$

- and n-type

$$\rho_n = (q\mu_n N_d)^{-1}$$

Where:

μ_p, μ_n *[$cm^2\ v^{-1}s^{-1}$]:*

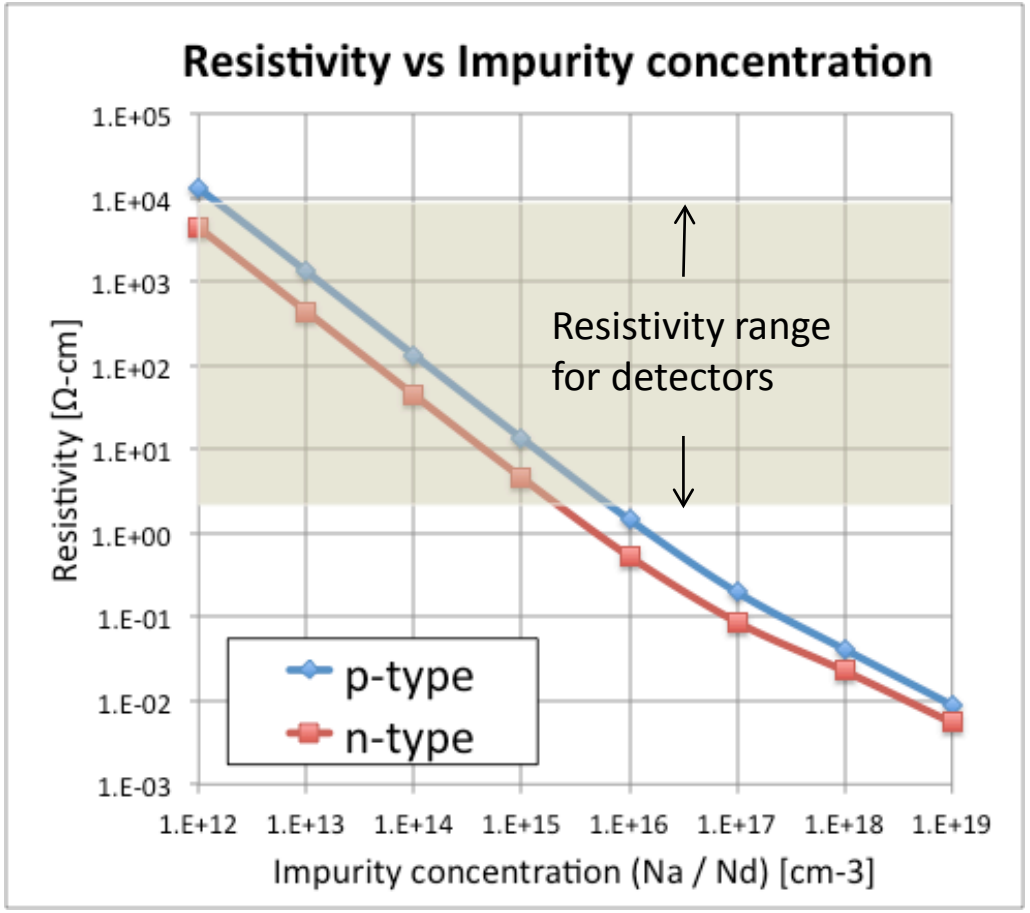
- *hole/electron motilities*
- *$\mu_p \approx 470$, $\mu_n \approx 1400$*

N_a, N_d *[cm^{-3}]:*

- *acceptor/donor concentration*

q *[C] unitary charge*

- *$q = 1.602 \times 10^{-19}$ C*



h/e Mobility vs Dopant Concentration

Resistivity (ρ_p, ρ_n) is given by

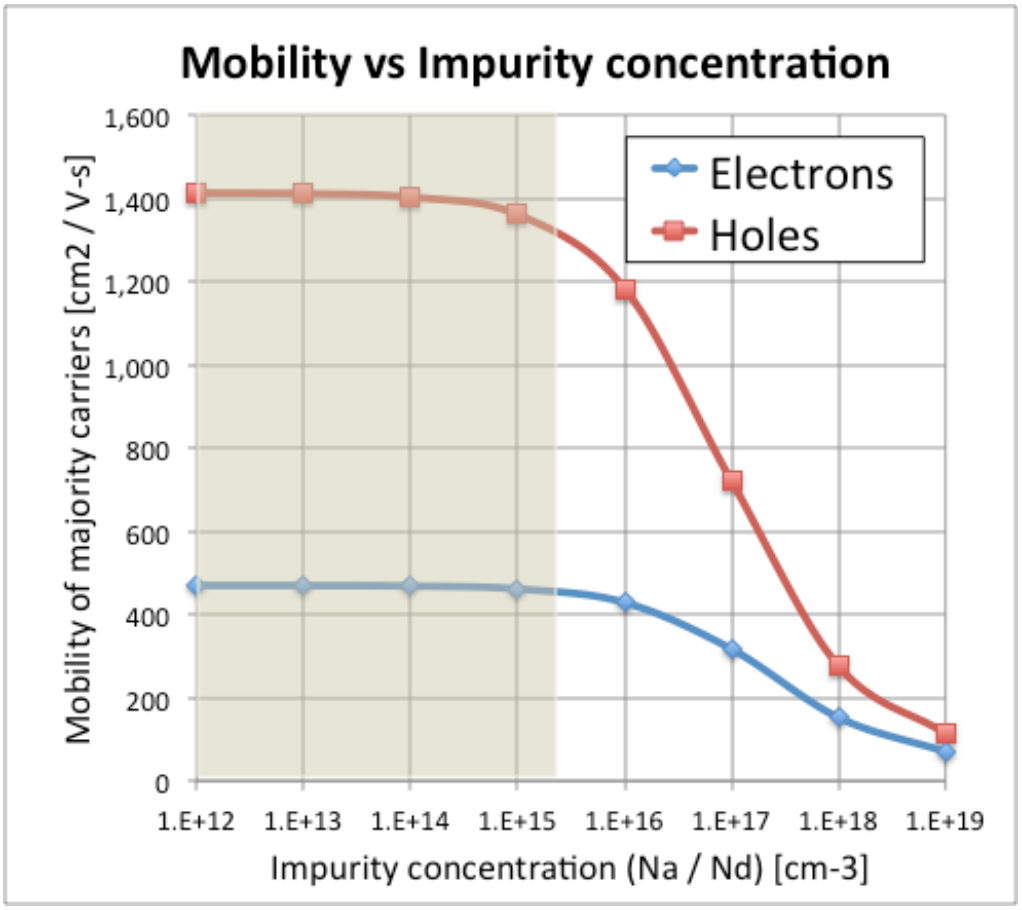
for p-type:

$$\mu_p = \frac{\rho_p}{qN_a}$$

and n-type:

$$\mu_p = \frac{\rho_p}{qN_a}$$

With the same notation as in the previous slides



Monolithic Pixel Detectors

Sideward depletion

- Charge confined by potentials generated by doping concentration
- Silicon drift chamber is one example

DEPFET (Depleted FET)

- Monolithic pixel integrating charge amplification and R/O on detector substrate

MAPS (CMOS active pixels)

- Use standard CMOS technology for pixel detector

Advantages

- Low noise, low power, low material budget, small pixels

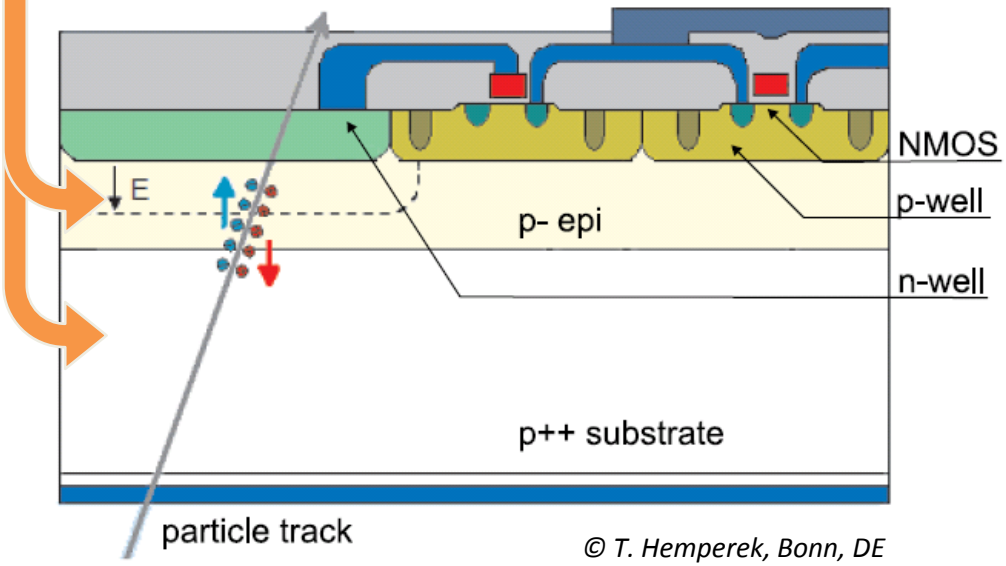
Disavantages

- Limited radiation hard, slow timing, R/O architecture

Origin

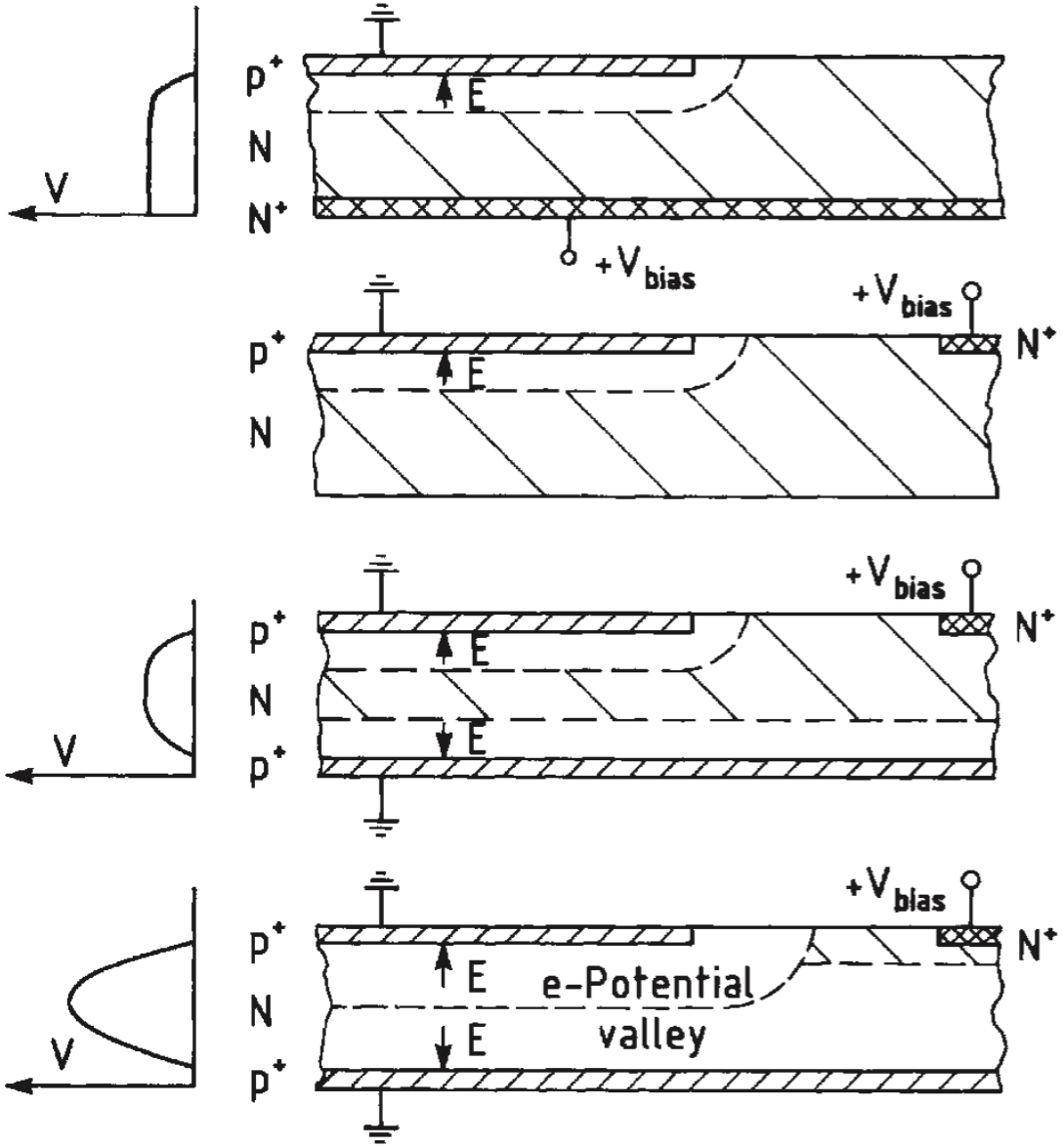
- Sideward depletion – E. Gatti & P.Rehak, 1984 [Ref.1]
- DEPFET – J.Kemmer & G. Lutz, 1987 [Ref.2]
- MAPS (CMOS) – R. Turchetta et al., 2001 [Ref.3]

$$\Delta V = \frac{kT}{q} \ln\left(\frac{N_{p++}}{N_{p-}}\right)$$



© T. Hemperek, Bonn, DE

Sideward Depletion



© G. Lutz [ref. c]

Standard Pixel Detector

- Depletion by back bias

Sideward detector

- Depletion from side bias

Double side junction

- Moderate side bias
- Partially depleted detector

- Increase side bias to fully deplete
- Valley for electrons created by positive potential

DEPFET

Sideward depletion when

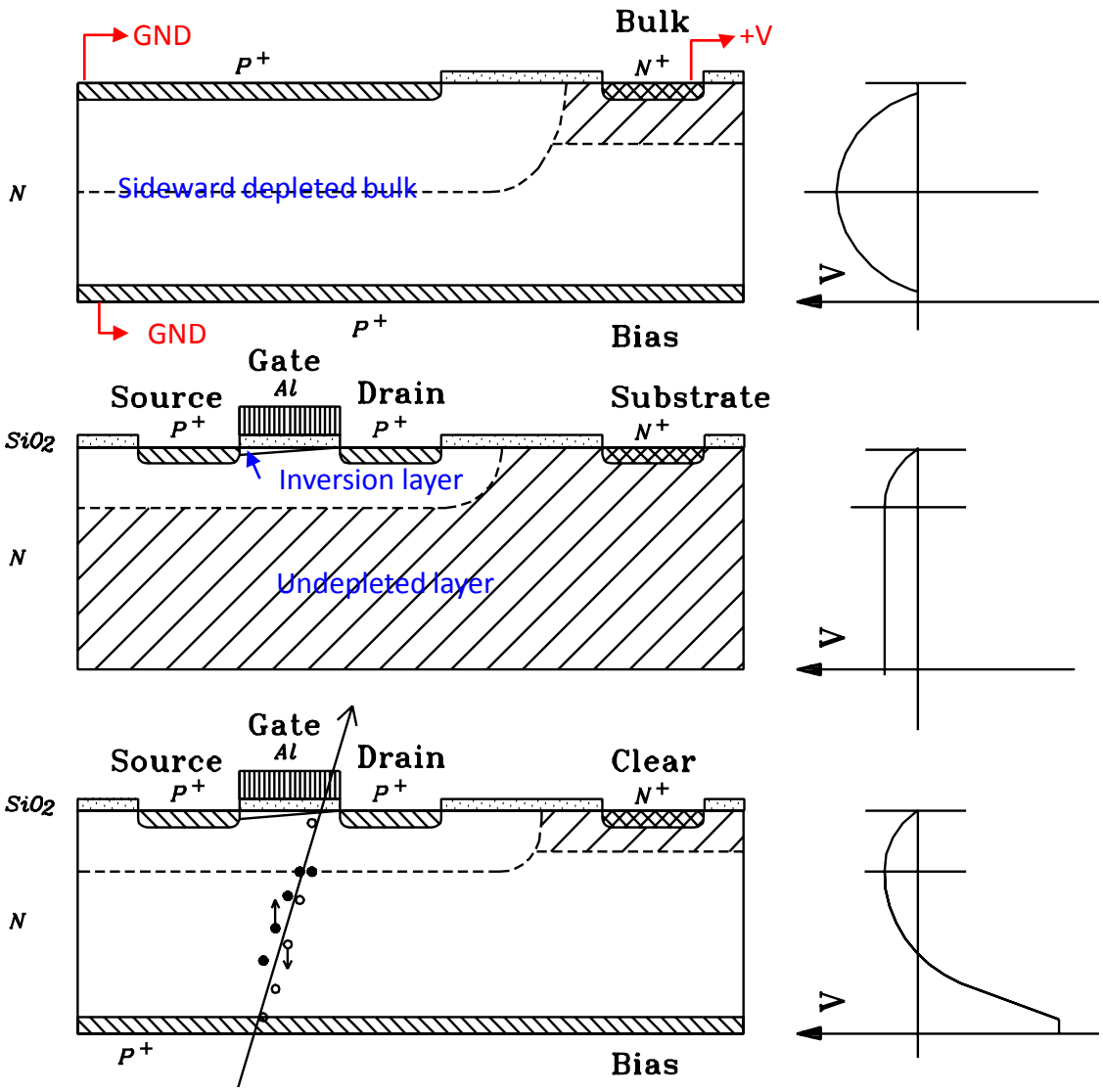
- diodes are located on both sides of a wafer
- substrate contact, located on the side, is polarized in the reverse bias direction with respect to the large-area diode junction
- A potential minimum for majority carriers (electrons in n-type silicon) forms between the two diode junctions.

MOS transistor

- A standard MOS enhancement-type transistor built on top of the bulk
- Conductivity of the channel steered not only by the gate voltage but also by the bulk potential.

DEPFET detector

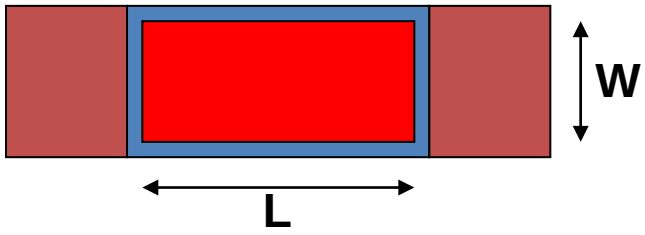
- Bias applied on back side – minimum valley moves toward FET channel
- Holes moves toward back side
- Electrons toward the potential valley
- Mirrored charge in the FET gate open the channel and current flows.
- Positive signal applied to Clear electrode moves away electrons from valley and close the FET channel

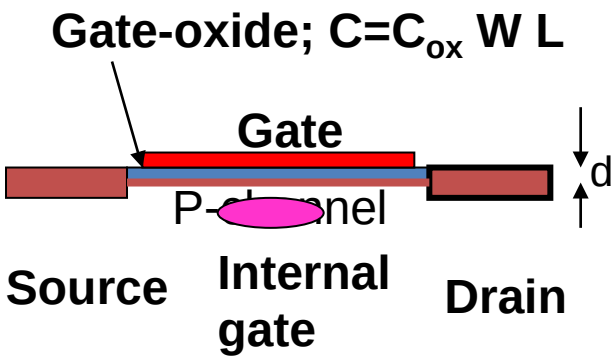


© L.Rossi et al. [ref. b]

How does a DEPFET Work?

© N.Wermes, 9th "Trento" Workshop, Genova 2014





A charge q in the internal gate induces a **mirror charge** αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage:

$\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$

which in turn **changes the transistor current I_D .**

FET in saturation:

$$I_D = \frac{W}{2L}\mu C_{OX}\left(V_G + \frac{\alpha q_s}{C_{OX}WL} - V_T\right)^2$$

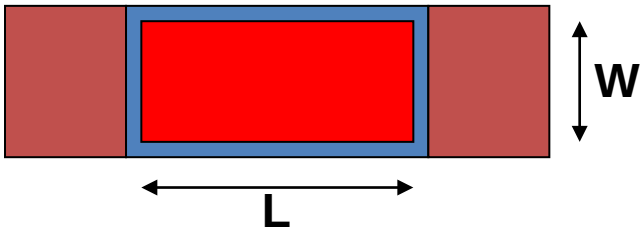
I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

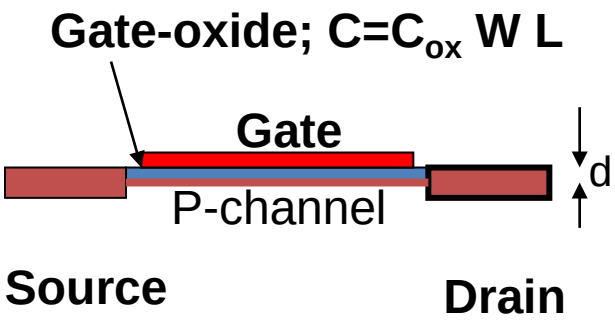
Conversion factor:

$$g_q = \frac{dI_D}{dq_S} = \frac{\alpha\mu}{L^2}\left(V_G + \frac{\alpha q_s}{C_{OX}WL} - V_{th}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3 W C_{OX}}}$$

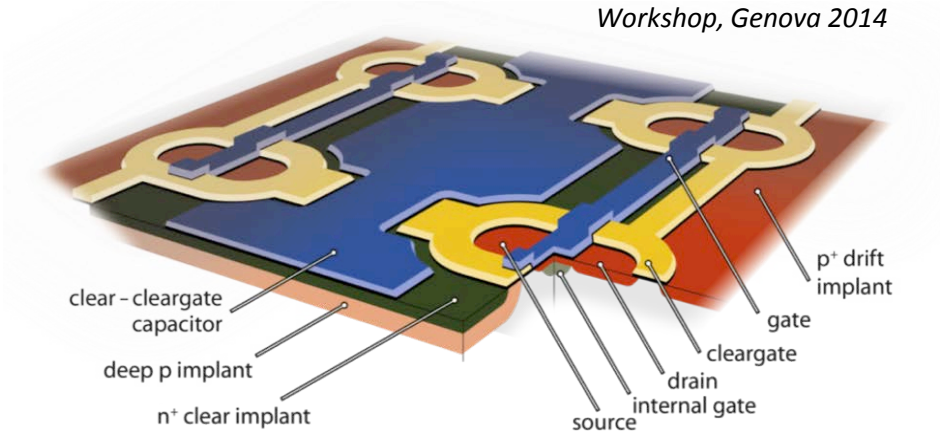
$$g_q = \alpha\frac{g_m}{WLC_{OX}} = \alpha\frac{g_m}{C}$$

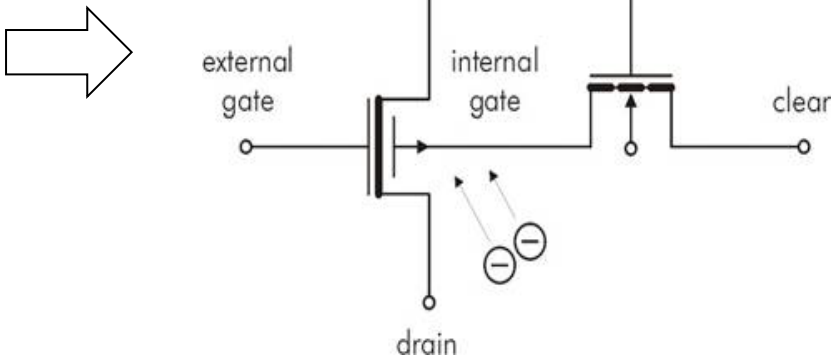
How does a DEPFET work?





© N.Wermes, 9th "Trento" Workshop, Genova 2014





A charge q in the internal gate induces a **mirror charge** αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage:

$\Delta V = \alpha\ q / C = \alpha\ q / (C_{ox}\ W\ L)$

which in turn **changes the transistor current I_D .**

- Internal amplification **g_q~ 500 pA/e^-**
- Small intrinsic noise
- Sensitive off-state, no power consumption

MAPS – Junction Collecting Element

- Collect charge by diffusion and then by drift near the electrode
- Standard CMOS technology, high resistivity p^- epitaxial substrate

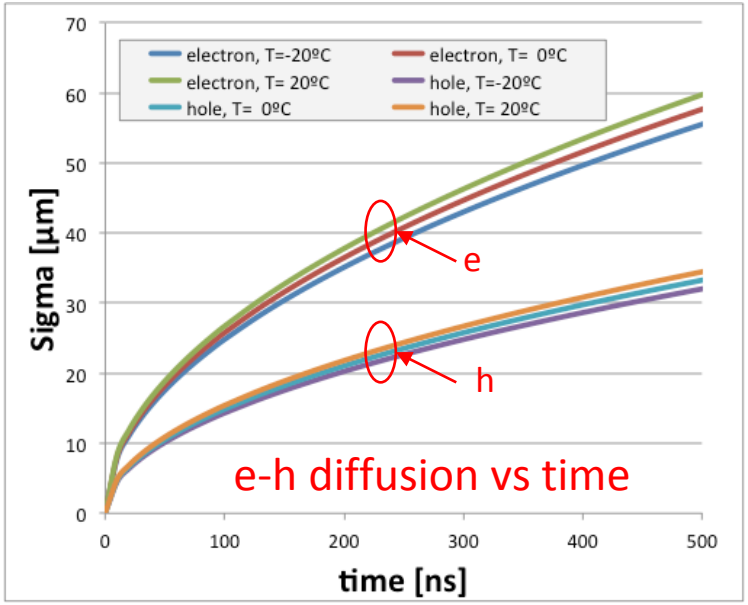
DIFFUSION

$$\sigma_y = \sqrt{2Dt} = \sqrt{2\mu t \frac{kT}{q}}$$

Where D (diffusion coefficient) is given by (Einstein relation):

$$D = \frac{kT}{q}\mu$$

D (electrons) ≤ 36 cm²/s
D (holes) ≤ 12 cm²/s

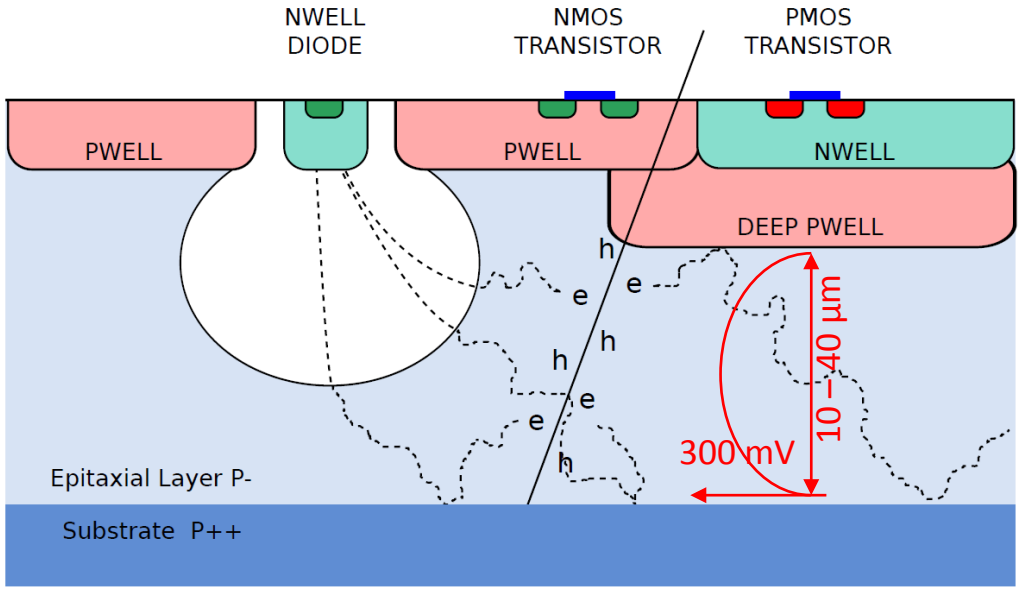


CHARGE COLLECTION – POTENTIAL "MIRROR"

Doping concentration create potentials

$$\Delta V = \frac{kT}{q}\ln\left(\frac{N_{p++}}{N_{p-}}\right) = 26\ln\left(\frac{\sim 10^{19}}{\sim 10^{12}}\right)[mv] \approx 300[mv]$$

Charge confined by potentials diffuse to electrode



Consideration on MAPS R/O

Typical architecture:

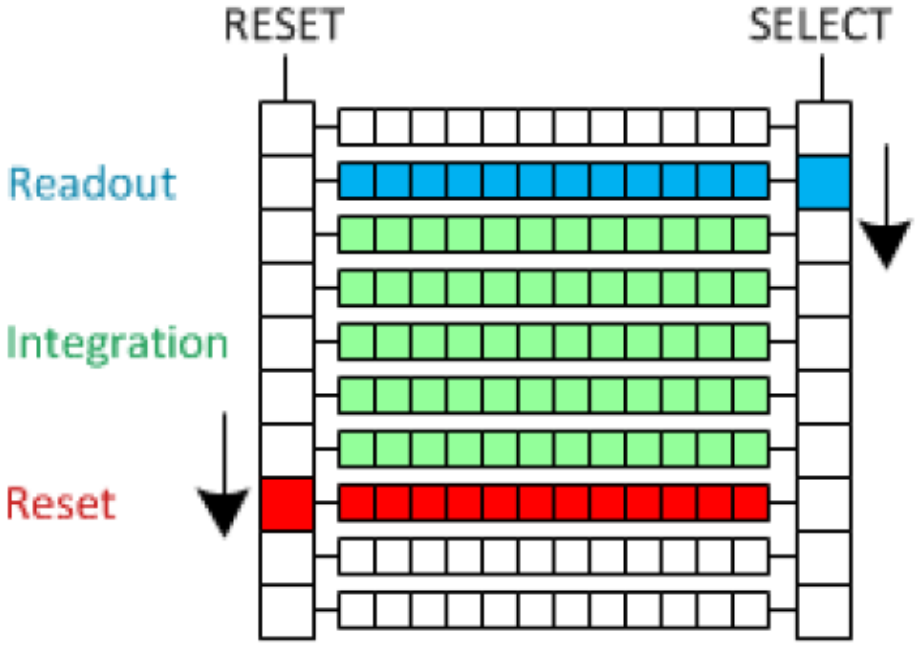
- Rolling shutter

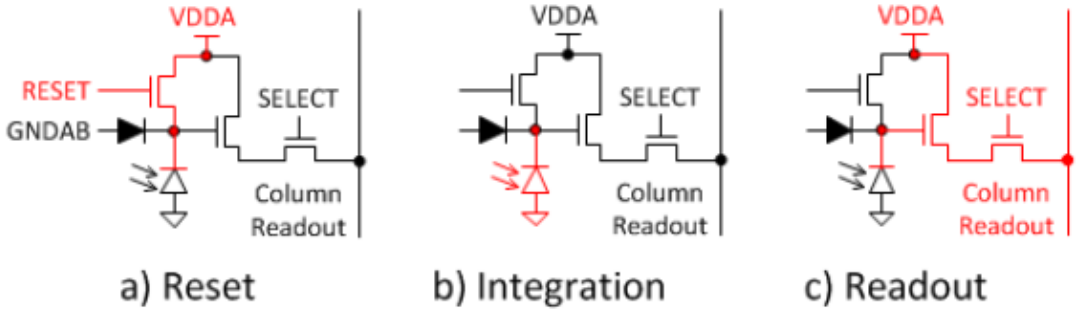
How it works?

- Sequential R/O by rows
- Correlate double sample (CDS) to compensate leakage current and effect of reset pulse

Comments

- 3-transistors cell R/O → small pixel
- Sequential R/O → slow

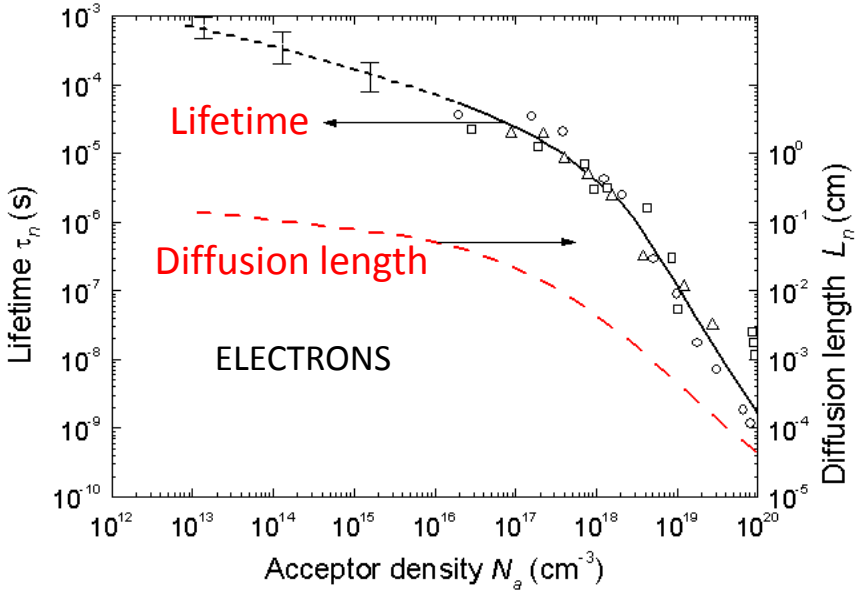




Considerations on Monolithic Pixels

Monolithic pixels (examples shown) works because:

- **Small charge** ~1000 e^- compensated by small detector capacitance (~5 fF) gives small noise (~5 eV).
- **Long integration time** allows collection by diffusion, if carriers have long enough diffusion length L_n: little trapping centres (low enough doping and limited damage from radiation)



Lifetime τ_n and diffusion length L_n of electrons in p-type Si vs. acceptor density

Ref.: Tyagi and Van Overstraeten [1983]

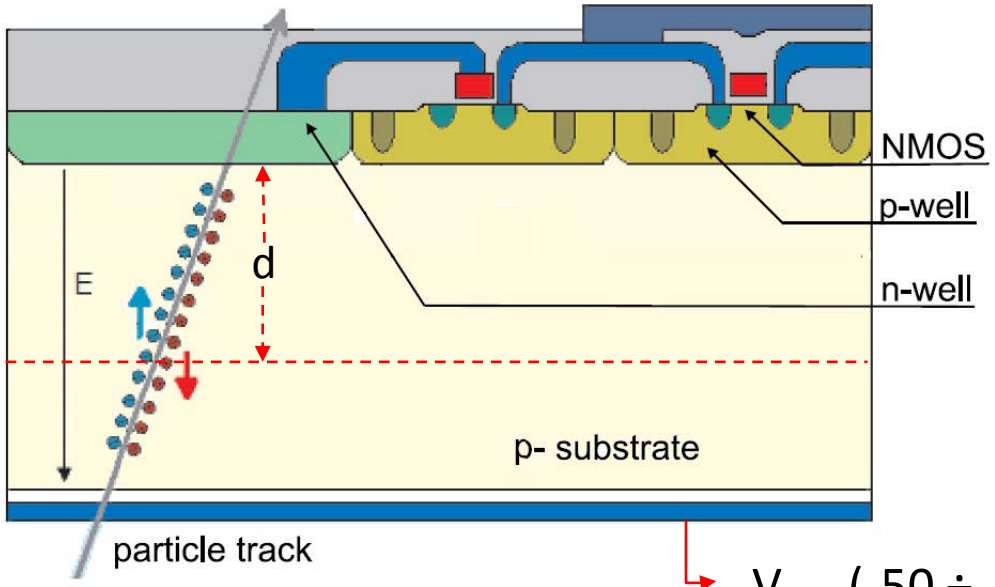
To overcome radiation effect…

… add Drift → HV-CMOS(*)

Go to High Voltage (HV) CMOS technology to add V_{bias} (drift field).
Features:

- Designed for (V_{bias}) 50 – 100 V isolation between transistors and to substrate
- Minimum feature size (technology node): 180 (with shrink 160 µm).
- Gate oxide < 4nm (180 nm technology) → radiation tolerant
- Available medium / high substrate resistivity: ρ = 100 ÷ 3000 Ωcm

(*) Sometimes called HV/HR-CMOS – HR = High Resistivity



Depletion depth (d):

$$d \propto \sqrt{\rho V_{bias}}$$

d: few tens of micron
Substrate can be fully or partially depleted

How to fit architecture

CCPD

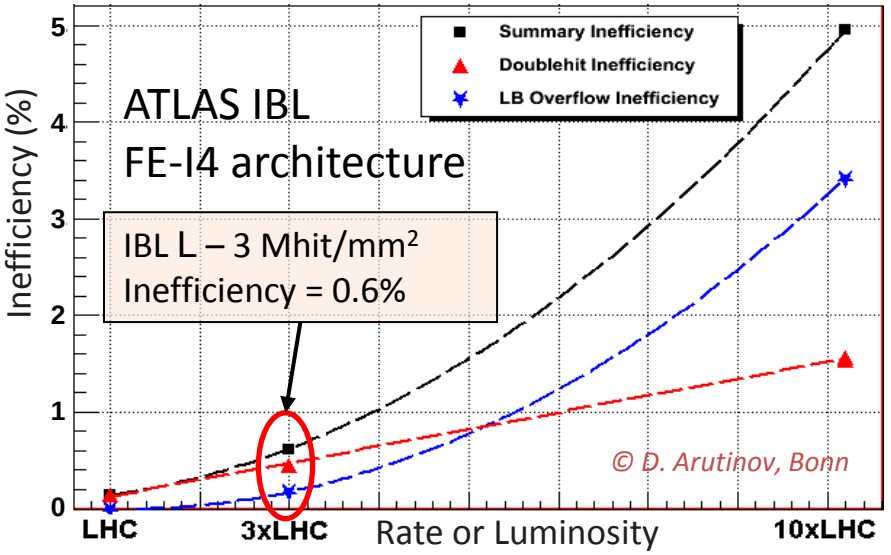
Architecture for (HL-) LHC Data Rates

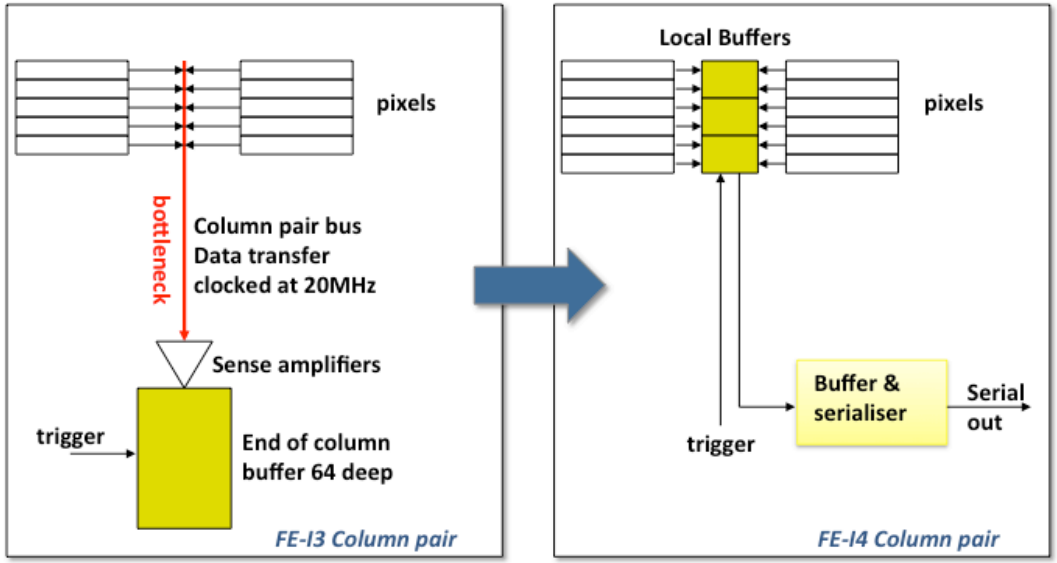
ATLAS example

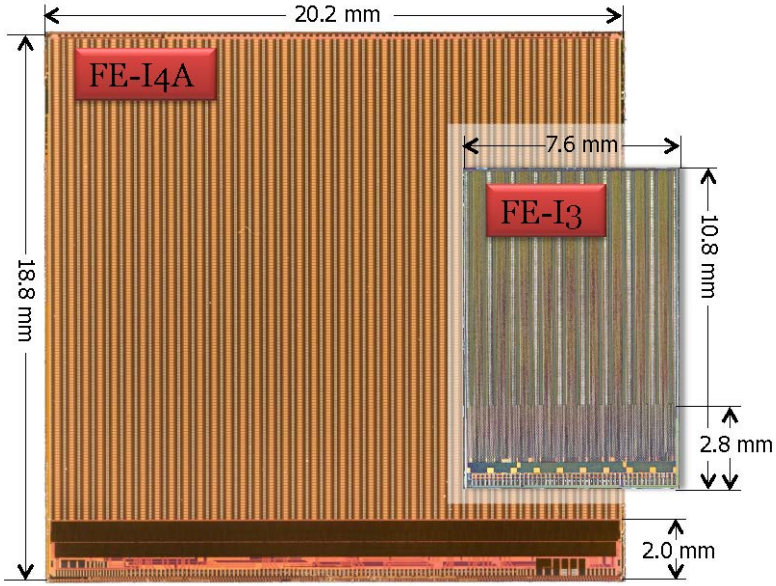
- Hit inefficiency rises steeply with L
- Bottleneck: congestion in transmission from pixels to chip periphery
- Solution: local storage in the pixel array
- > 99% of hits not triggered! Do not move

Chip design considerations

- Memory, pointers and logic in each pixel
- LHC: 250 nm → HL-LHC: LHC 65 nm
- HV-CMOS not suitable for R/O architecture







HV / HR – CMOS Pixels in ATLAS

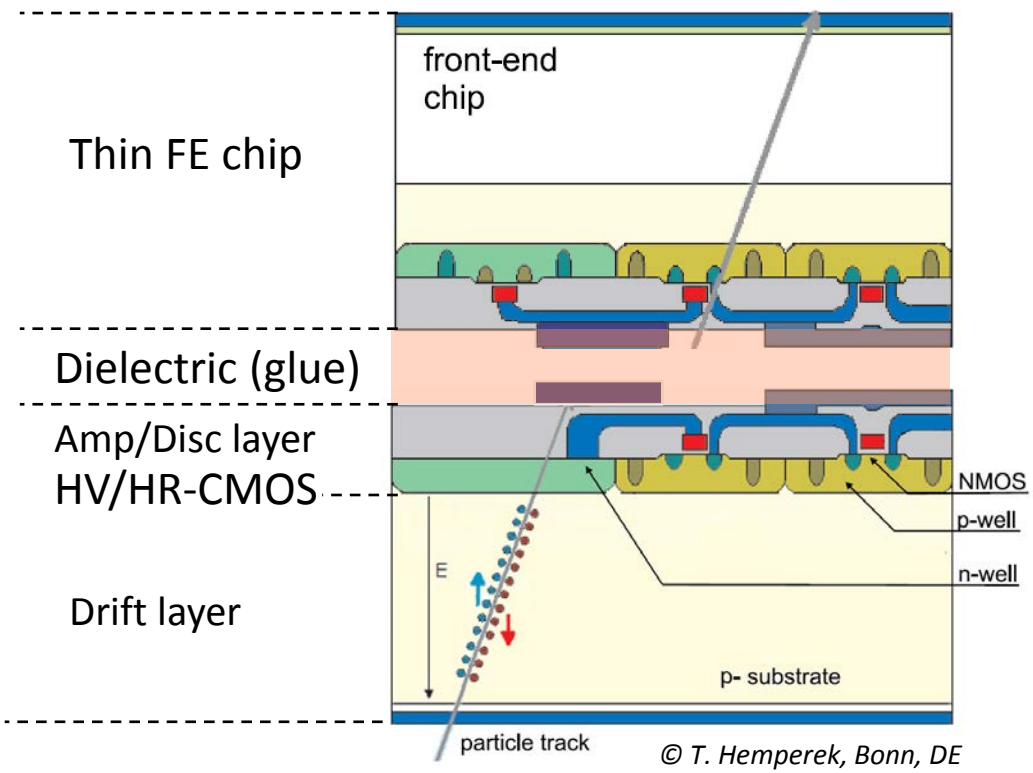
How to match HV/HR-CMOS with R/O Architecture for (ATLAS/CMS) at HL-LHC?

- Hybrid solution:
  - HV/HR-CMOS with pre-amplifier/discriminator (100th transistors / pixel)
  - Pixel chip with trigger/data handling (1000th transistors / pixel)
- Electrical connection… like usual hybrid pixels: bump-bonding, but other options are available…
- As capacitive coupling…

Why capacitive?

- Passive sensors need diode biasing from amplifier other than for collecting charge: AC coupling is (almost) not an option.
- Capacitive coupling it might be cheaper: glue and alignment looks easier.

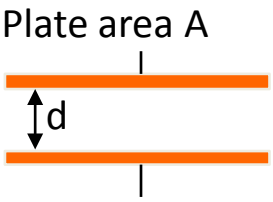
Can it work?...



© T. Hemperek, Bonn, DE

Why Capacitive Coupling Works?

Parallel plate capacitor



$$C = \frac{\varepsilon_r \varepsilon_0 A}{d}$$

Example:

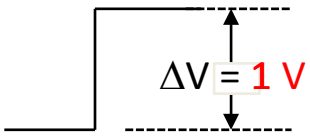
Square pads 20 x 20 μm², 5 μm spacing dielectric with ε_r = 3.8

C = 2.7 fF (C = 4.2 fF with edge effect(*))

(*) http://chemandy.com/calculators/rectangular-capacitor-calculator.htm

HV-CMOS Detector

Assume HV-CMOS output:



Charge at FE-I4 chip in-pad:

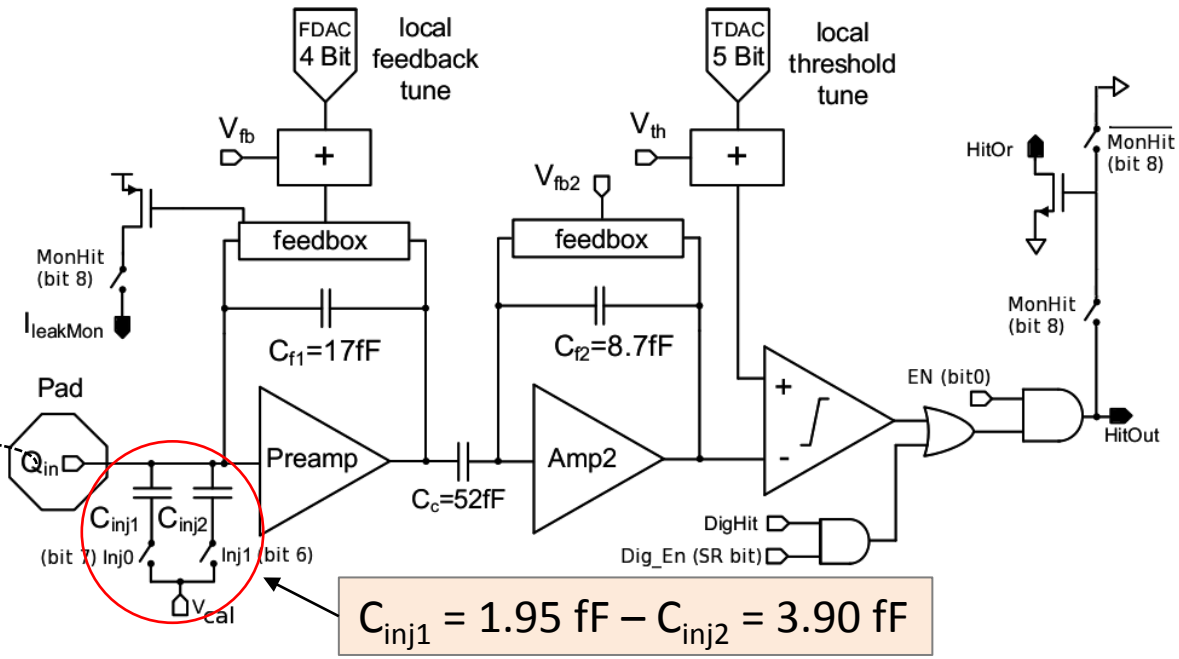
Q [fC] = C [fF] x V [V] = 4. 2 [fC]

Track charge in 200 μm silicon:

Q = 16 ke⁻ = 2.6 fC

The FE-I4 works for HV-CMOS!

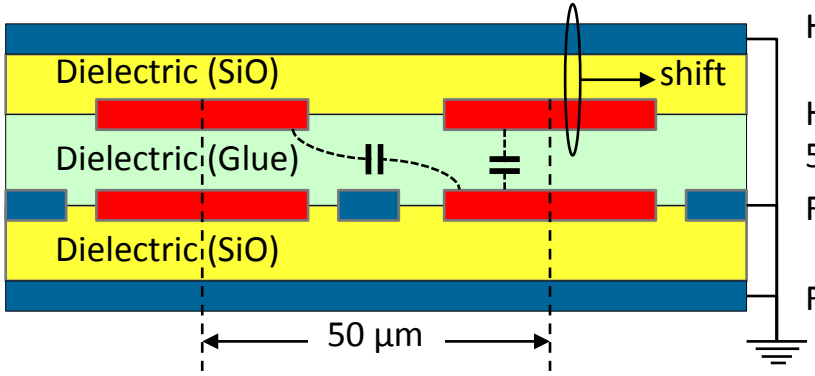
ATLAS IBL – FE-I4 Pixel channel



Coupling Capacitance – 3D Simulation

Coupling capacitance evaluation with 3D electromagnetic simulation (ID3D)

- Example: 25 µm (diagonal) octagonal pads with 50 µm pitch and 5 µm glue

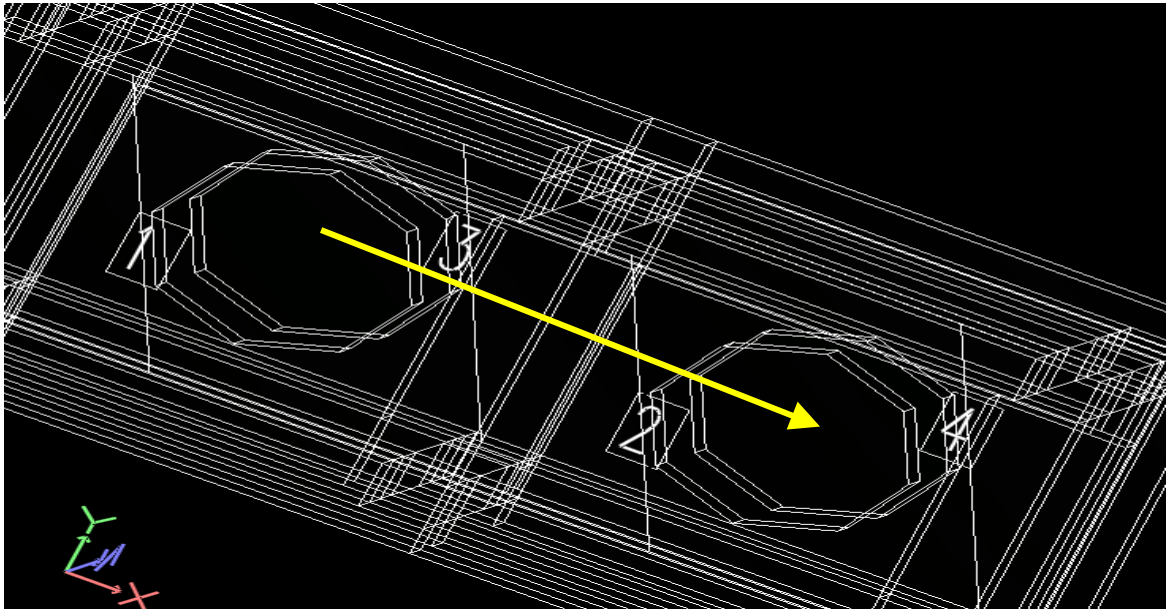


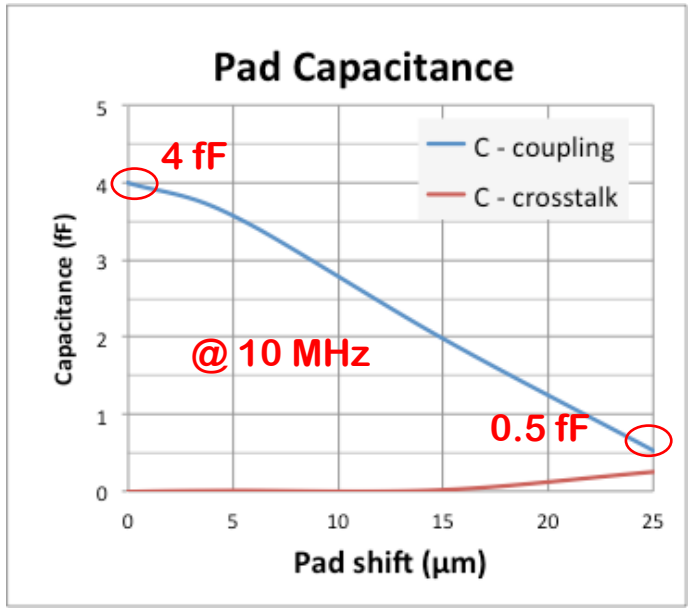
HV/HR-CMOS (Sensor) Ground

HV/HR-CMOS (Sensor) pads
5µm EPOTEK_301-2 (No. 2 substrate layer)

FE-I4 pads

FE-I4 (*) Ground





© E. Ruscino, Genova, IT

Controlled Glue Thickness

Controlled Glue Procedure

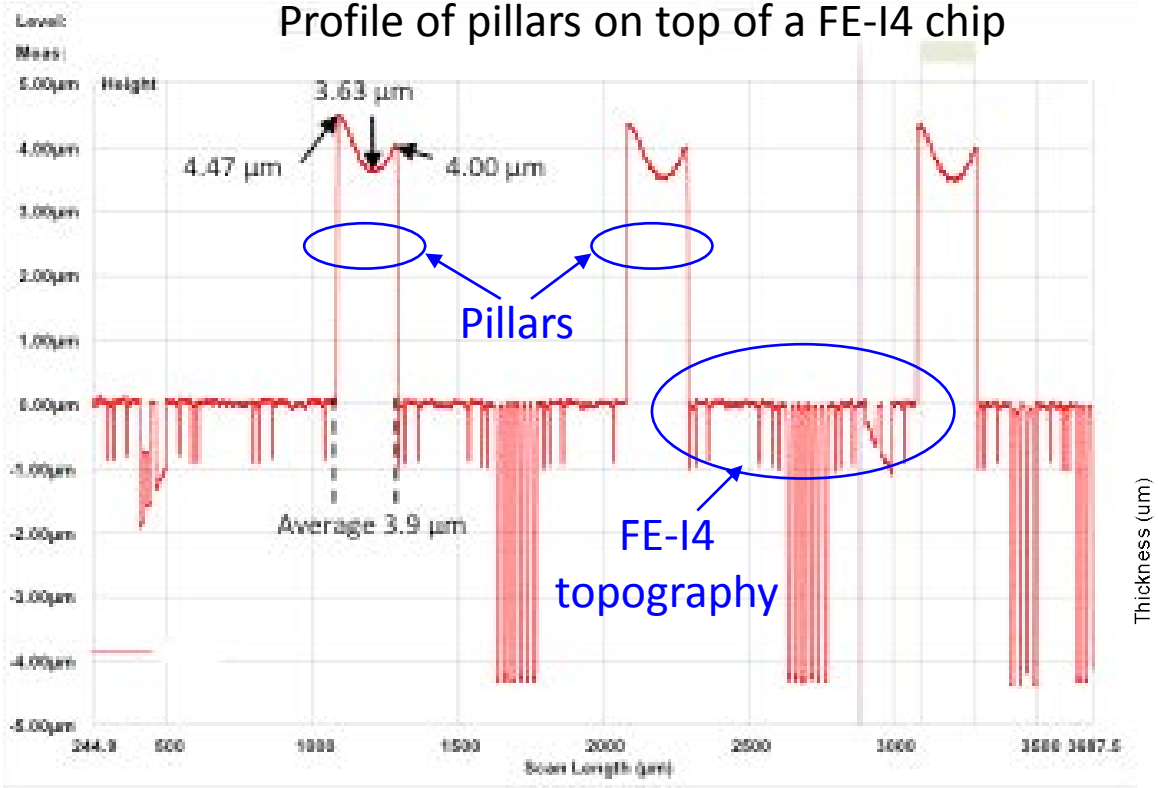
- Deposit uniform layer of SU8 photoresist on R/O chip wafer (or single chip) by spinning – tune for 5µm layer by controlling RPM speed
- Patter pillars using lithographic process .

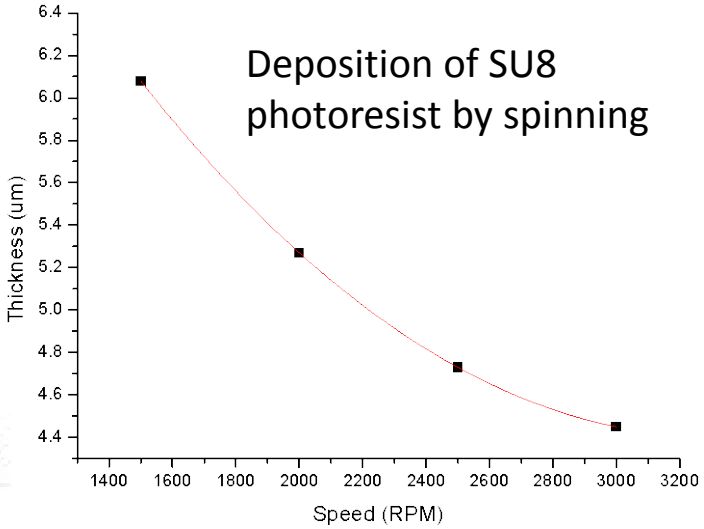
Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition

Align & pressure

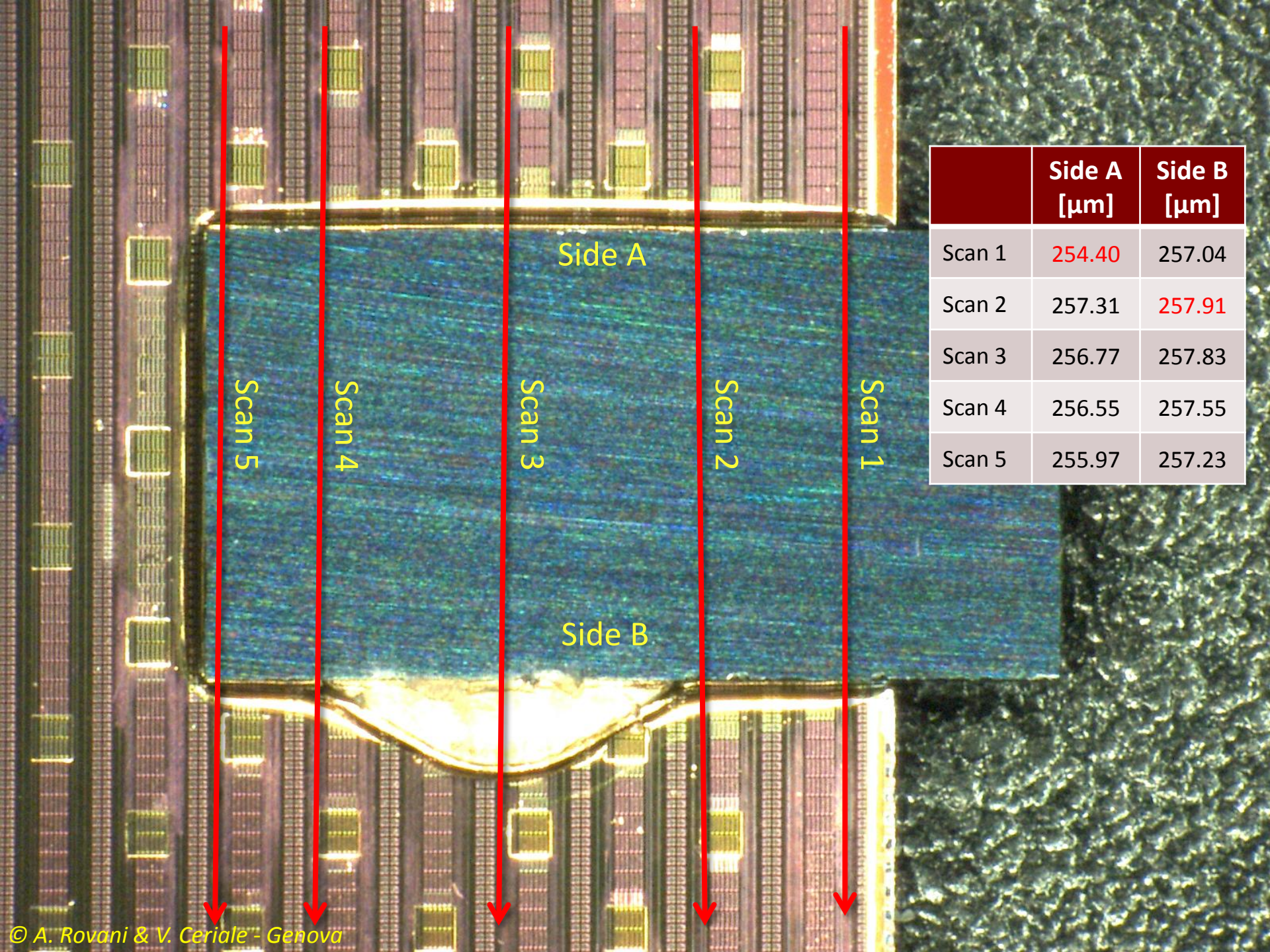
Profile of pillars on top of a FE-I4 chip





Deposition of SU8 photoresist by spinning

© V. Ceriale, A. Rovani, Genova, IT



	Side A [µm]	Side B [µm]
Scan 1	254.40	257.04
Scan 2	257.31	257.91
Scan 3	256.77	257.83
Scan 4	256.55	257.55
Scan 5	255.97	257.23

© A. Rovani & V. Ceriale - Genova

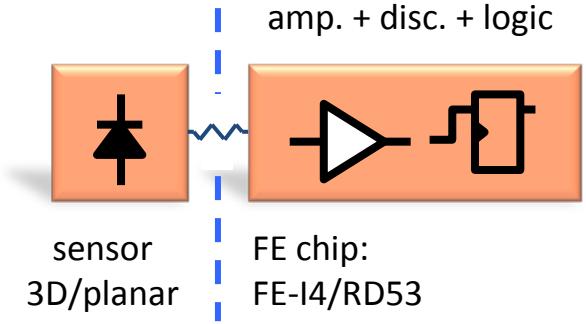
HV/HR-CMOS & CCPD CHIPS

HV/HR-CMOS & CCPD

New detector concept: best of MAPS and Hybrid Pixels (for ATLAS/CMS at HL-LHC)

- Charge collected by drift vs. diffusion: Depleted MAPS (DMAPS)
- Sensor HV/HR-CMOS chip Capacitively Coupled to R/O chip: Capacitively Coupled Pixel Detector (CCPD)

Standard hybrid pixels

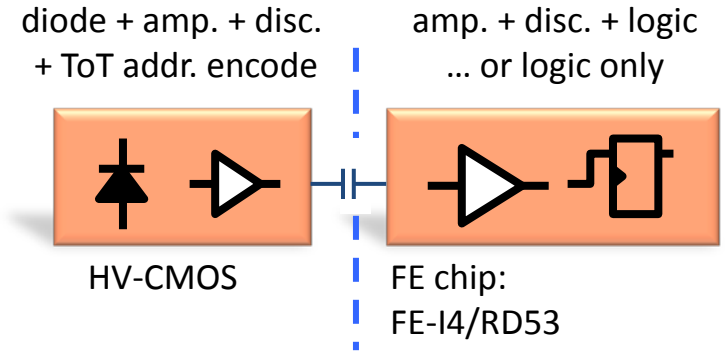


→ expensive

Pro's
Mature technology
Radiation hard
Multi-chip modules

Con's
Sensor/bump cost
4"÷6" sensor wafer
Spatial resolution
Cost/yield of BB

HV-CMOS hybrid pixels



→ simpler/cheaper ?

Pro's
8" (or 12") HV-CMOS wafers
"Standard" IC process
Cheap BB (to demonstrate)
Small pixel → resolution

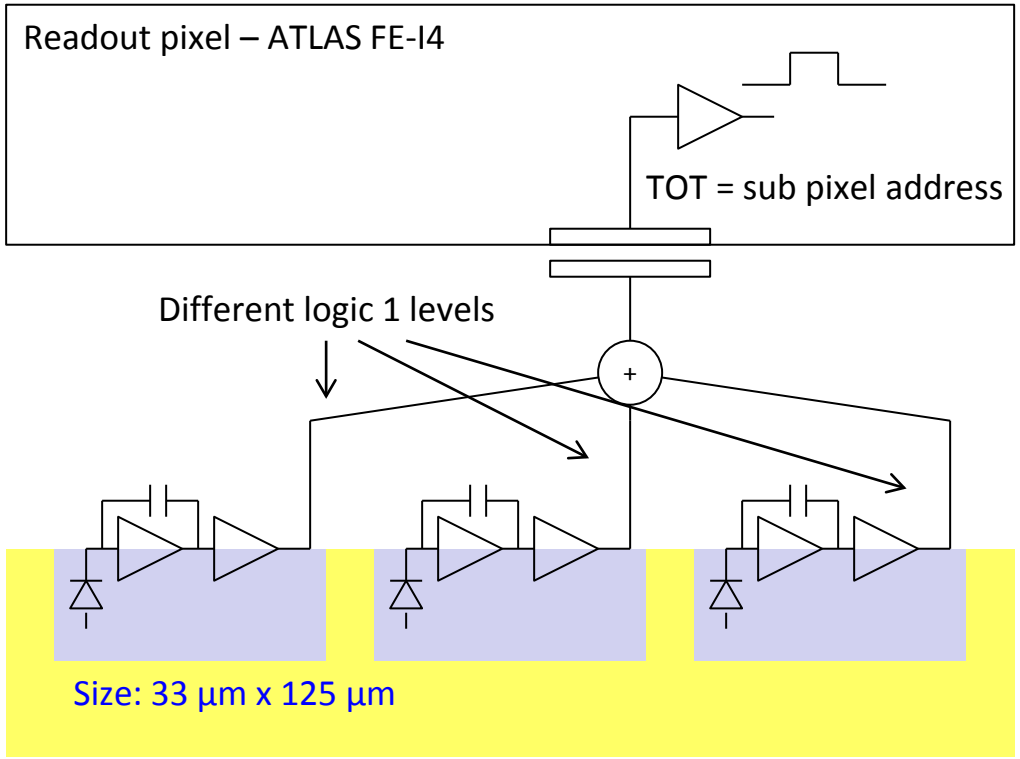
Con's
Novel technology
Small charge (800÷1500 e)
Extreme radiation ?
Single chip (multi-chip difficult)

CCPD

CCPD with sub-pixel address encoding

Example: using FE-I4 R/O chip

Size: 50 µm x 250 µm

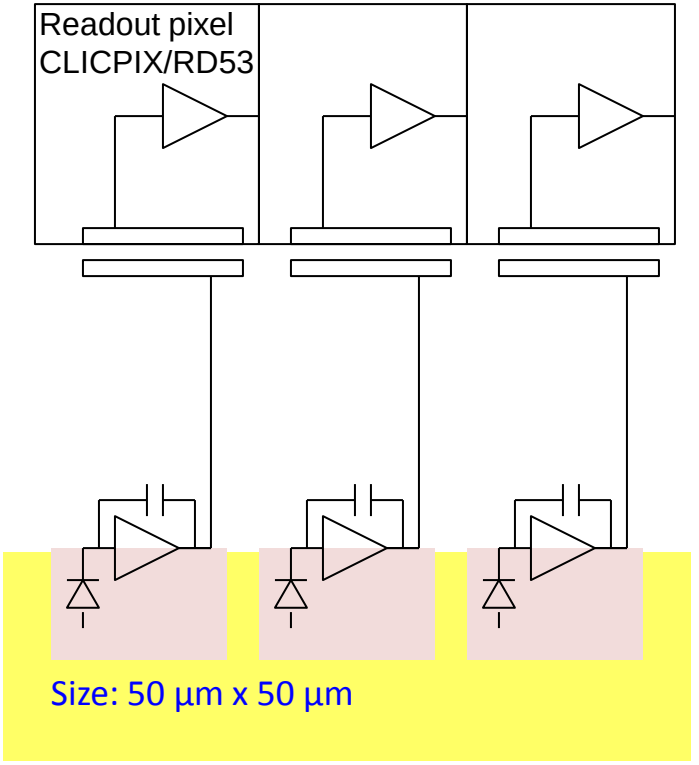


© Ivan Perić, KIT, Germany

CCPD with one-to-one pixels

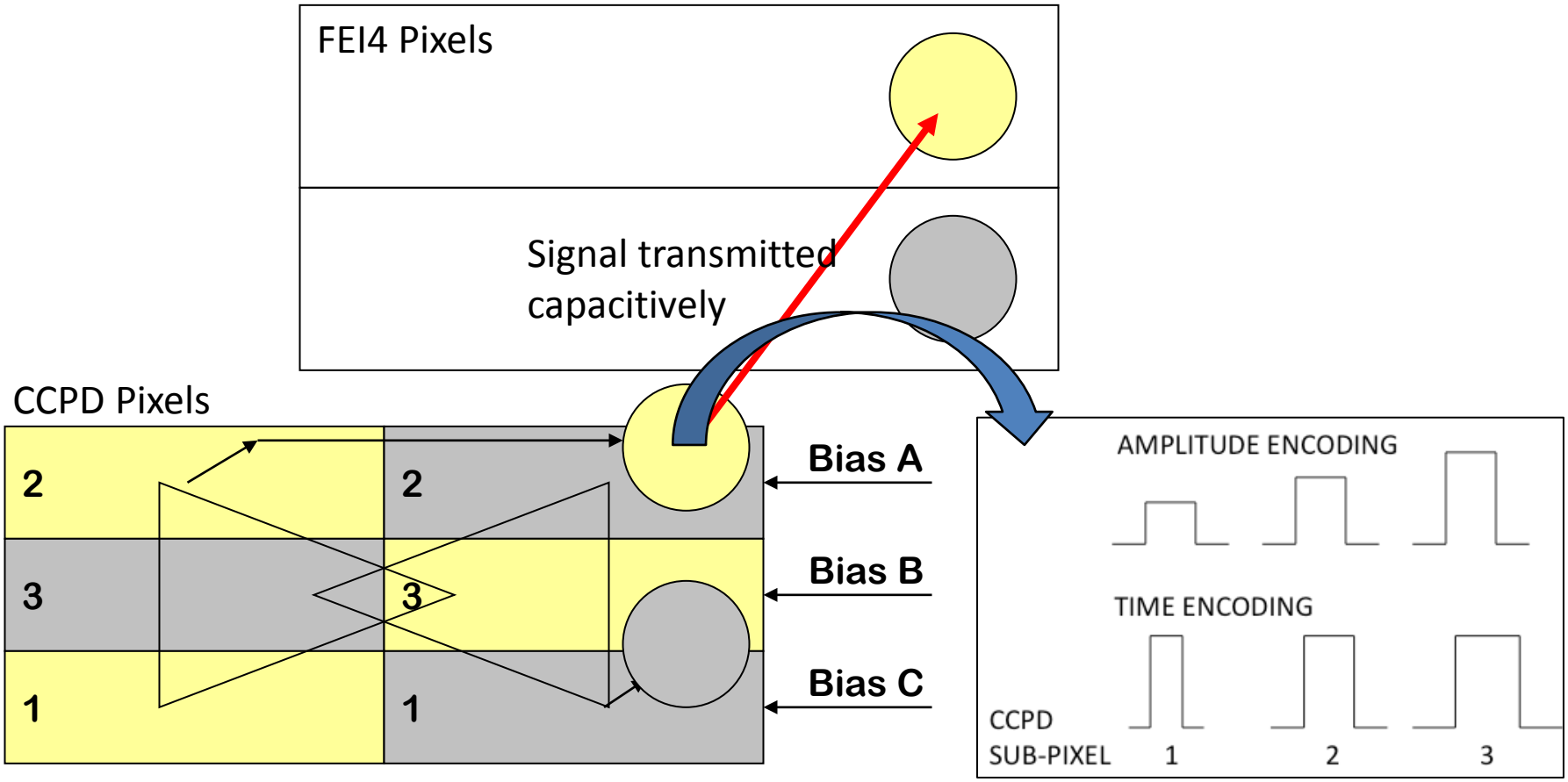
Example: CLIC or RD53 R/O chips

Size: 25 x 25 µm² (CLICPIX)
50 x 50 µm² (RD53)

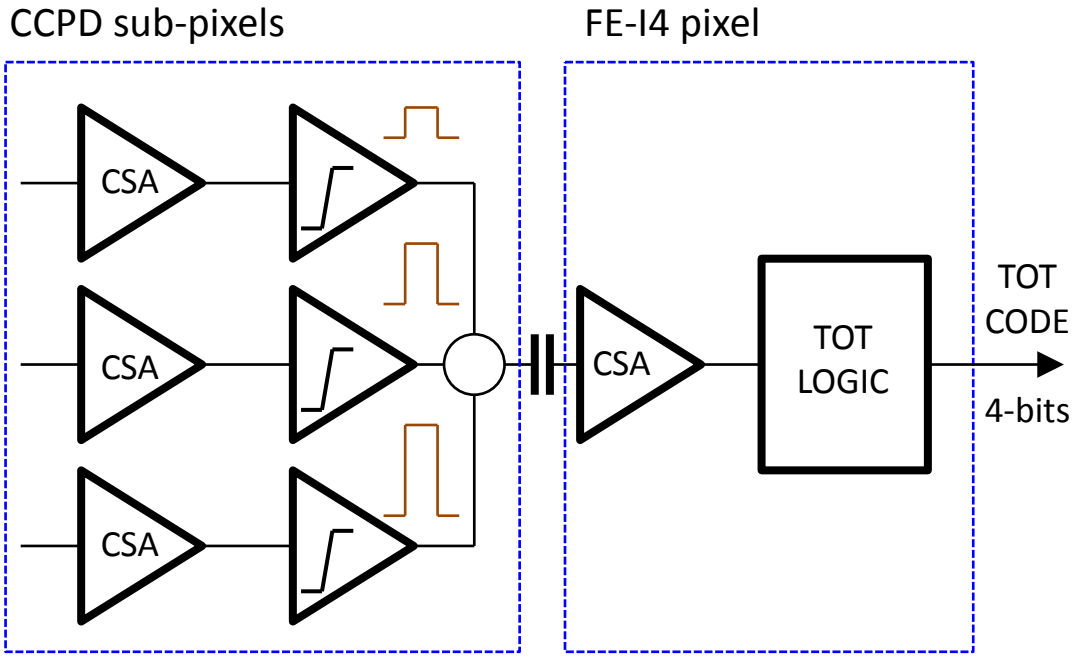


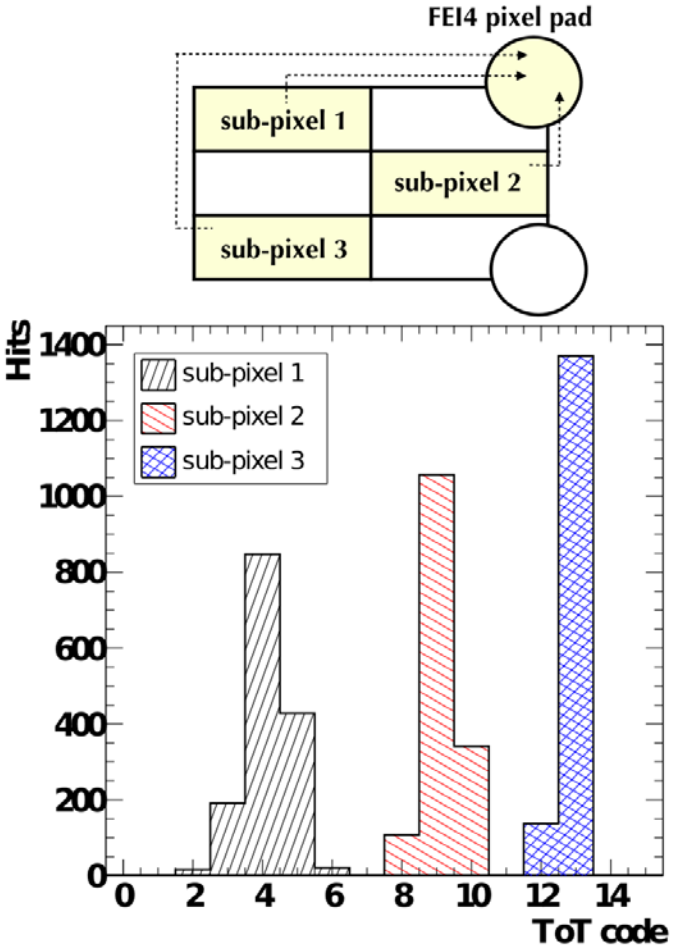
© Ivan Perić, KIT, Germany

Sub-pixel Encoding



TOT Encoding





Distribution of the Time over Threshold (ToT) for a single FEI4 pixel.

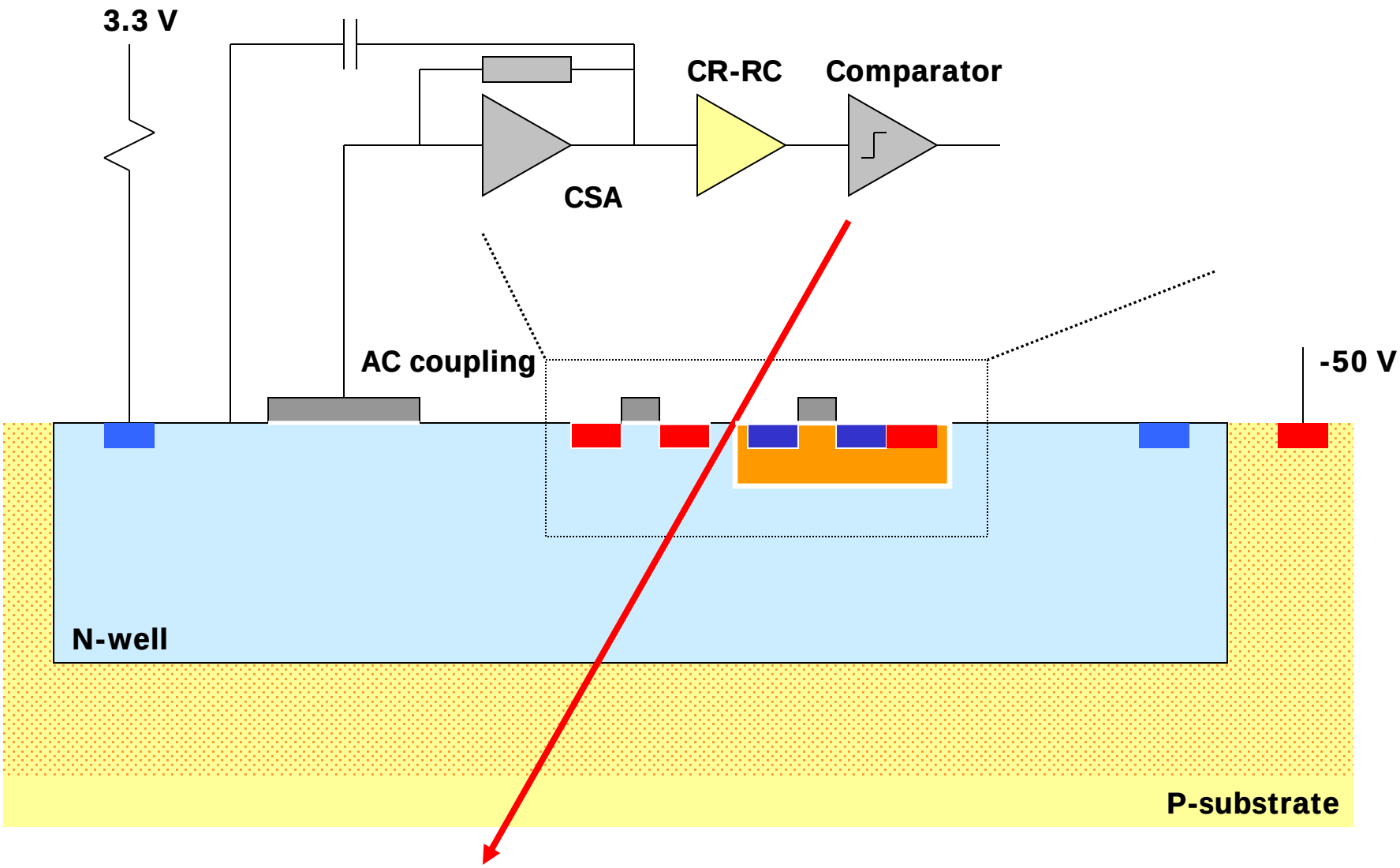
A.Miucci et al. IWORID2013 [Ref.5]

Definitions

CSA = Charge Sensitive Amplifier

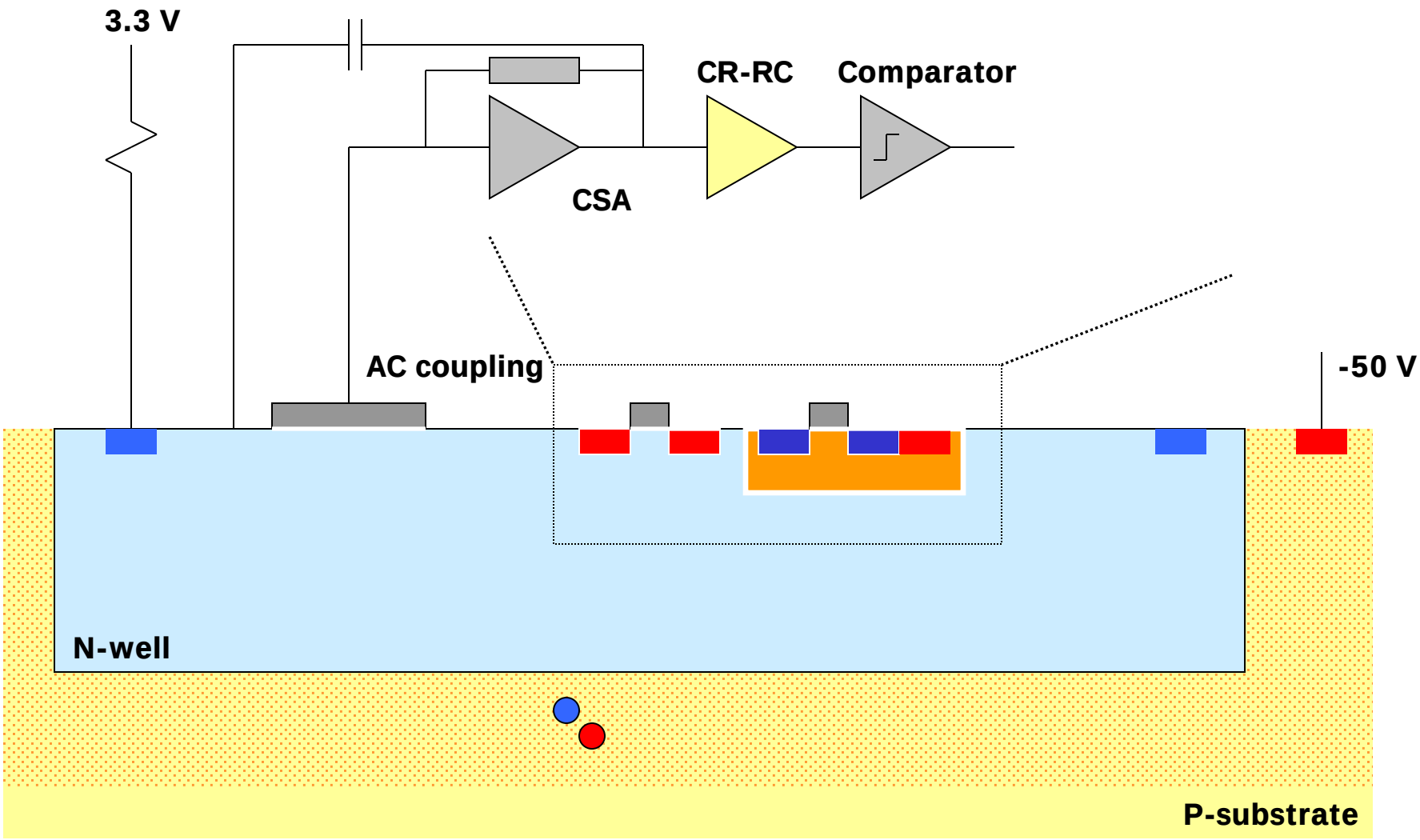
TOT = Time Over Threshold
(Amplitude to Time Conversion)

HV/HR-CMOS Operation Principle



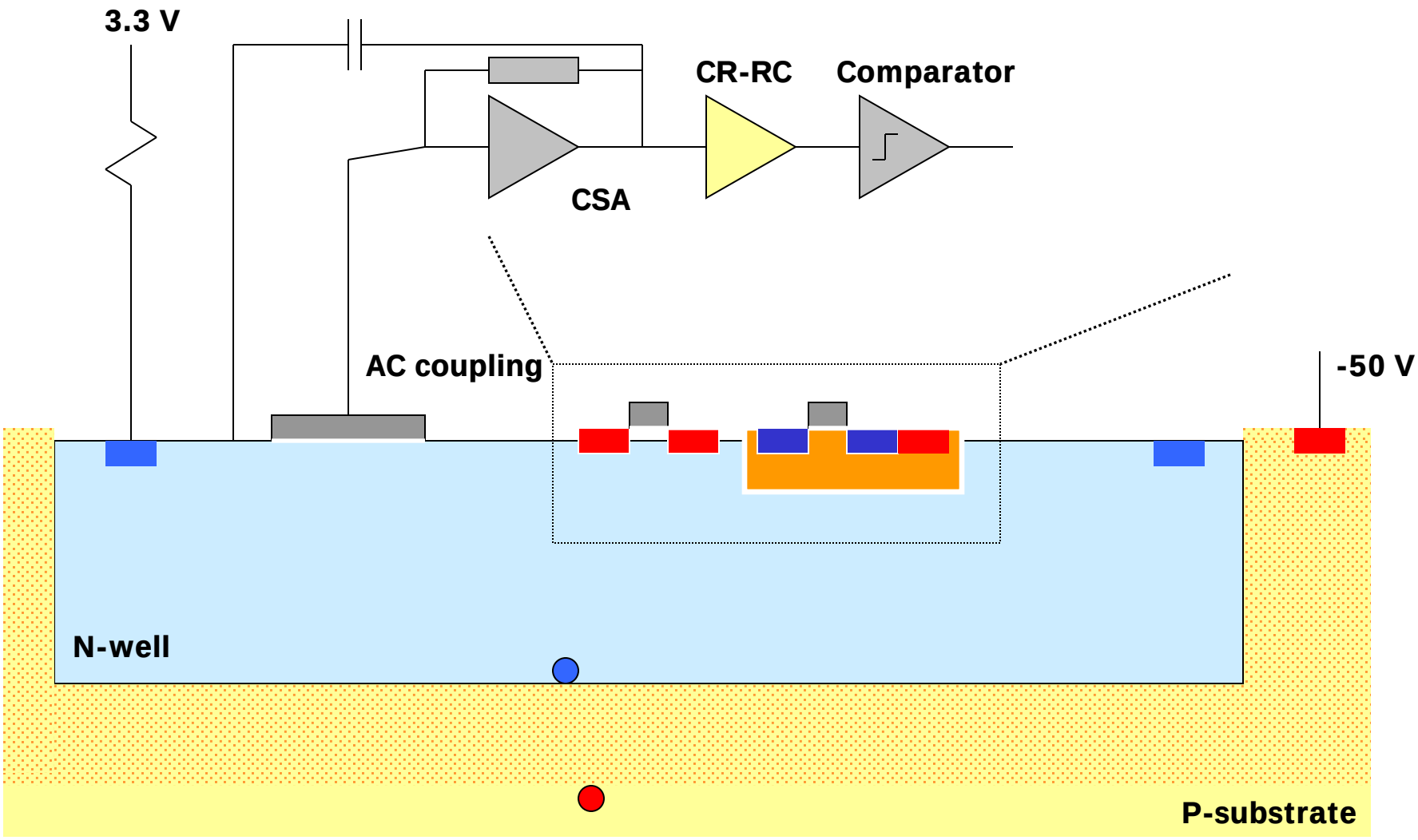
© Ivan Perić, KIT, Germany – Seminar Milano July 2014

HV/HR-CMOS Operation Principle



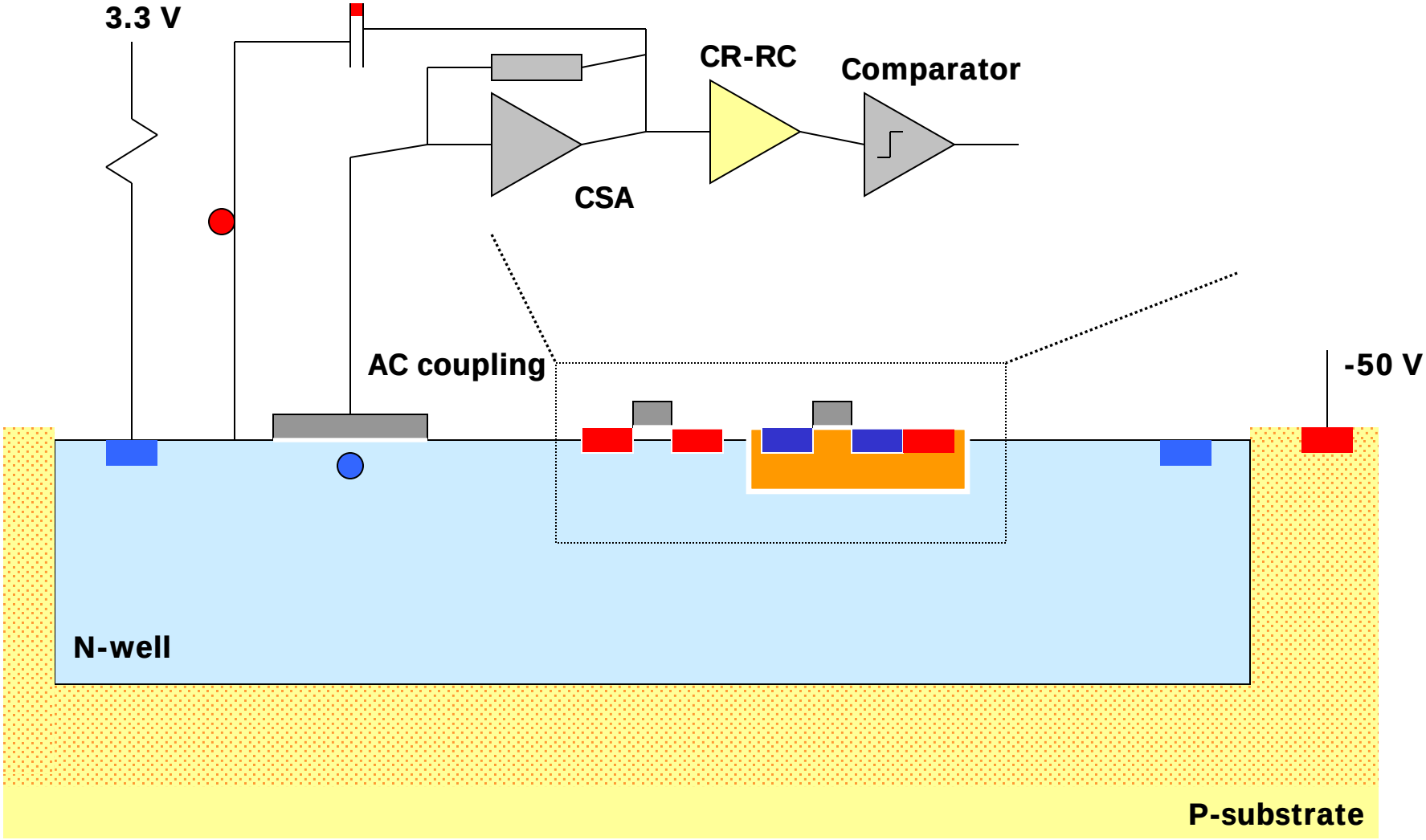
© Ivan Perić, KIT, Germany – Seminar Milano July 2014

HV/HR-CMOS Operation Principle



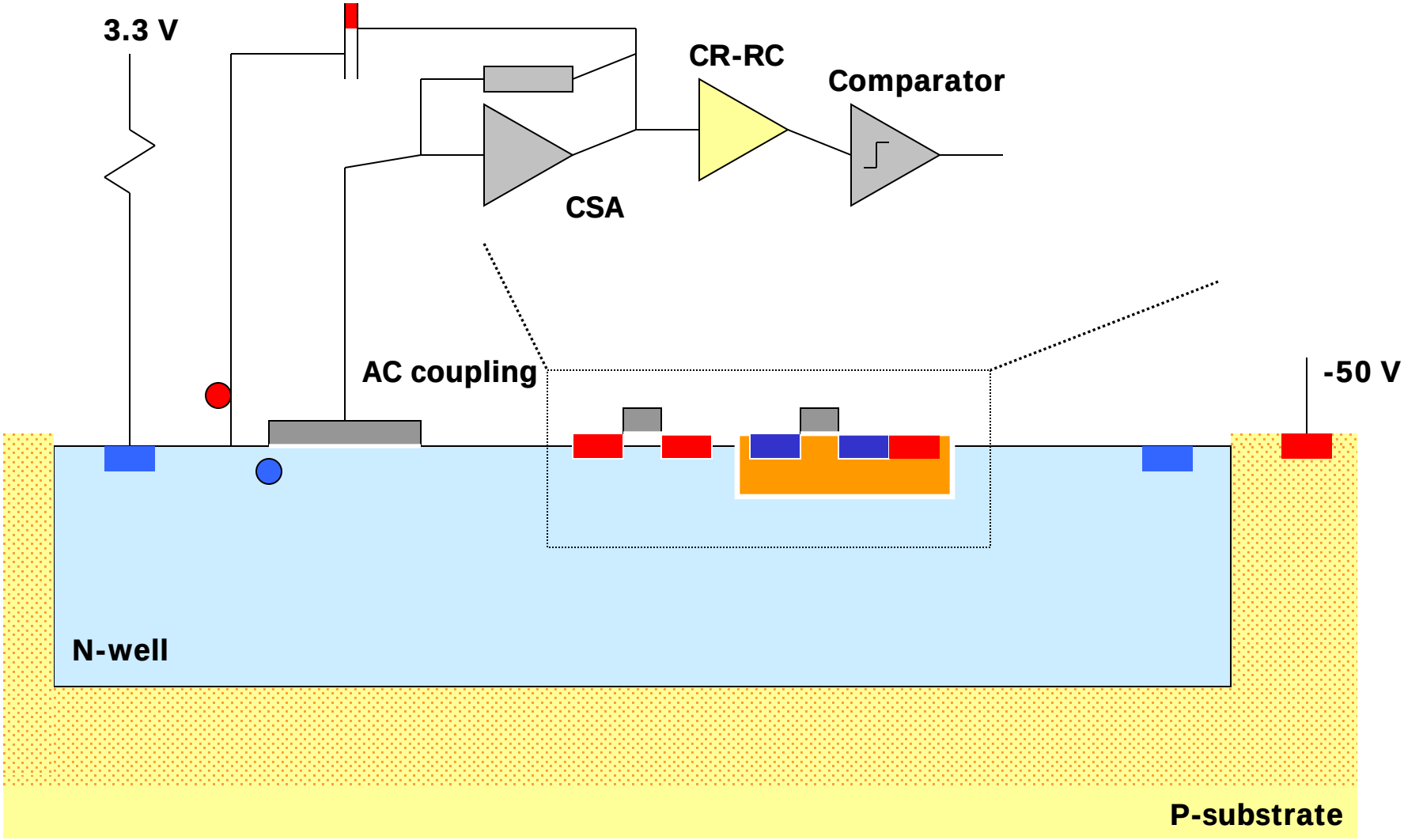
© Ivan Perić, KIT, Germany – Seminar Milano July 2014

HV/HR-CMOS Operation Principle



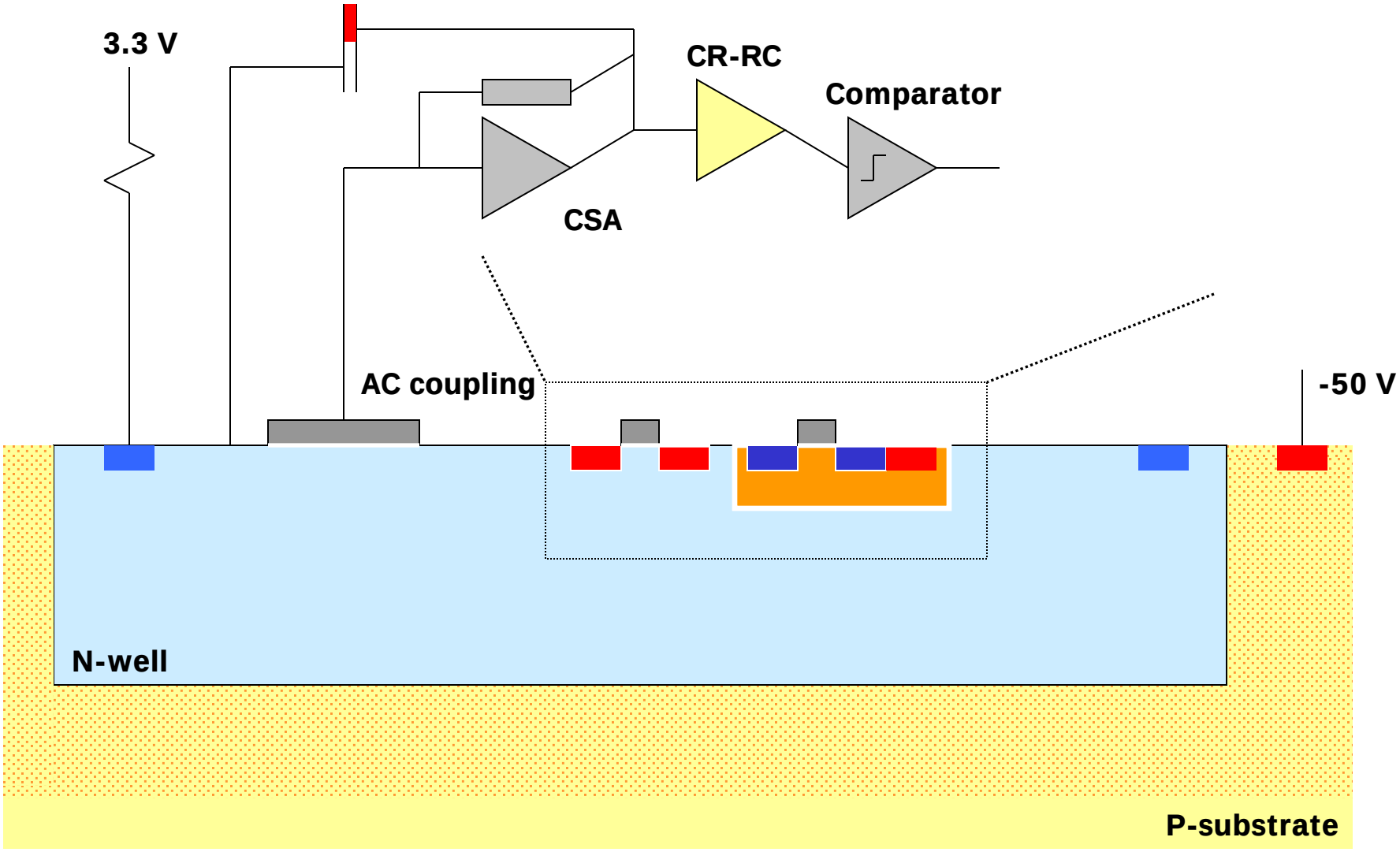
© Ivan Perić, KIT, Germany – Seminar Milano July 2014

HV/HR-CMOS Operation Principle



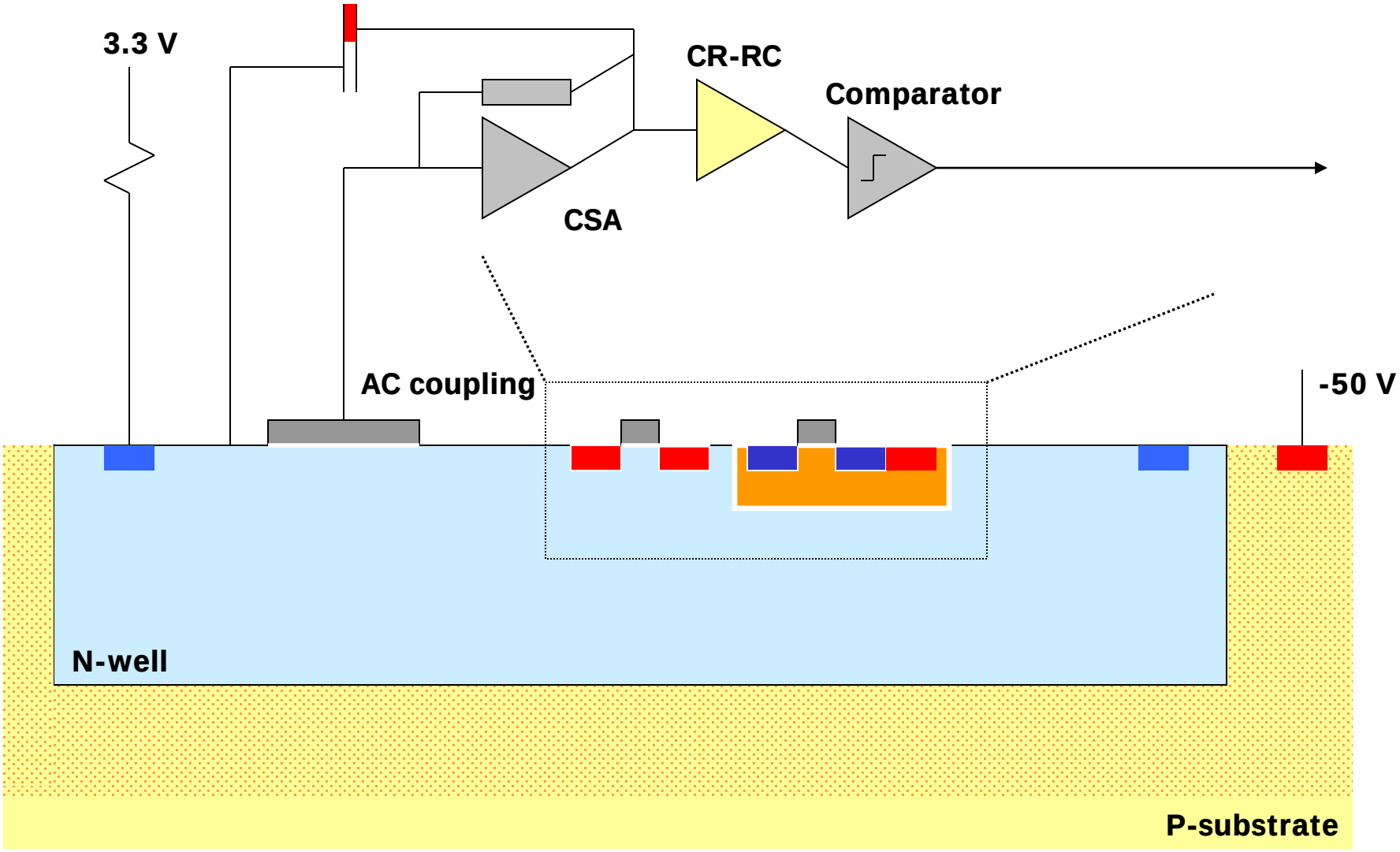
© Ivan Perić, KIT, Germany – Seminar Milano July 2014

HV/HR-CMOS Operation Principle



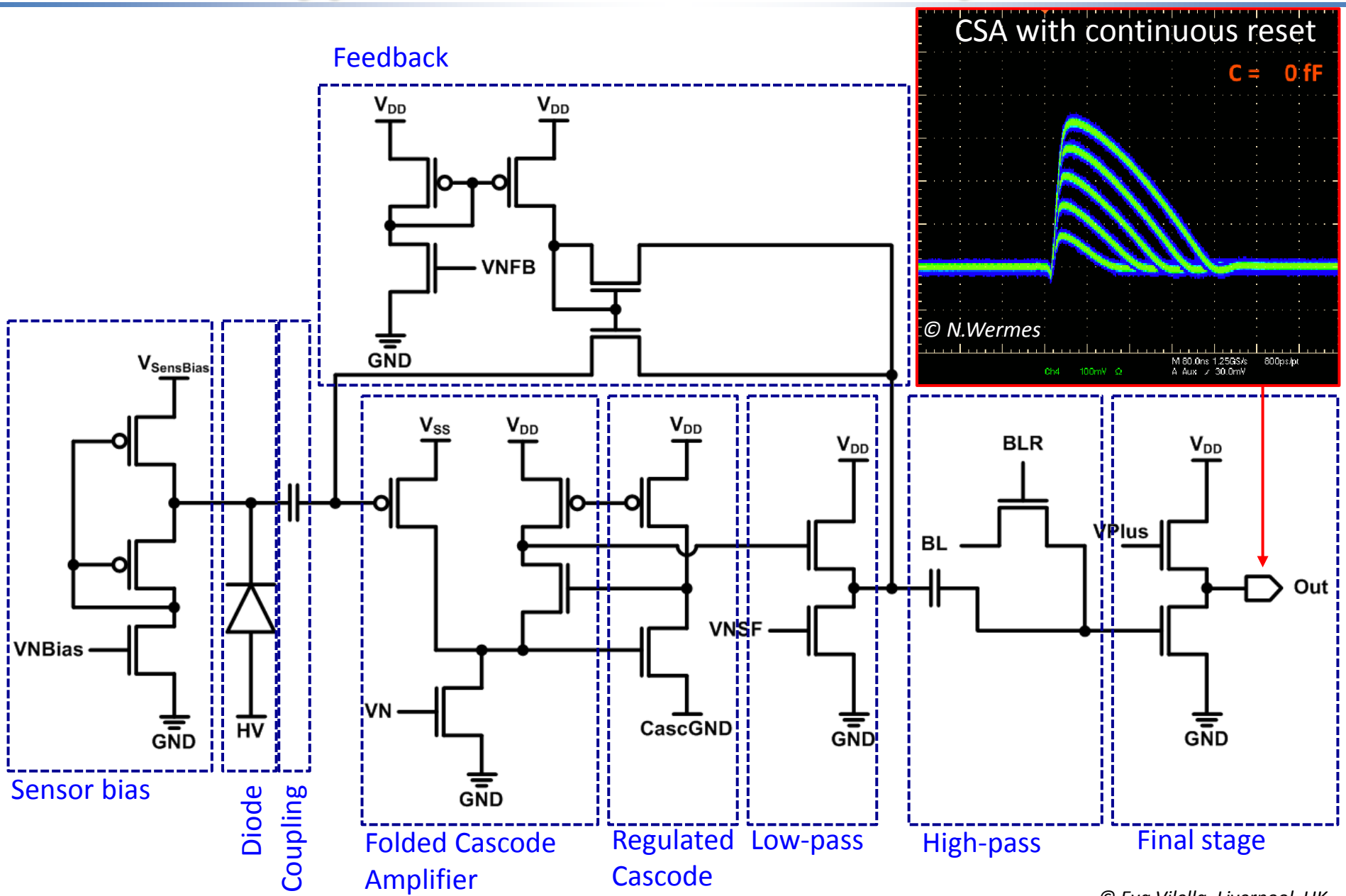
© Ivan Perić, KIT, Germany – Seminar Milano July 2014

HV/HR-CMOS Operation Principle



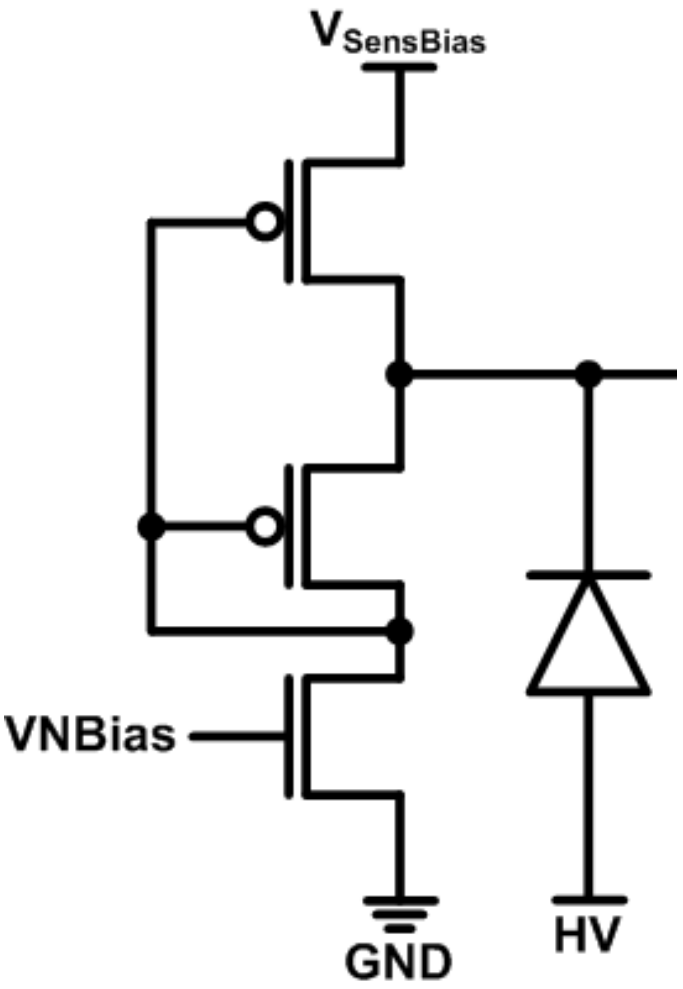
© Ivan Perić, KIT, Germany – Seminar Milano July 2014

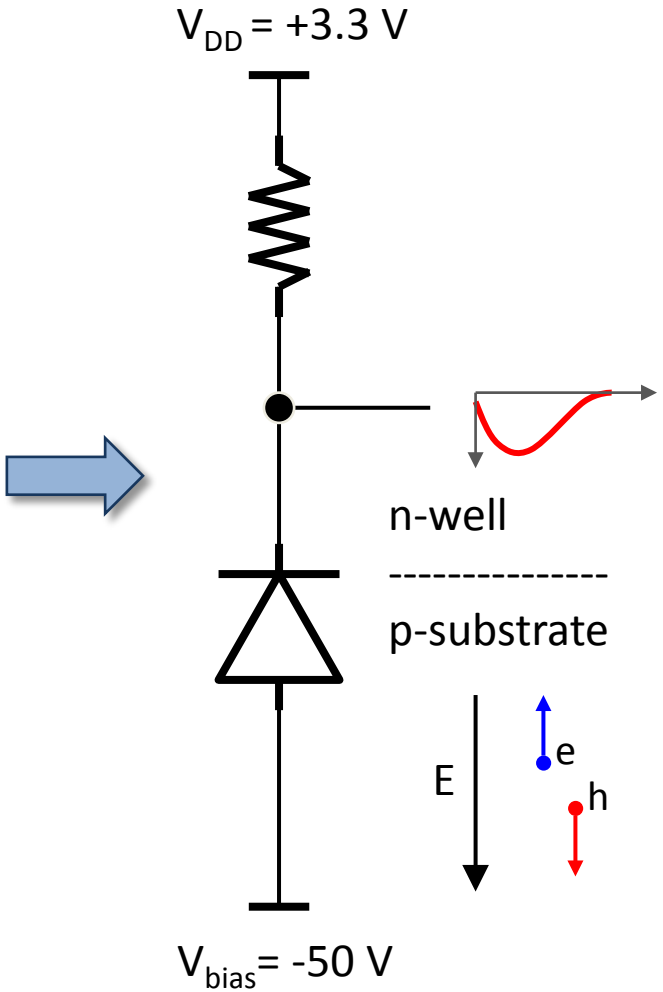
“Typical” HV-CMOS Amplifier



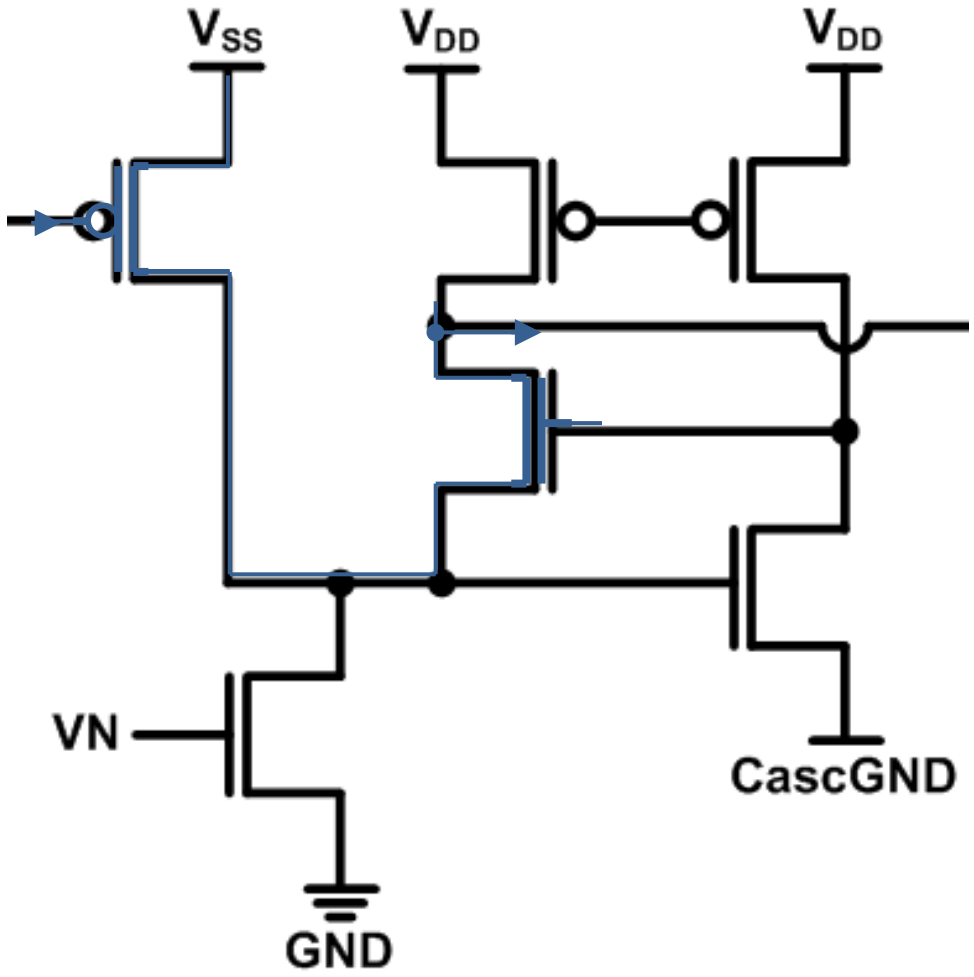
© Eva Vilella, Liverpool, UK

“Typical” HV-CMOS Amplifier



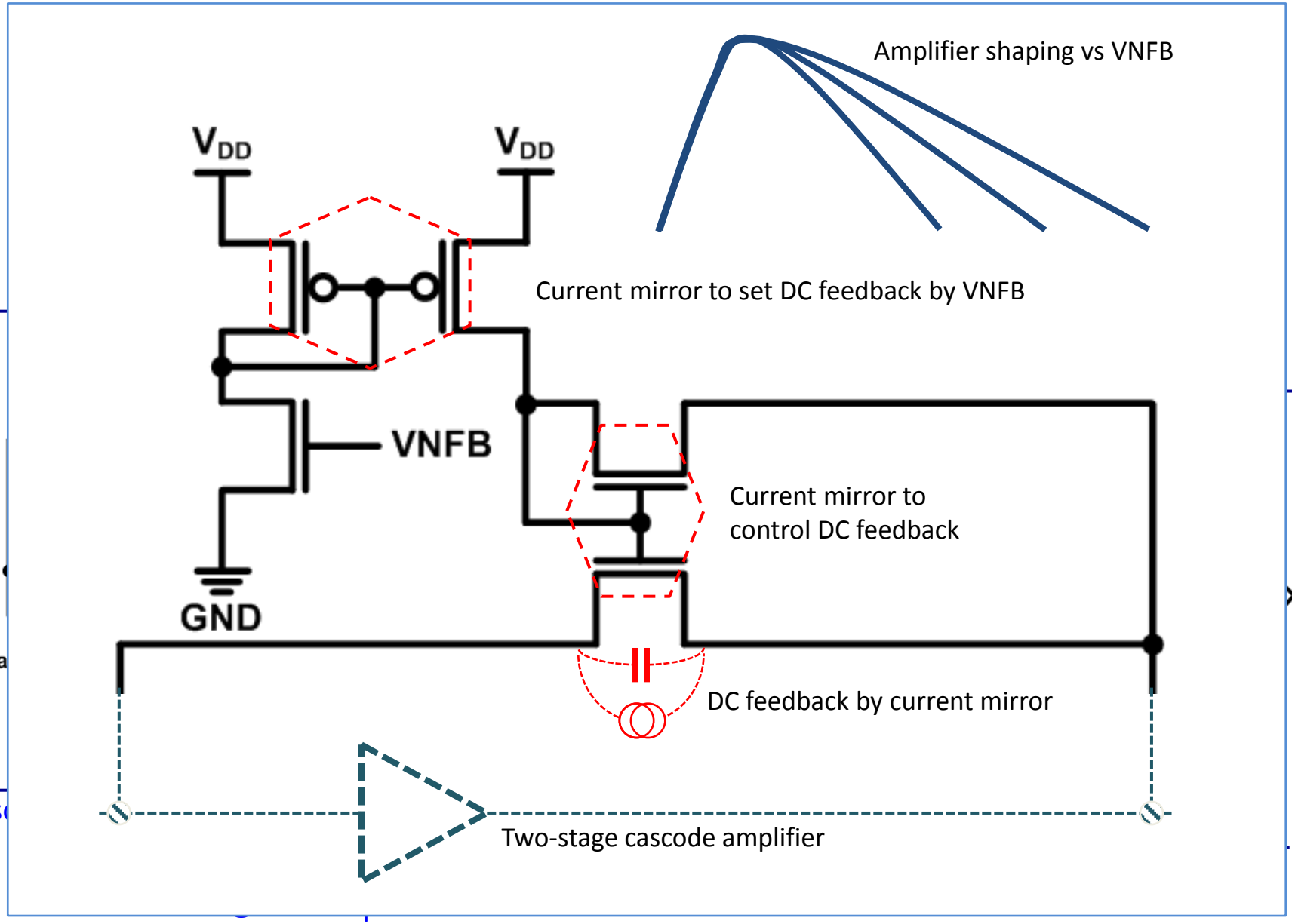


“Typical” HV-CMOS Amplifier



Folded Cascode:
is a two-stage amplifier composed of a trans-conductance amplifier followed by a current buffer.

"Typical" HV-CMOS Amplifier

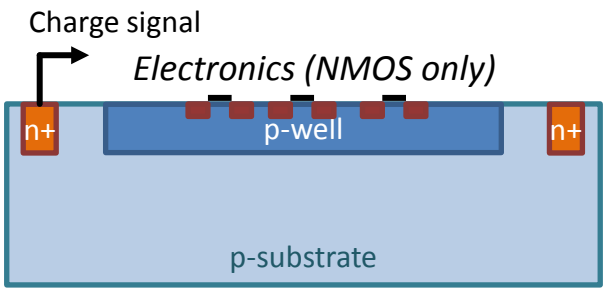


For DC feedback analysis see [ref.4]

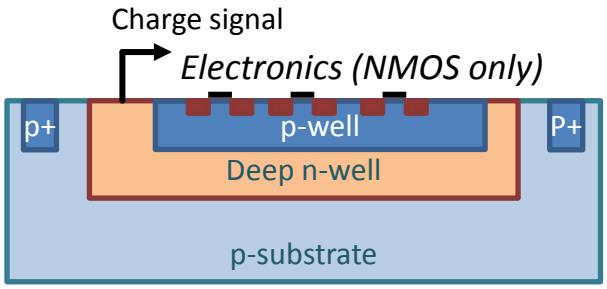
TECHNOLOGY IMPLEMENTATION

CMOS: 2 vs 3 Wells

CMOS with twin or triple wells

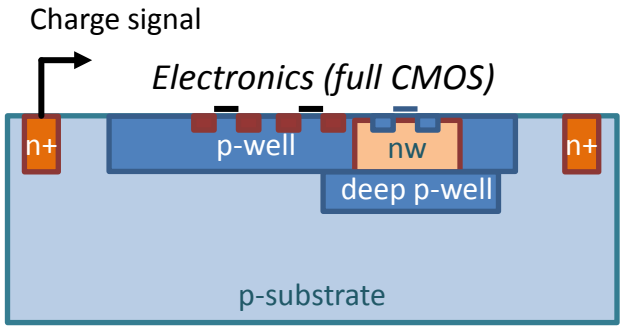


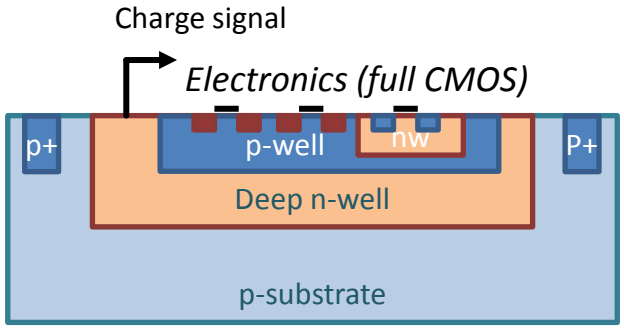
"MAPS" like



CCPD (HVCMOS)
DMAPS

CMOS with additional implants





Electronics outside charge collection well

- Very small sensor capacitance → low power
- Potentially less rad. hard (longer drift lengths)
- Full CMOS with additional deep-p implant

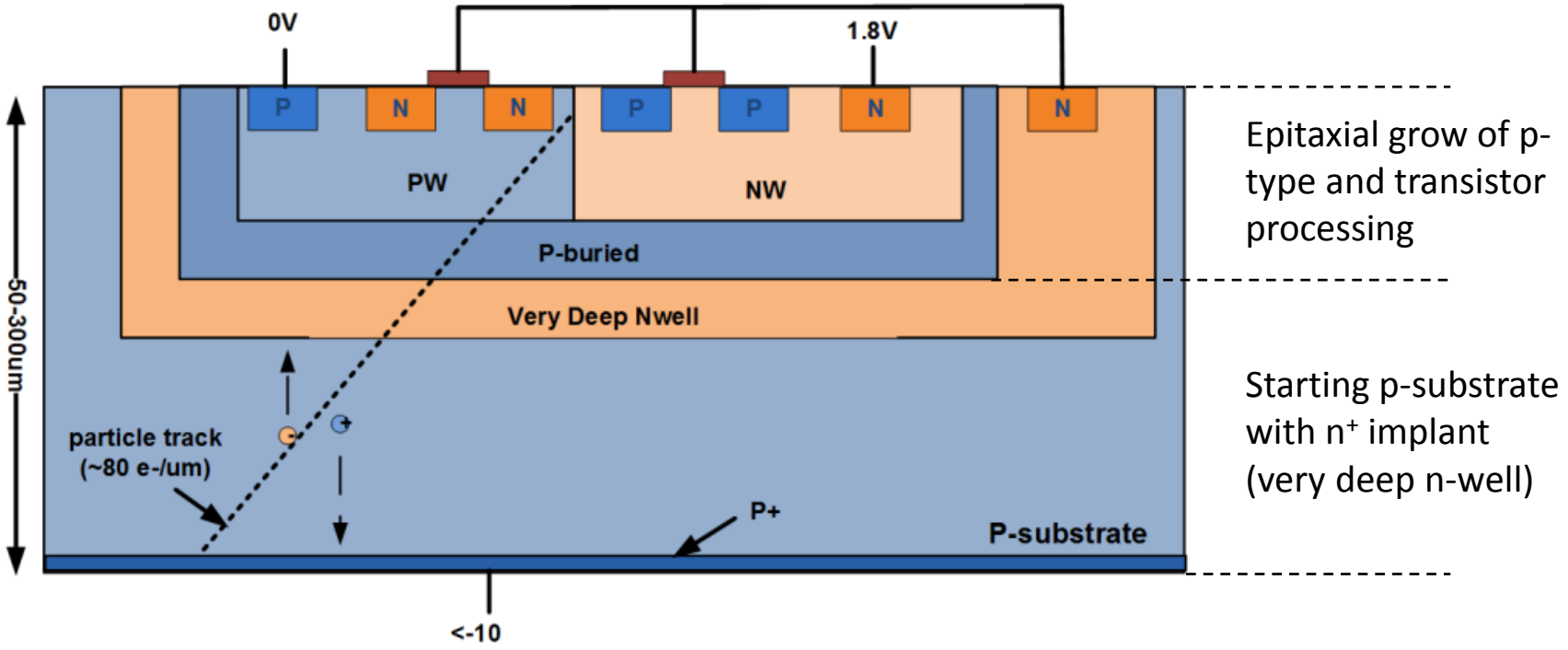
Electronics inside charge collection well

- Collection node with large fill factor → rad. hard
- Large sensor capacitance (DNW/PW junction!) → x-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

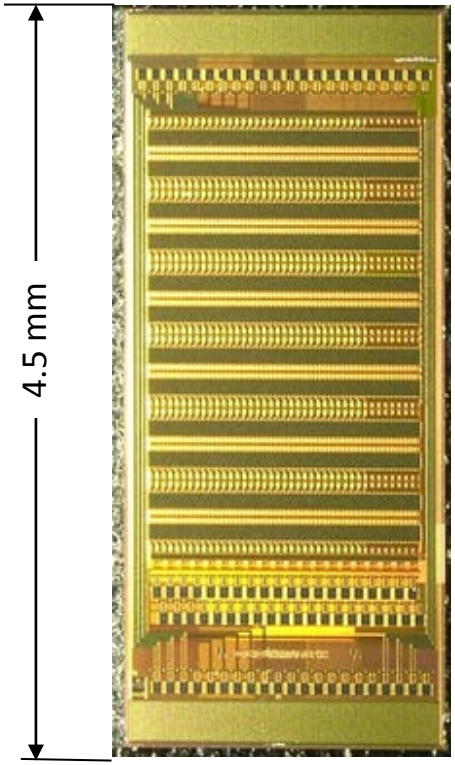
Something Better: Buried n-well

Technology with buried n-well

- Better isolation for p-type transistors (lower cross-talk)
- Less capacitance of detecting element.



Existing and planned Silicon



CCPDv1
11/2011

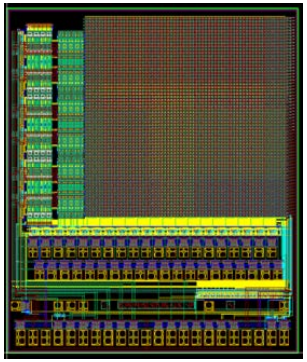
CCPDv2
11/2012

Several technology vehicle submissions.

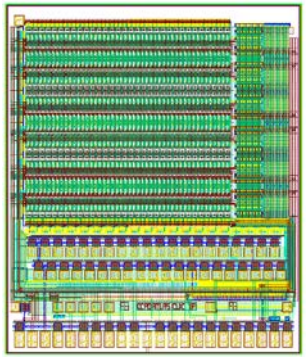
- Lab test.

Prototype CPPD modules in H180 AMS

- Test beam results in the next slides
- Dies photos and dimensions below



CCPDv3/CLICPI
X
11/2013

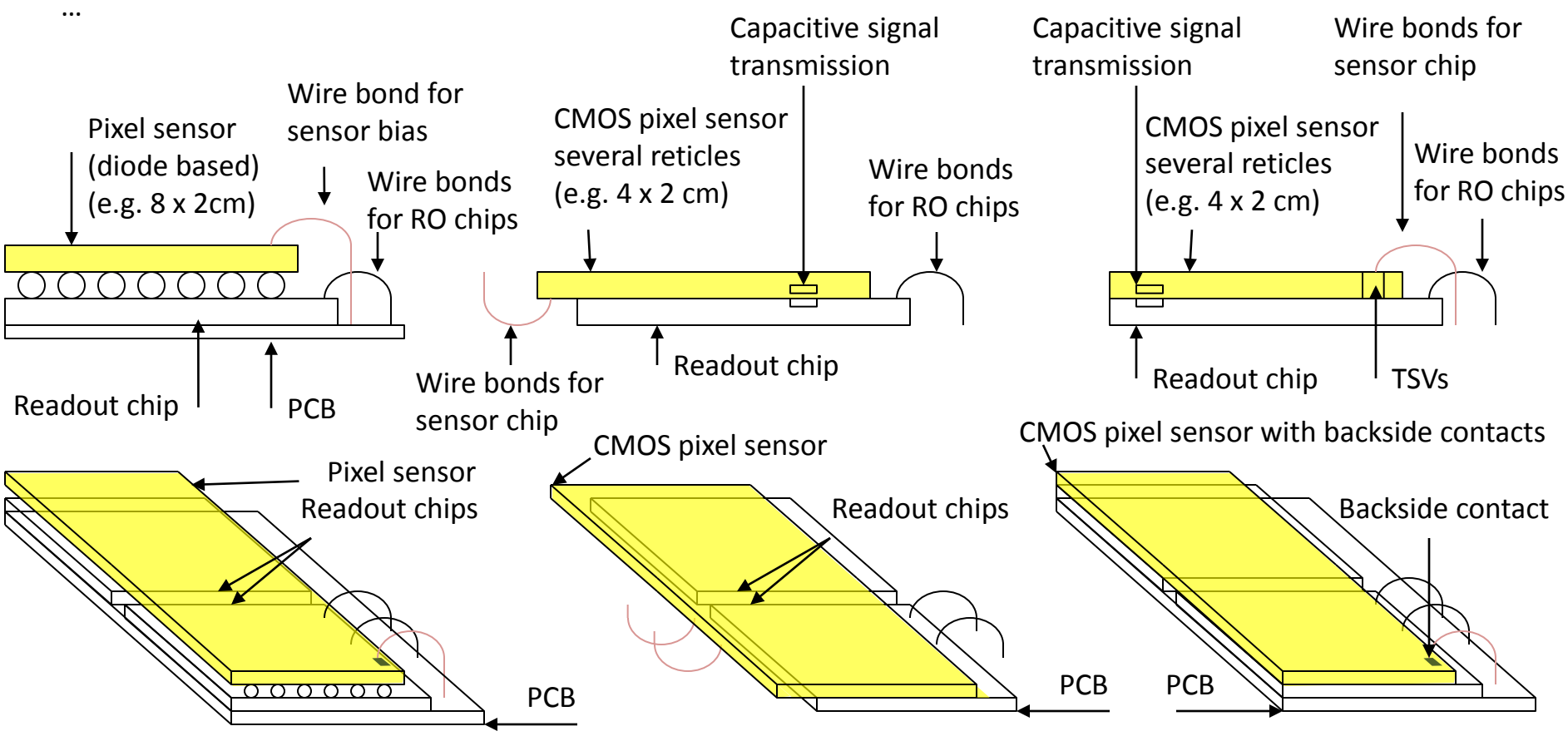


CCPDv4
6/201

ATLAS working on HV/HR-CMOS demonstrators – silicon by end 2015

- Pixel modules with FE-I4 having reasonable size (1÷2 cm^2)
- Designs undergoing on 5 technologies / 4 foundries
- Qualification for ATLAS: >50 Mrad (TID) and 1x10^{15} neq/cm^2 (NIEL), eff.>95%

Pixel Detectors – How put things together



Detector as it is done now:
Diode based pixel sensor bump-bonded to readout ASICs

Present development:
CMOS pixel sensor capacitively coupled to readout ASICs

With TSVs CMOS pixel sensor with backside contacts capacitively coupled to readout ASICs

Why not Proximity Transmission?

The HV-CMOS, differently from a passive sensor, has internally digital elements to configure (amplifiers settings, discriminator threshold).

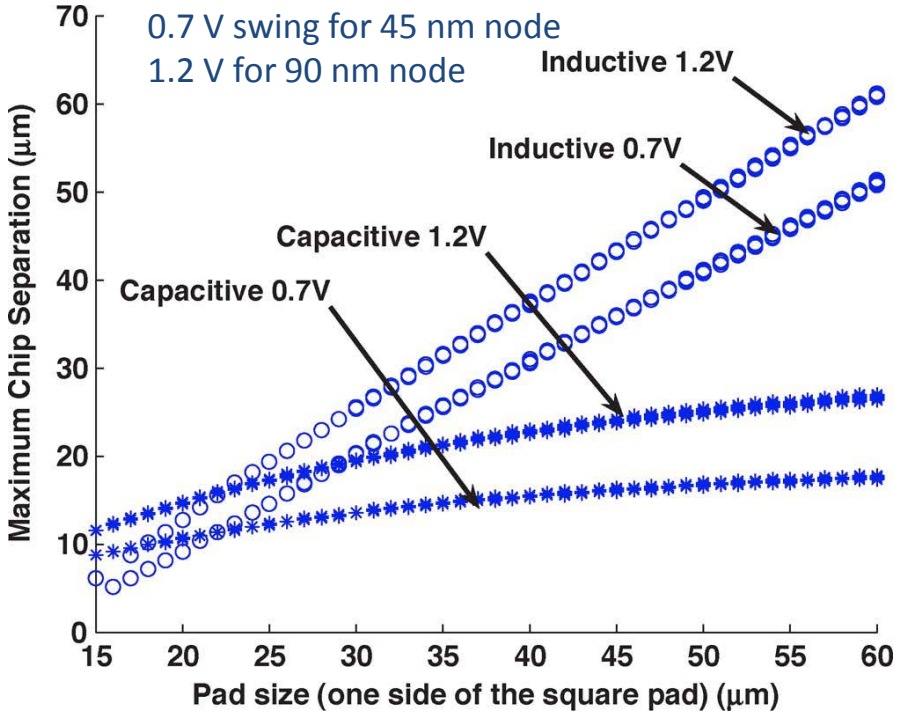
For CCPD looks natural to transmit from HV-CMOS to R/O chip by proximity

- A lot of work exist in this field using inductive and capacitive coupling

This could used instead of TVS (Through Silicon Vias) for all the configuration signals lines.

Remains to find a solution for power and ground:

- TAB bonding? Conductive glue?



Arka Majumdar et al. [Ref.6]

From CCPDv2

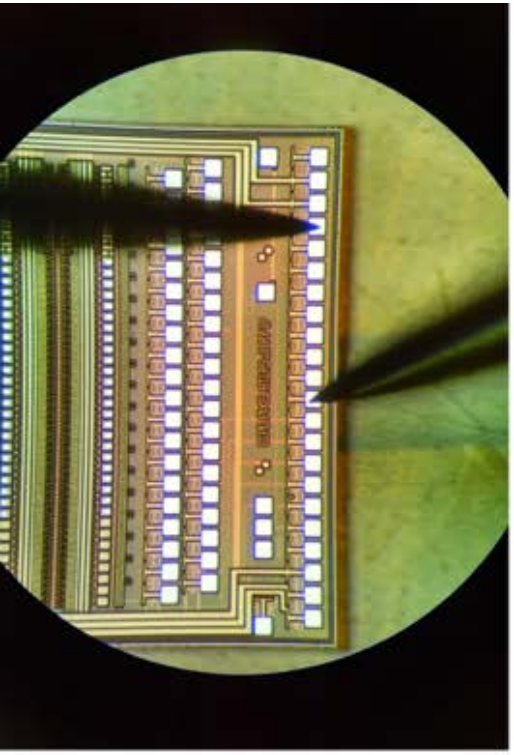
EXPERIMENTAL RESULTS

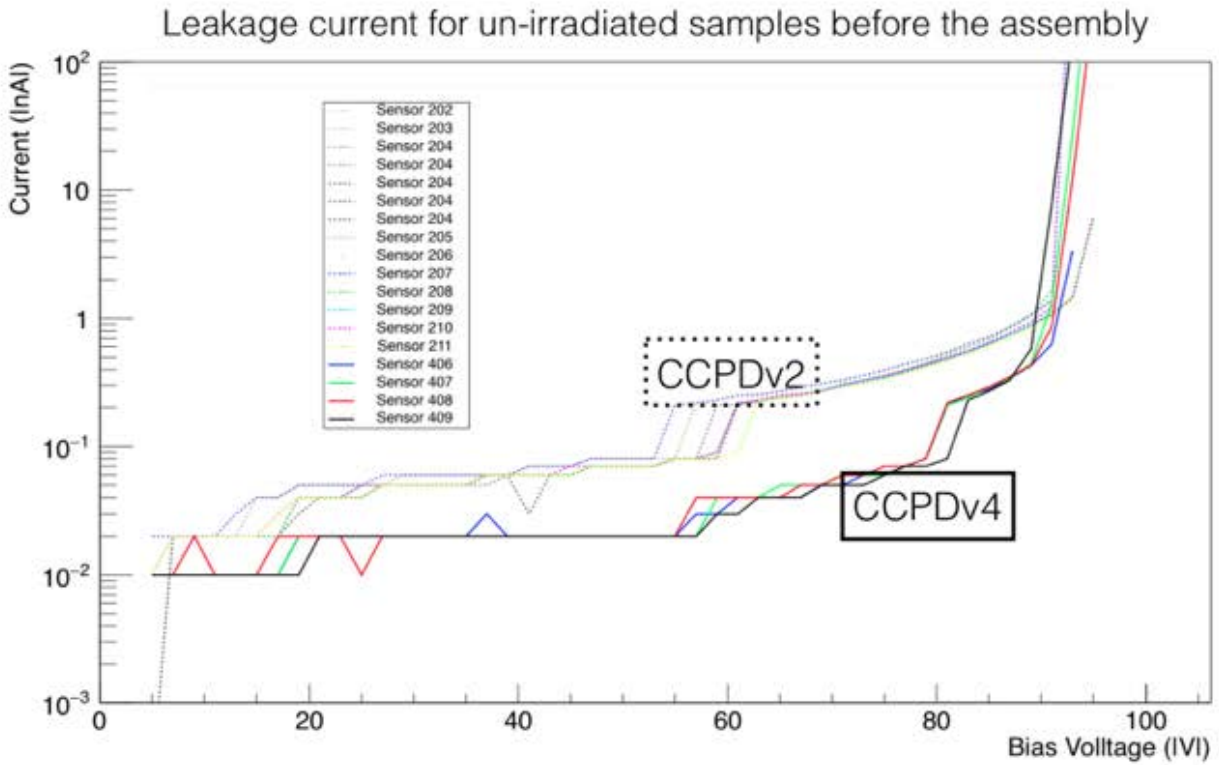
IV Curves

Example of IV curves for CCPD chip (AMS H180 technologies)

- operational currents are below 1nA
- Probed only HV and GND pads

Reminder: AMS H180 technology has low resistivity substrate – 10÷30 µm depletion @100 V

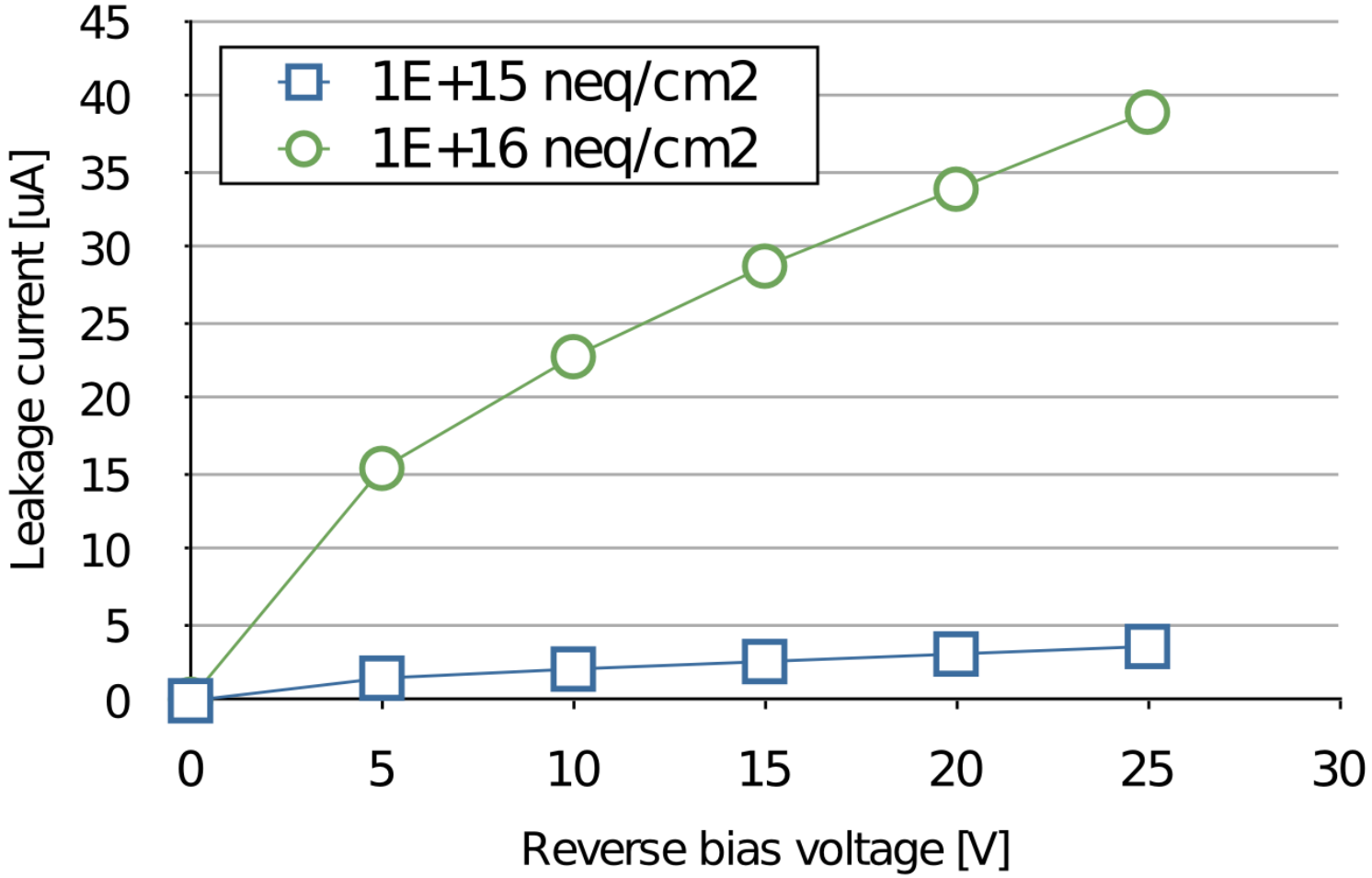




© M. Caloz @ 10-th "Trento" Workshop, 2015.

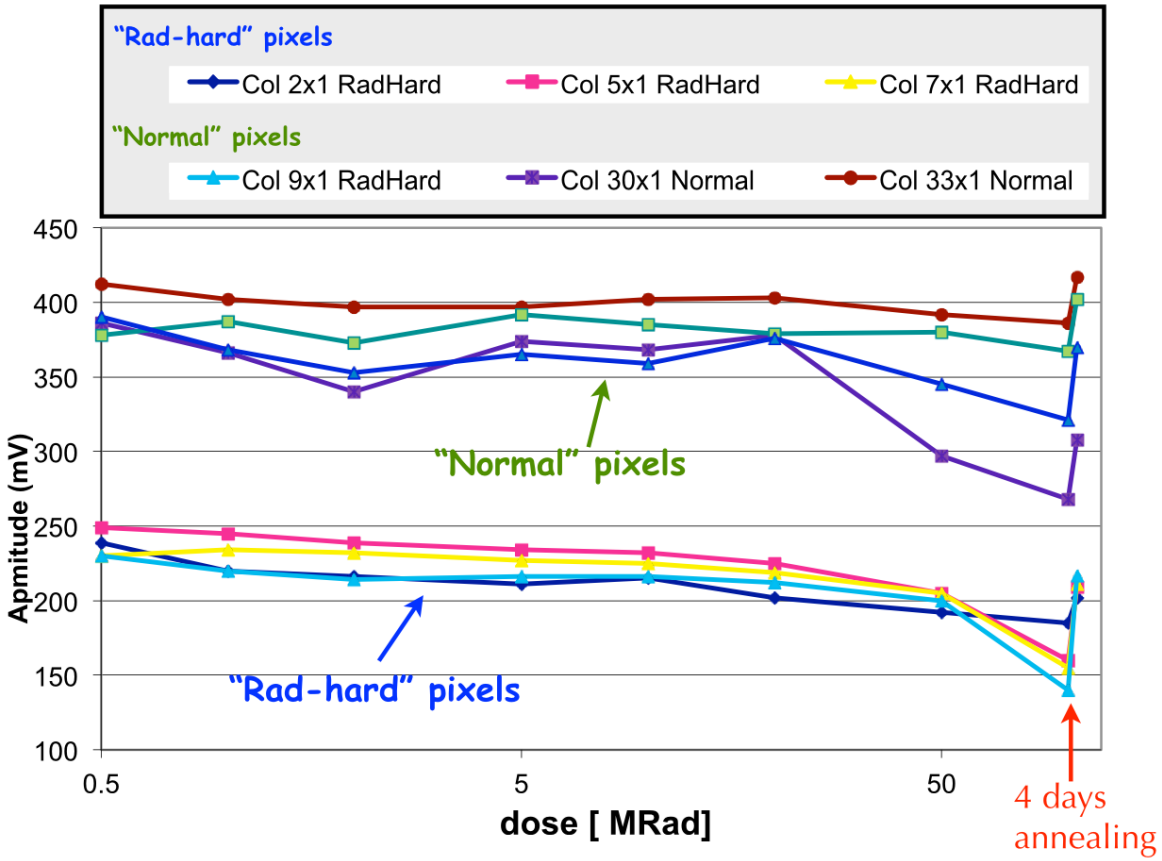
CCPDv2 IV after Irradiation

IV after neutron irradiation, up to 10^{15} $n_{eq}cm^{-2}$ and 10^{16} $n_{eq}cm^{-2}$, measurements at room temperature



A.Miucci et al. IWORID2013 [Ref.5]

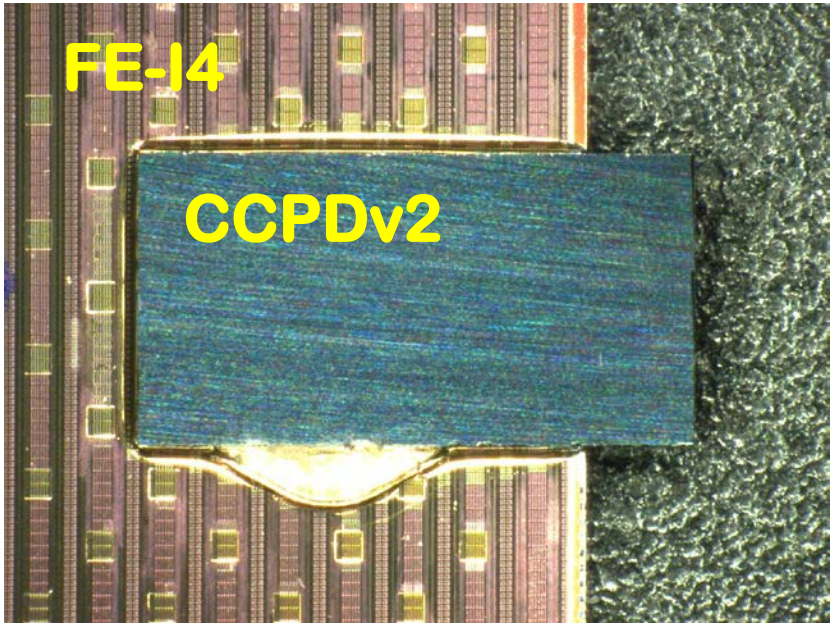
Pulse amplitude at the preamplifier out for 1 V injected-pulse after X-ray irradiation up to 100 MRad of a CCPDv2 prototype chip

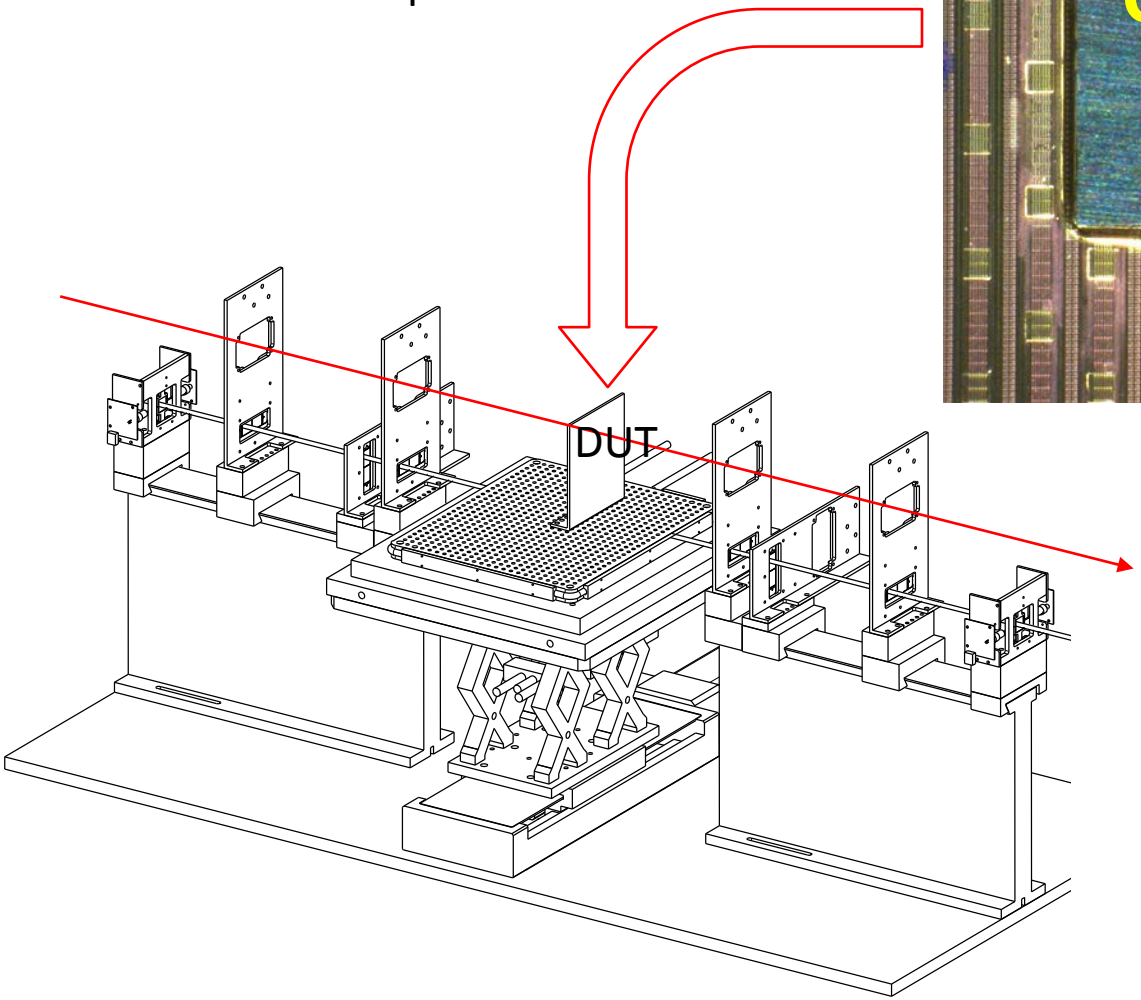


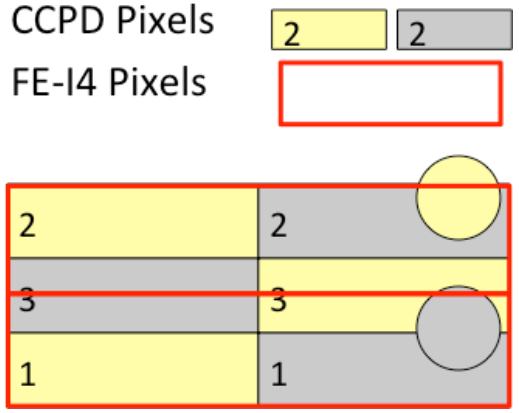
A.Miucci et al. IWORID2013 [Ref.5]

Test Beam Results - Efficiency

CCPDv2: 32 x 24= 576 pixels
Readout by:
12 x 16 = 192 FE-I4 pixels



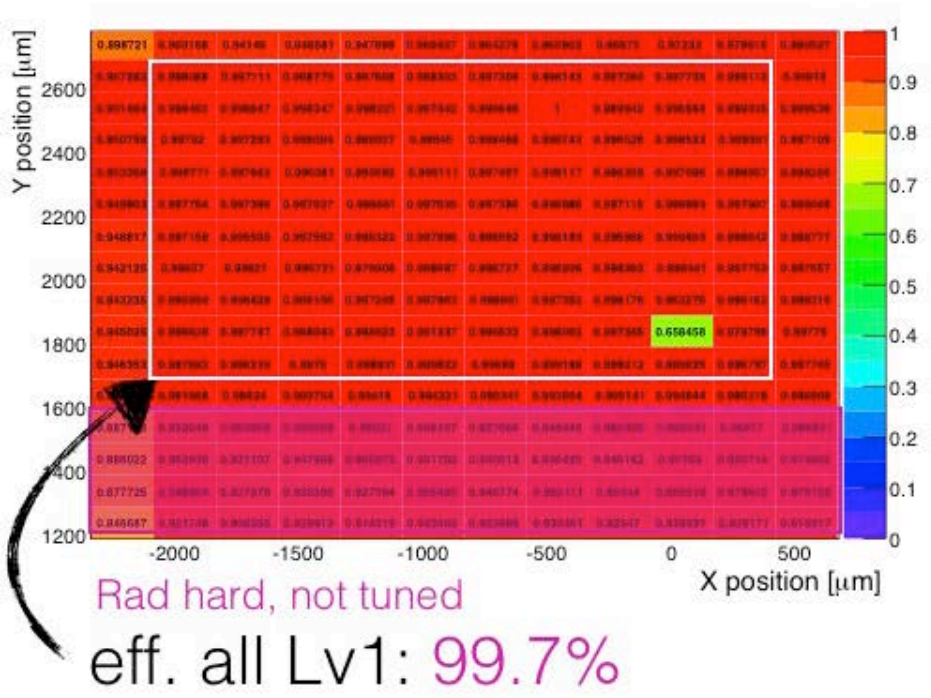


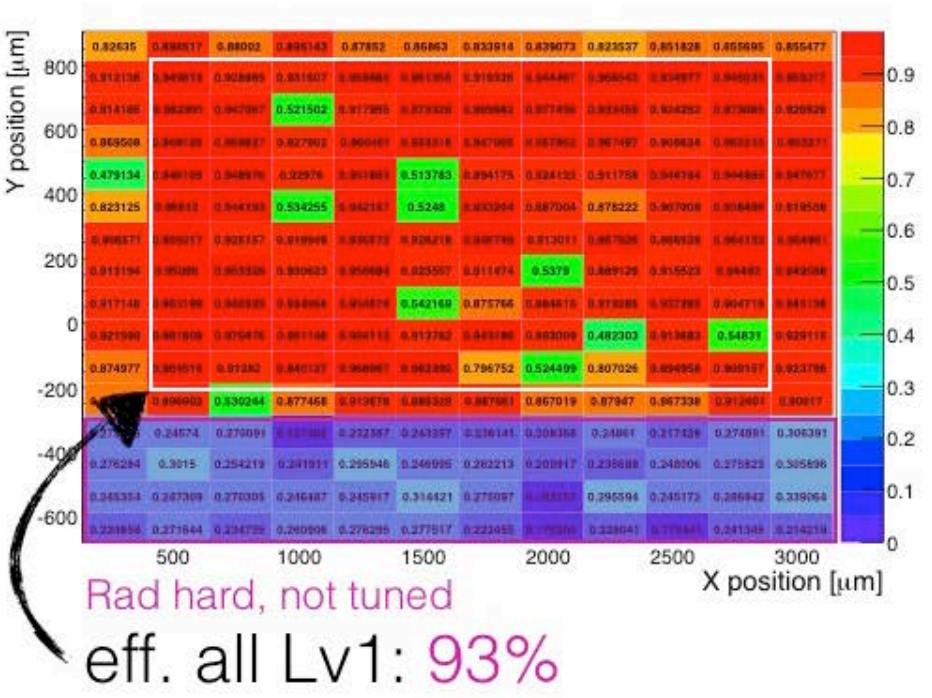


Efficiency Map

Efficiency of unirradiated and irradiated CCPDv2

- Global efficiency recorded by 12 x 16 FE-I4 pixels





Not irradiated
CCPD V_{bias} = 90 V

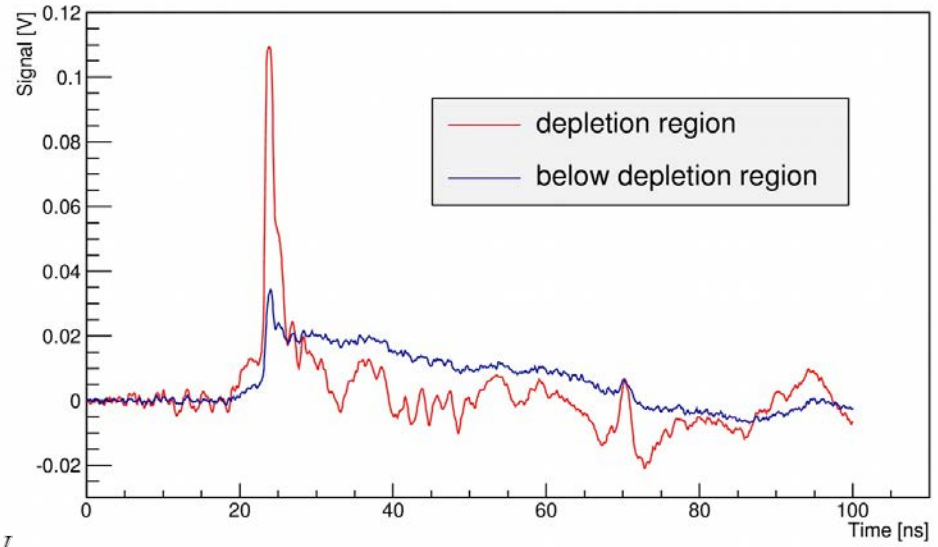
Irradiated to 10^{15} n_{eq}/cm^2
CCPD V_{bias} = 80 V

© Javier Bilbao de Mendizabal, Trento Workshop, 2015

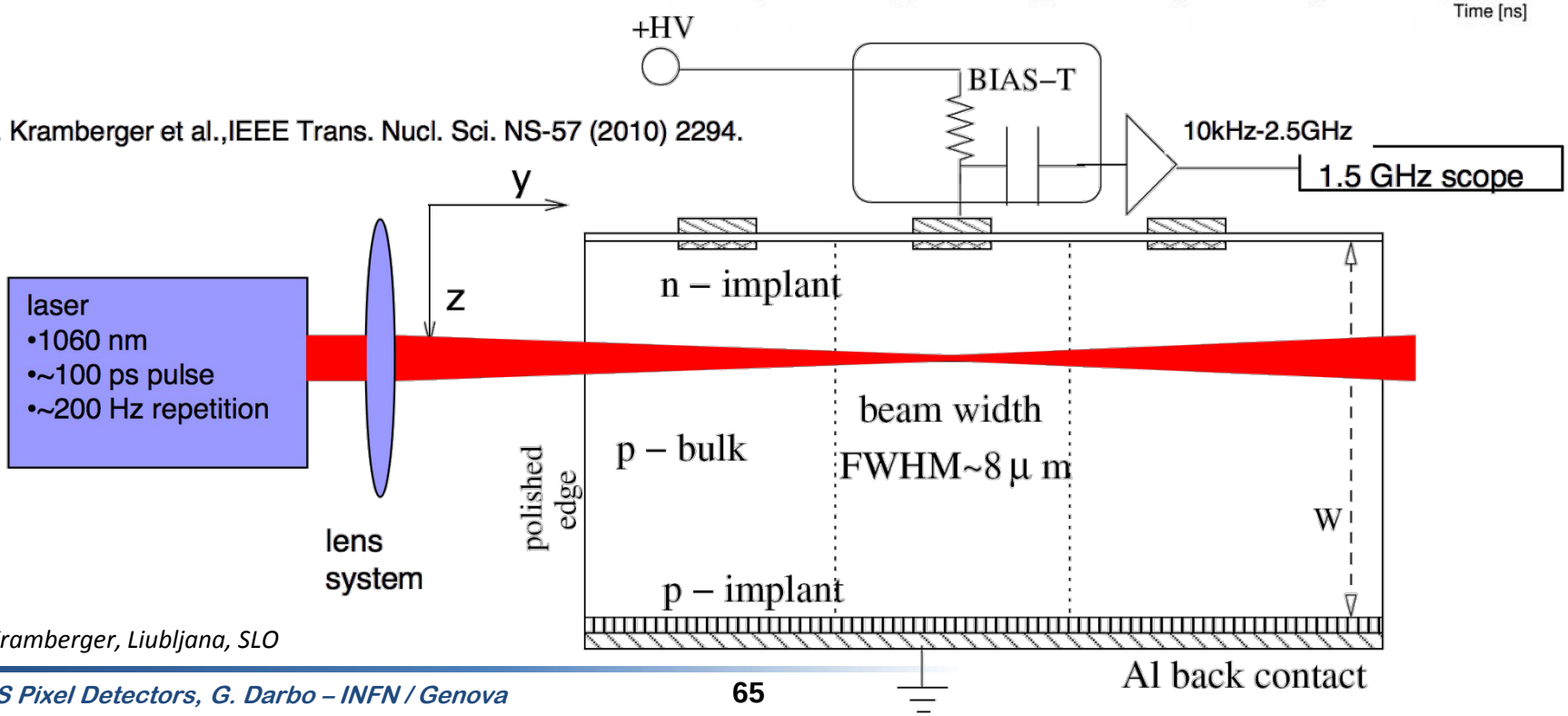
Transient Current Technique (TCT)

TCT: Transient Current Technique, i.e. observe the time-resolved charge collection generated by MIP, alpha or **laser pulse**

- Fast current contribution: collection by drift
- Slow current contribution: collection by diffusion

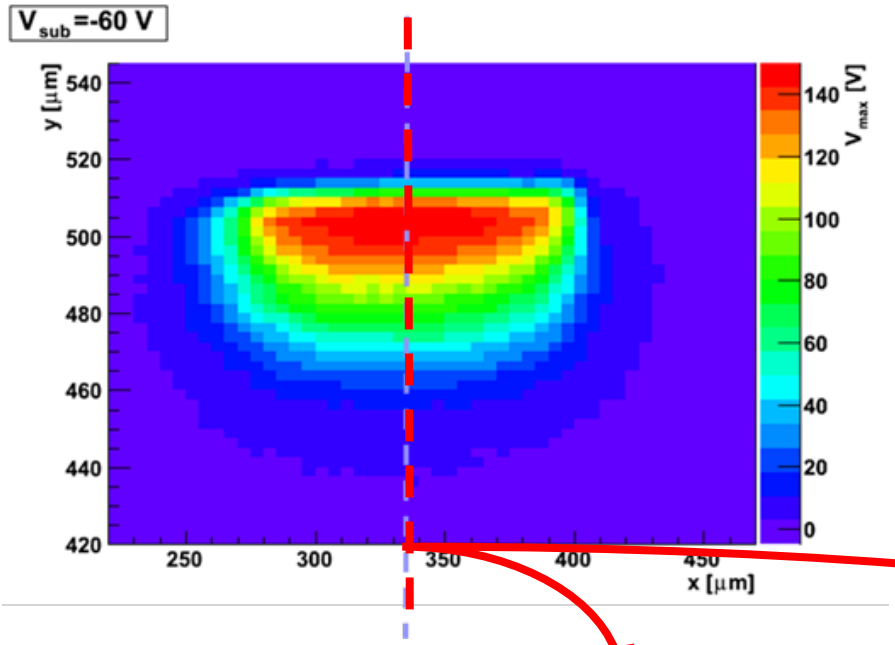


G. Kramberger et al.,IEEE Trans. Nucl. Sci. NS-57 (2010) 2294.



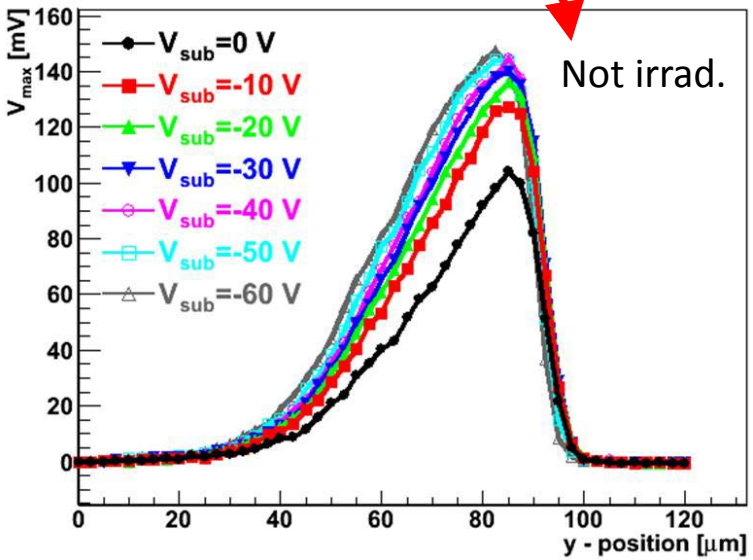
© G. Kramberger, Liubljana, SLO

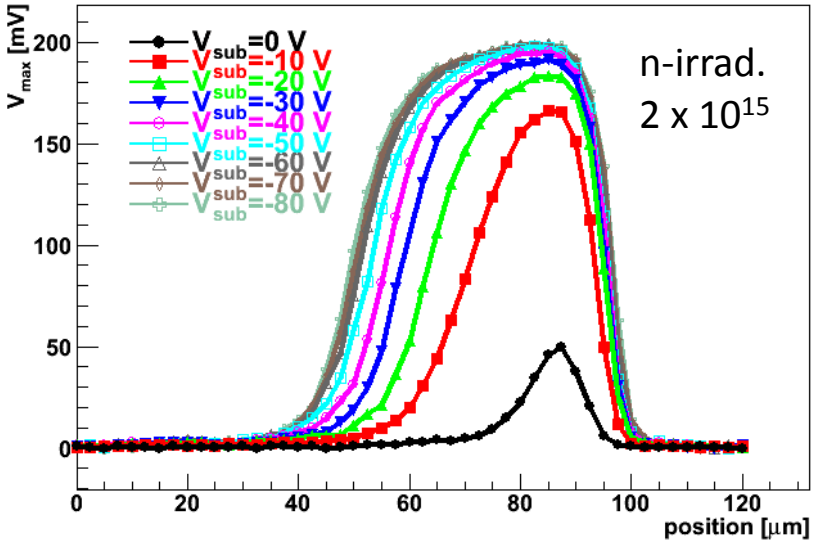
TCT: Results on CCPDv2



Measure the output of pre-amplifier:

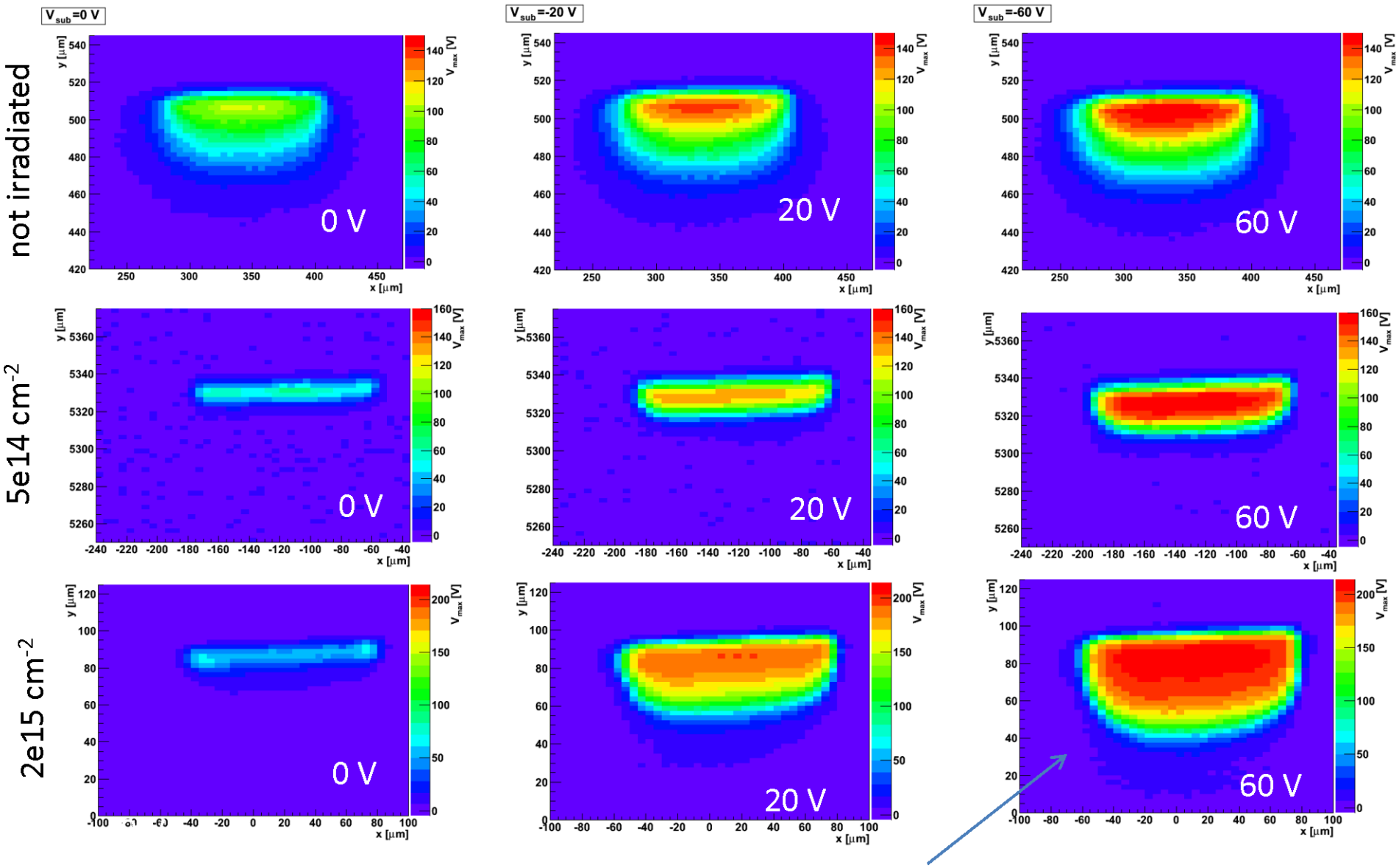
- Measure V_{MAX} at the amplifier output as function of the X,Y position of the laser
- Charge is collected by diffusion + drift before irradiation slow slope, and mainly by drift after heavy irradiation
- Depletion depth (surprisingly) increases after irradiation - interpretation as donor removal





© G. Kramberger, Trento Workshop, 2015

Edge-TCT, CCPDv2, irradiated with neutrons



Charge collection region **larger** at high fluence

© I. Mandić, Trento Workshop, 2015

Conclusion

HV-CMOS are a (relatively) new in detector technology

- Specially with HR substrate and used for CCPD
- HV-CMOS detectors are still in the infancy but with big promises
- ATLAS is serious about them and demonstrators will be available in 2015
- They could be a cheap alternative to hybrid pixel detectors for the upgrades of ATLAS and CMS at the HL-LHC.

References

BOOKS

a. *H. Spieler, **Semiconductor Detector Systems**, Oxford University Press, 2005*

b. *L.Rossi, T.Rohe, P.Fischer and N.Wermes, **Pixel Detectors - From Fundamentals to Applications**. Springer, 2006.*

c. *G. Lutz, **Semiconductor Radiation Detectors - Device Physics**. 1st ed. Springer, 2007*

ARTICLES AND PROCEEDINGS

1. *E.Gatti and P.Rehak, **Semiconductor drift chamber: An application of a novel charge transport scheme**. Nuclear Instr. and Meth. in Physics Research 225, 3 (9 1984), 608–614.*
2. *J.Kemmer and G.Lutz, **Low capacitive drift diode**. Nucl. Instr. & Meth. A253 (1987) 378-381*
3. *R.Turchetta et al., **A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology.** Nuclear Instr. and Meth. in Physics Research A 458, 3 (2001), 677–689.*
4. *L.Blanquart, A.Mekkaoui, V.Bonzom, and P.Delpierre. **Pixel analog cells prototypes for ATLAS in DMILL technology**. Nucl. Instr. and Meth. A 395 (1997) 313–317.*
5. *A. Miucci et al. **Radiation-hard active pixel sensors for HL-LHC detector upgrades based on HV-CMOS technology**. JINST 9 (2014) C05064.*
6. *Arka Majumdar et al. **Alignment and Performance Considerations for Capacitive, Inductive, and Optical Proximity Communication**. IEEE TN ON ADVANCED PACKAGING, VOL. 33, NO. 3, AUGUST 2010.*

CONFERENCES AND WORKSHOPS (most recent)

- *CPIX2014 – Workshop on CMOS Active Pixel Sensors for Particle tracking, 15-17 Sept 2014, Bonn, Germany. http://cpix14.org*
- *10th "Trento" Workshop on advanced Silicon Radiation Detectors, 19-21 Feb 2015, Trento, Italy. http://indico.cern.ch/event/351695/*

BACKUP SLIDES

MAPS R/O - CDS

The principle of a CDS shaper is shown in Figure. Input signals are superimposed on a slowly fluctuating baseline.

To remove the baseline fluctuation signal is sampled at beginning and after integration time. Pedestal is then subtracted to signal.