# MONOLITHIC PIXEL DETECTORS FOR HIGH ENERGY PHYSICS

Walter Snoeys

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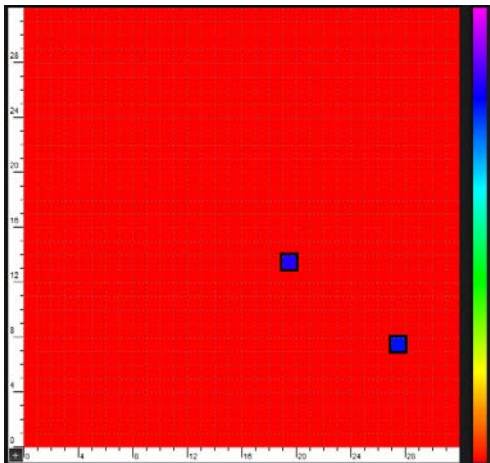
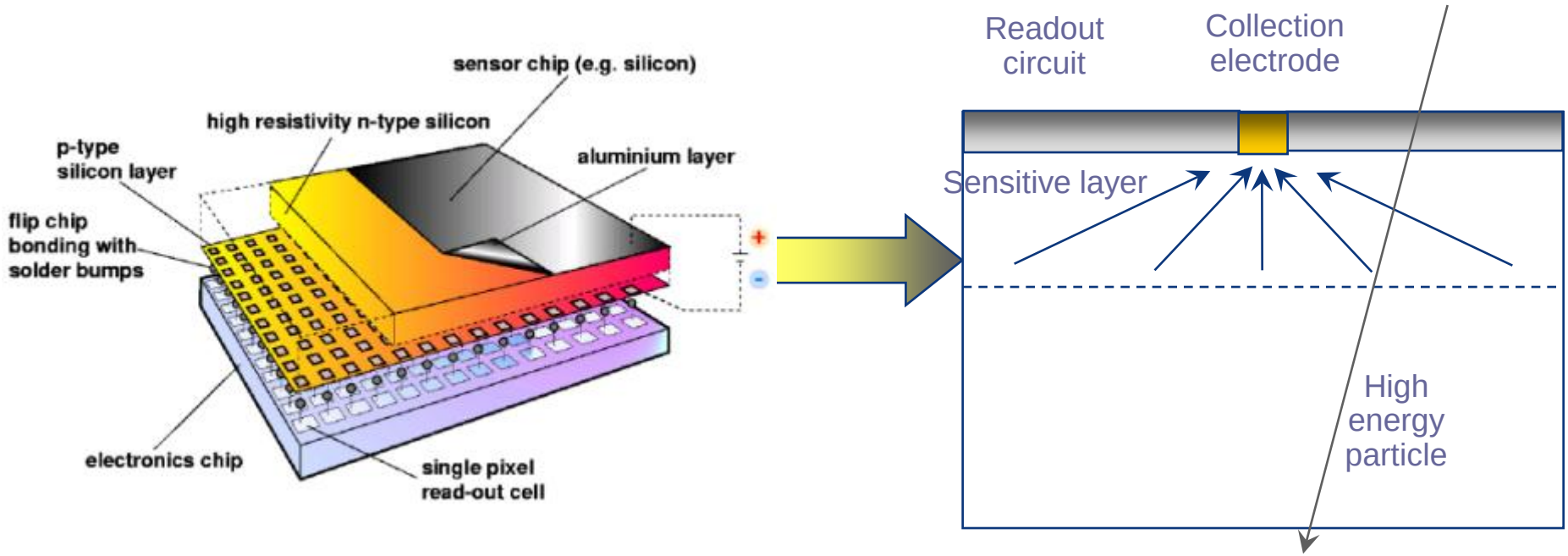


# MONOLITHIC DETECTORS: DEFINITION




Integrate the readout circuitry – or at least the front end – together with the detector in one piece of silicon

The charge generated by ionizing particle is collected on a designated collection electrode

# MONOLITHIC DETECTORS

- Motivation:
  - Easier integration, lower cost, possibly better power-performance ratio
  - Promising not only for pixel detectors, but also for full trackers
  - Potential of strong impact on power consumption and hence on material in high energy physics experiments

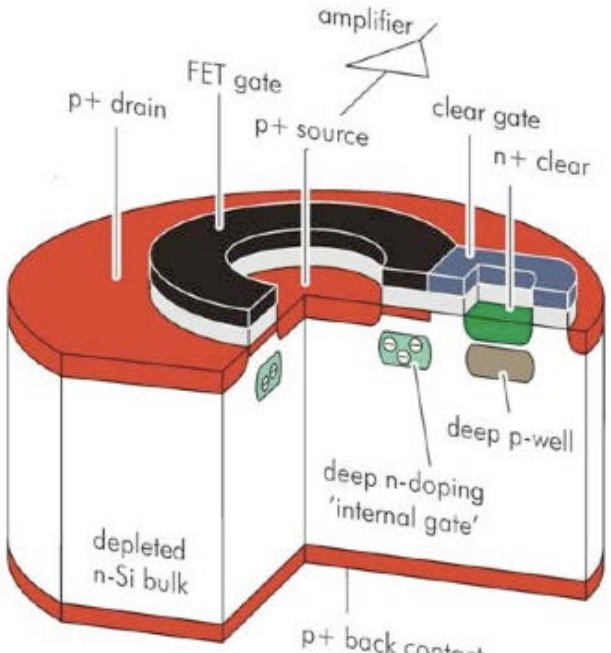
- Difference between high energy physics and traditional imaging:
  - single particle hits instead of continuously collected signal

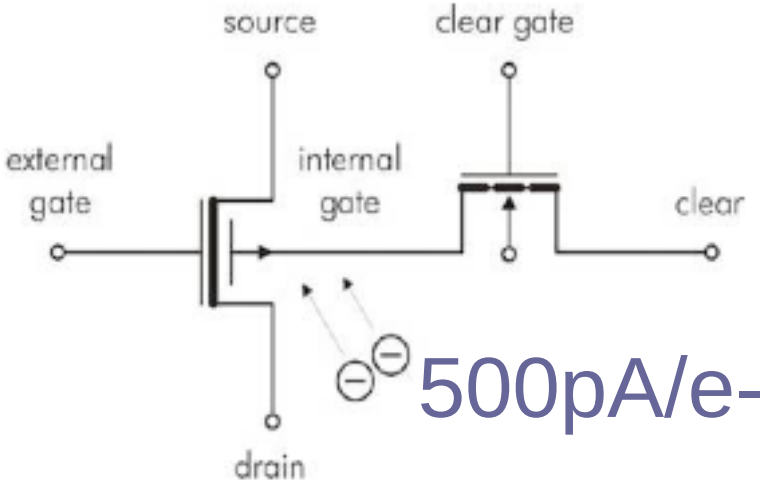
- Now in two experiments:
  - DEPFET pixels in Belle-II
  - MAPS in STAR experiment

    both relatively slow (row by row) readout, not always applicable

- Not yet in LHC, adopted for the ALICE ITS upgrade and considered for CLIC/ILC

# DEPFET (MPI MUNICH)
# an example of a special technology

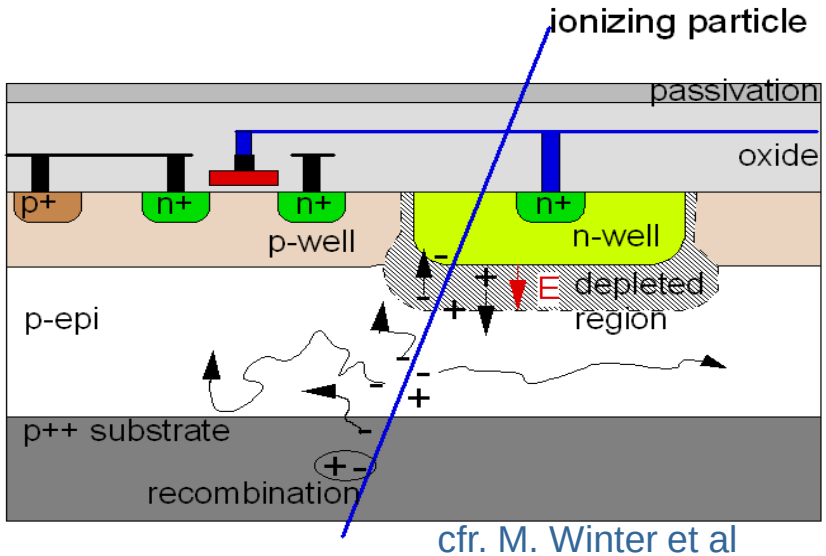



500pA/e-

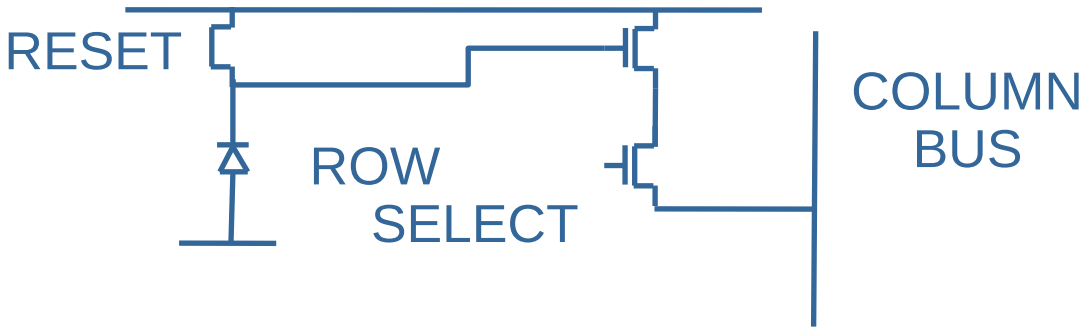
- An annular PFET on top of a fully depleted substrate (back side junction).
- A potential well under the gate area collects the charge generated in the substrate.
- The potential of this potential well changes with collected charge and modulates the PFET source-drain current.
- Charge collection continues even if DEPFET is switched off.
- Clear gate allows reset of the potential well.
- The readout can occur via the source (voltage out), or via the drain (current out)
- Very small collection electrode capacitance, allows high S/N operation.
- Need steering and rest of readout off chip or on another chip.

# MONOLITHIC ACTIVE PIXEL SENSORS (MAPS)




cfr. M. Winter et al

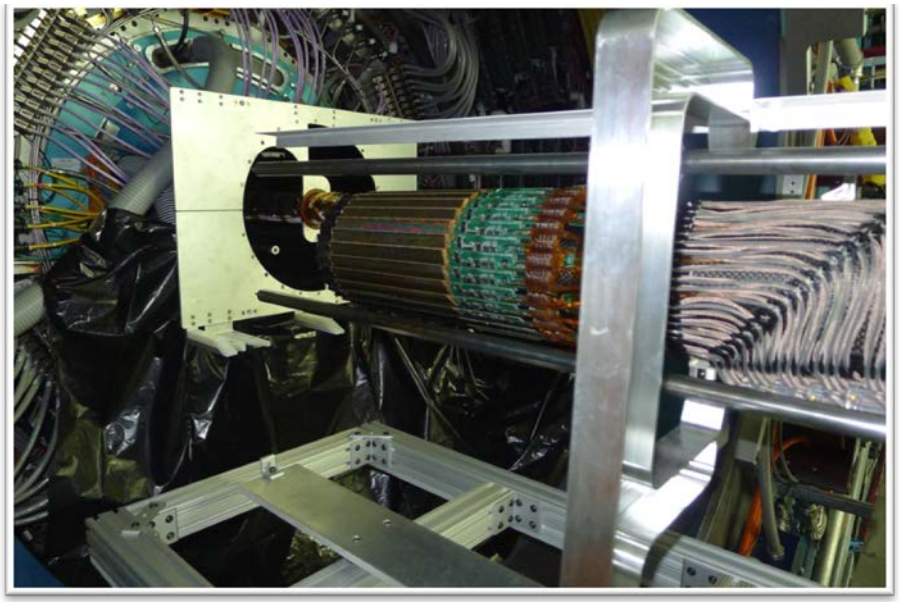
- Commercial CMOS technologies
- Very few transistors per cell
- Pixel size : 20 x 20 micron or lower
- Charge collection by diffusion, more sensitive to bulk damage (see next slides)
- Serial readout, slower readout
- Time tagging can be envisaged but would like to have faster signal collection, and will need extra power.

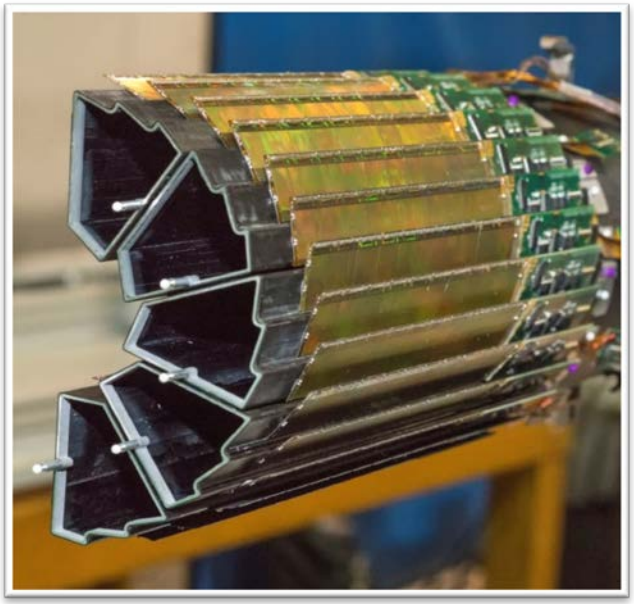


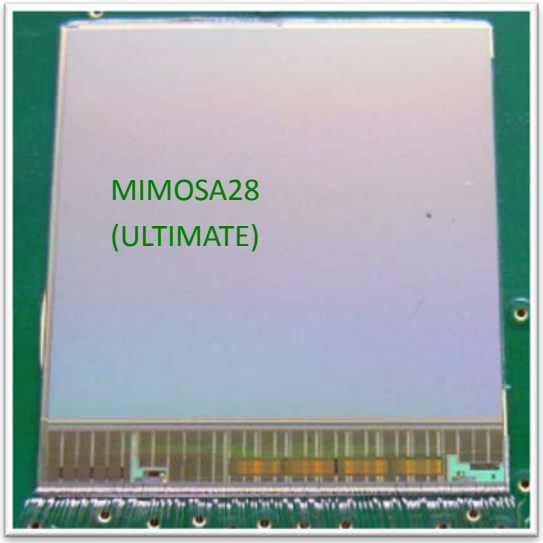

Example: three transistor cell

# MAPS SENSOR CHIP in STAR experiment

Data taking March-June 2014








First MAPS system in HEP

MIMOSA28 (ULTIMATE) chip
IPHC Strasbourg :

- Twin well 0.35 µm CMOS
- High resistivity (> 400 Ωcm) 15 µm epi
- Readout time 190 µs
- TID 150 krad
- NIEL few $10^{12}$ 1 MeV $n_{eq}/cm^2$

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# MONOLITHIC SENSORS

Main challenge for improvement:

need combination of:

- tolerance to displacement damage (depletion)
- very low capacitance collection electrode or high Q/C
- integration of complex circuitry without efficiency loss
- keep using commercial technology

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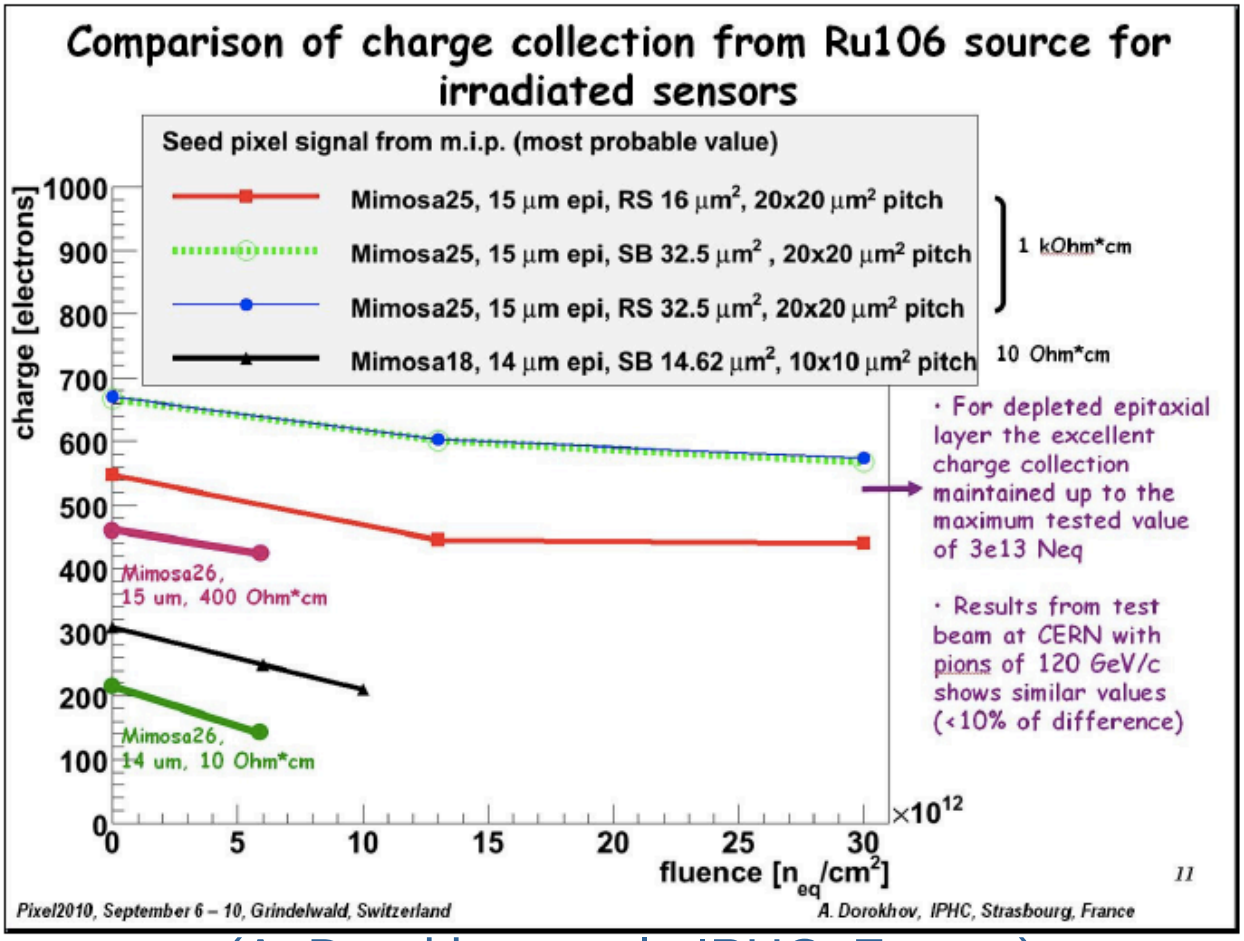
# Collection by diffusion : ex standard MAPS

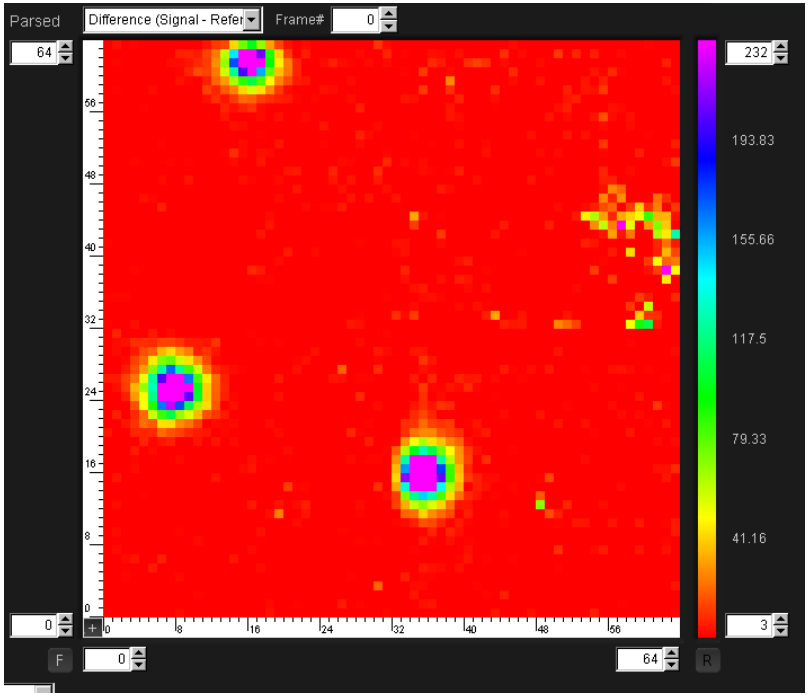


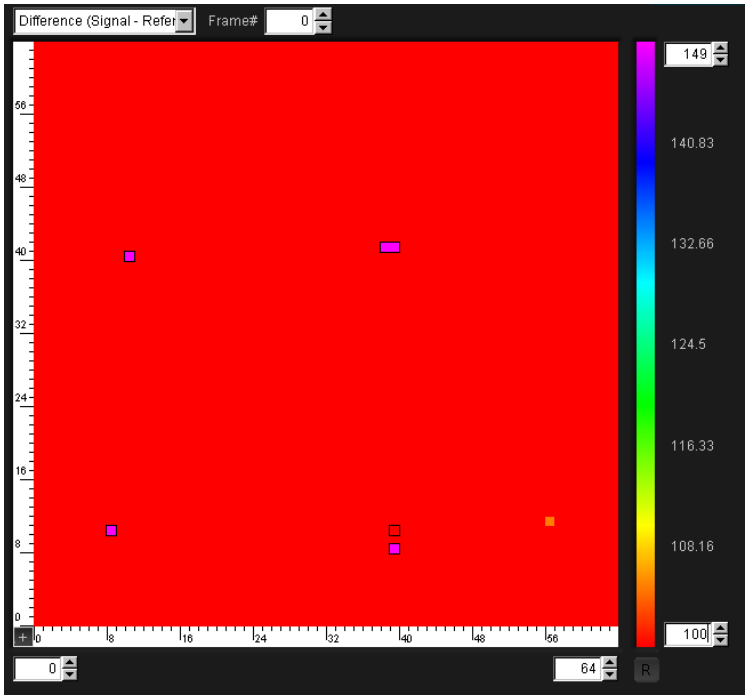

(A. Dorokhov et al., IPHC, France)

Need collection by drift for radiation tolerance beyond a few $10^{13} n_{eq}/cm^2$ !

# Drift vs diffusion- influence on cluster size

Measurement on LePIX prototypes (50x50 micron pixels !)



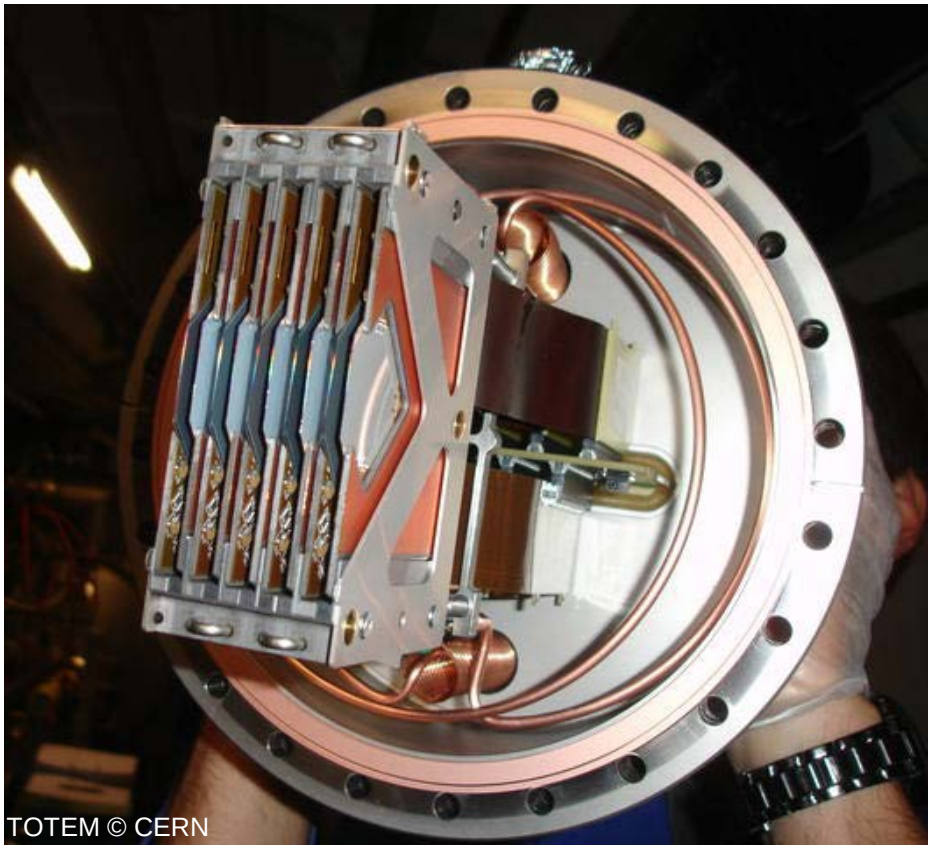

0 Volts bias

60 Volts bias

- *Diffusion:* at zero bias, incident protons generate on average clusters of more than 30 50x50 micron pixels.
- *Drift:* for significant reverse bias (60V) cluster reduced to a few pixels only

# LOW POWER IS KEY TO LOW MASS

- Cables, cooling etc… represent significant fraction of the material in the detector, and material in the tracker has to be minimized
- Limit for future upgrades
- Power consumed at CMOS voltages, so kW means kA

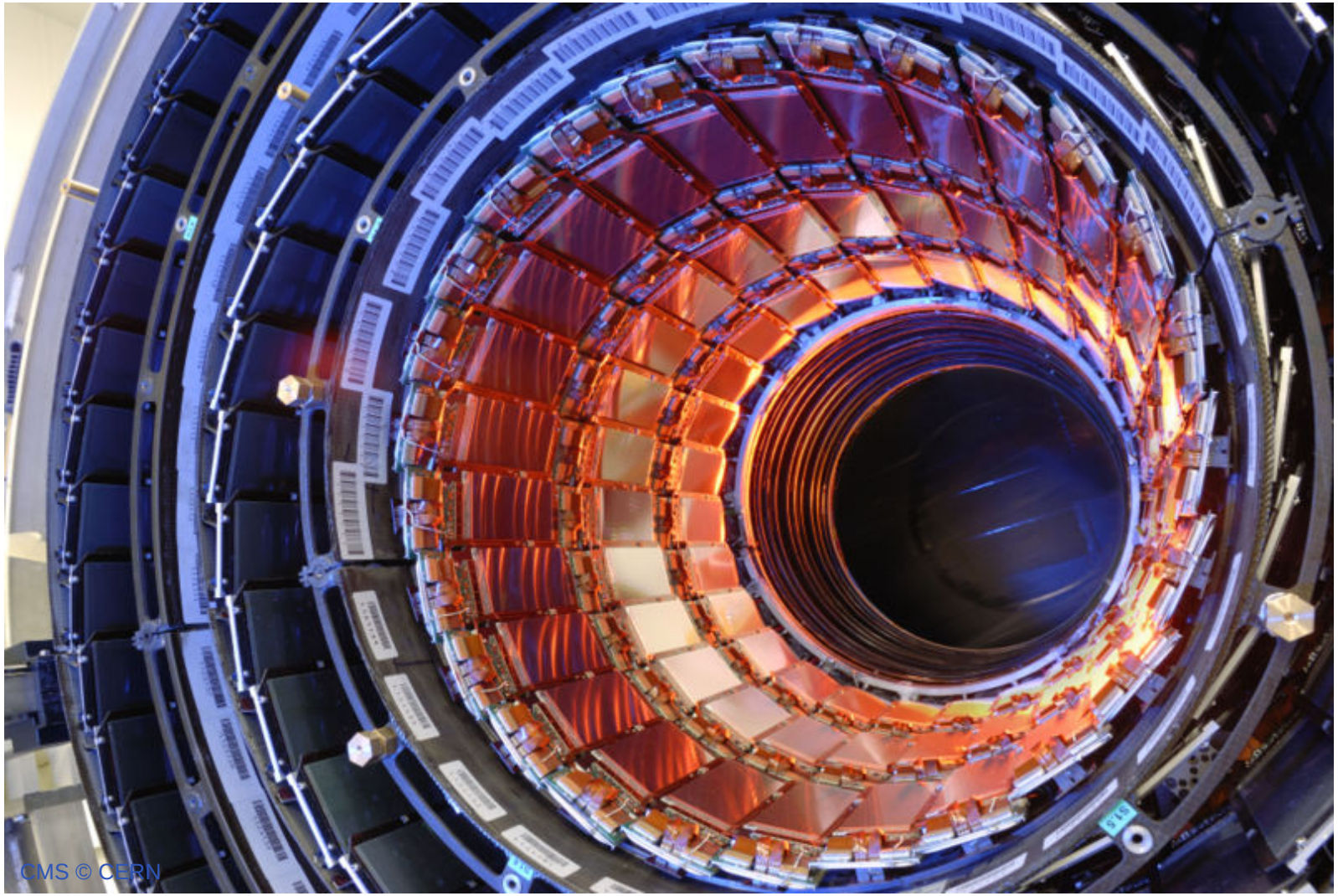



Example, currently installed at LHC:

Roman Pot in the TOTEM experiment:

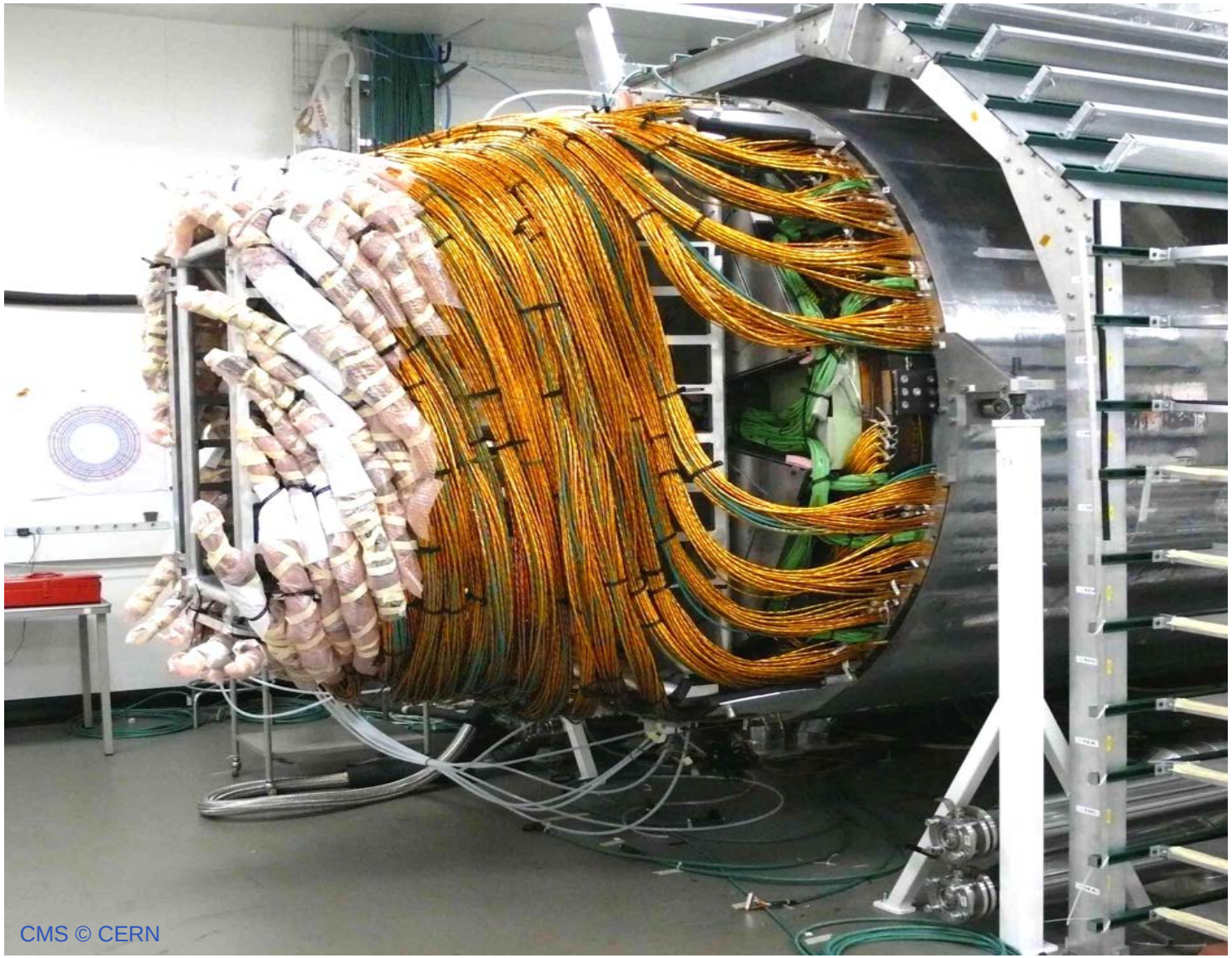
- ~ 6A @ 2.5 V
- ~100m 2x16mm$^2$ cable
- 26kg of Copper for ~ 15 W

# THE CMS TRACKER BEFORE DRESSING

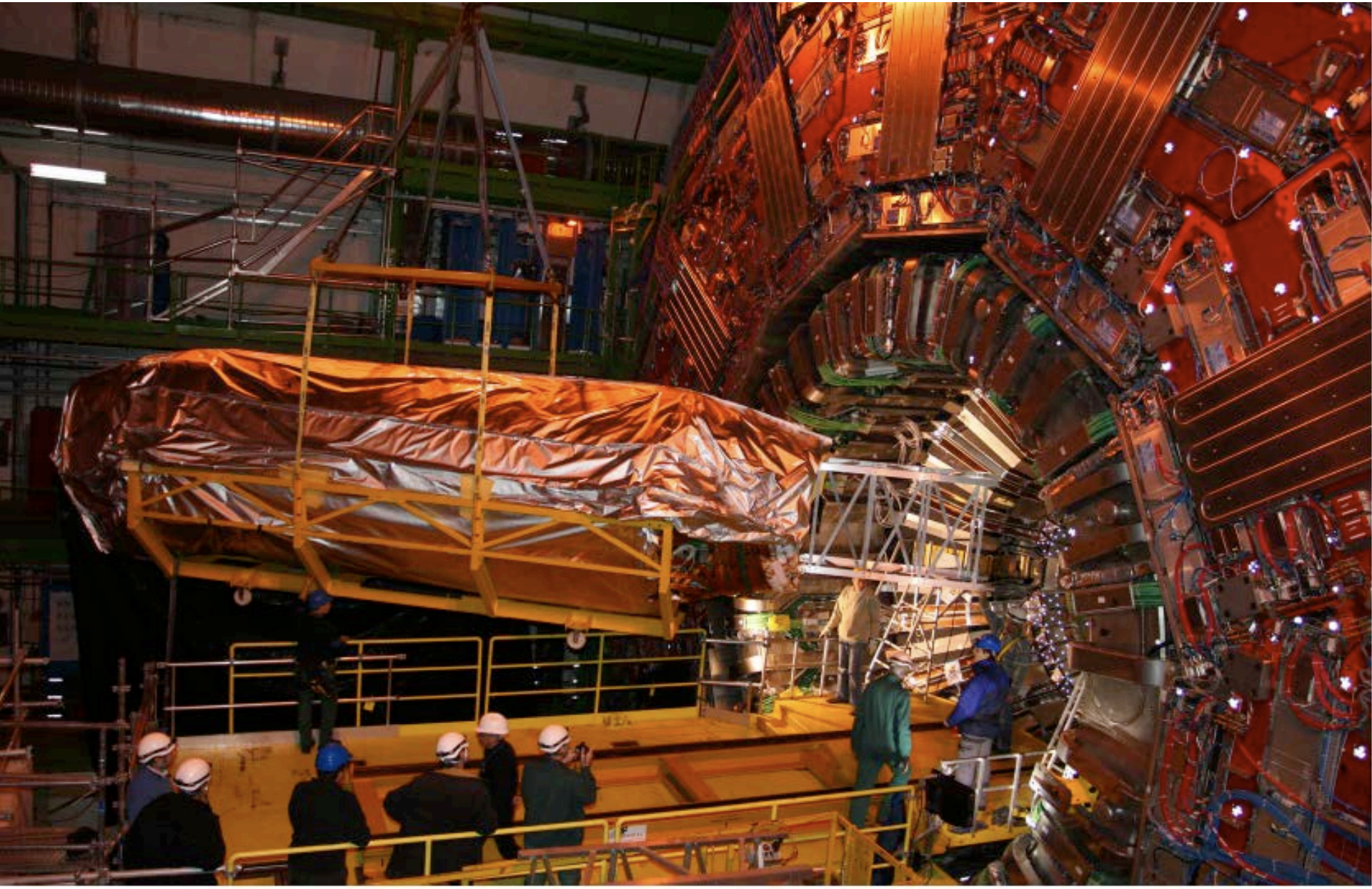


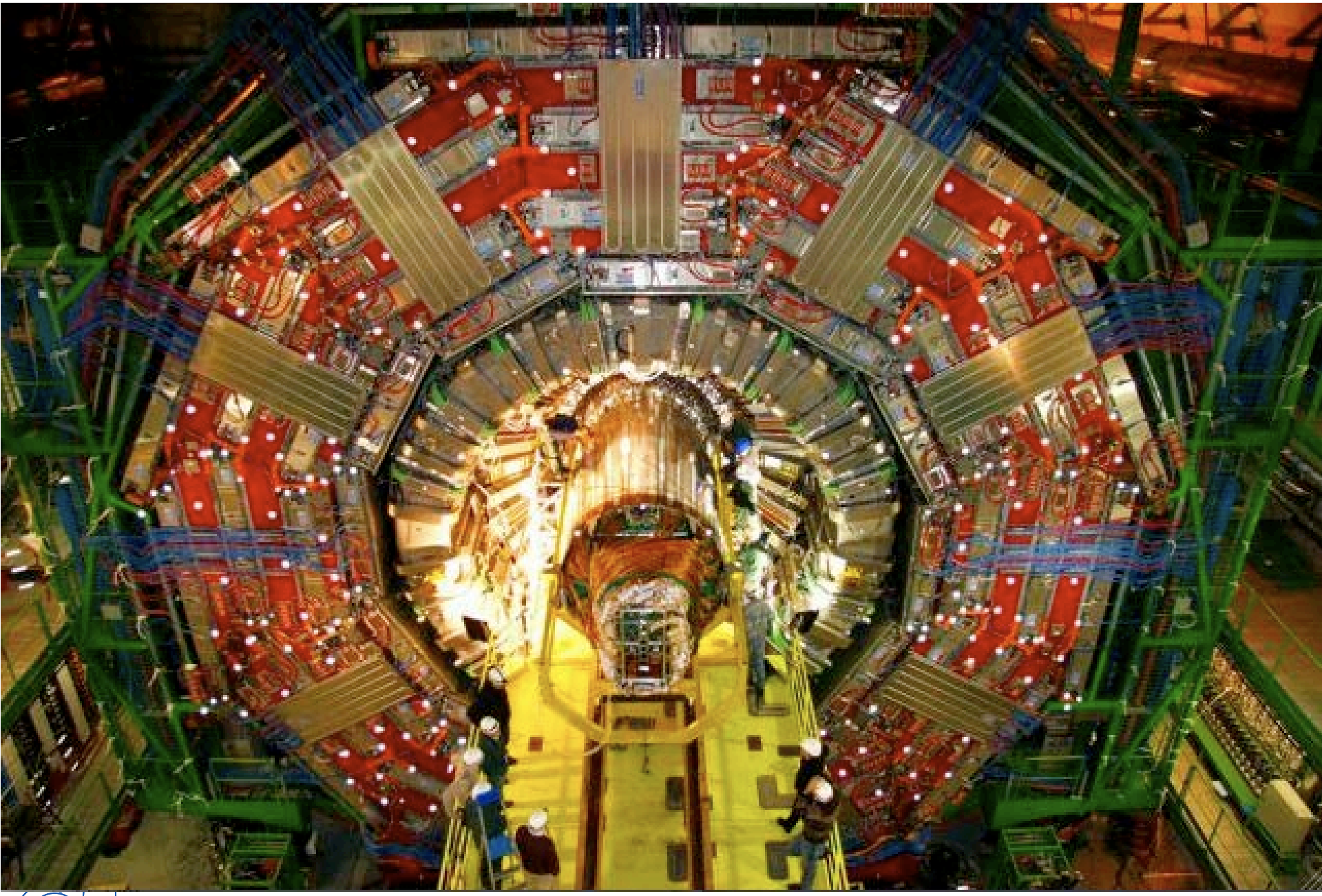

~ 200 $m^2$ of silicon strips

# … AND AFTER

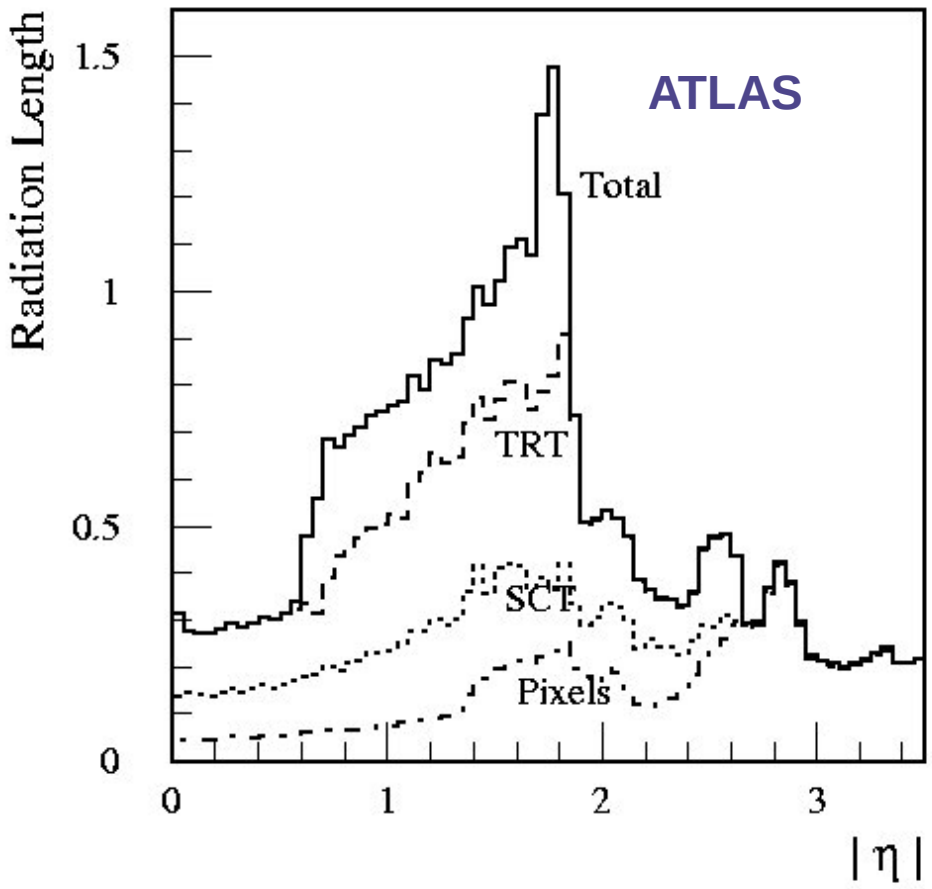


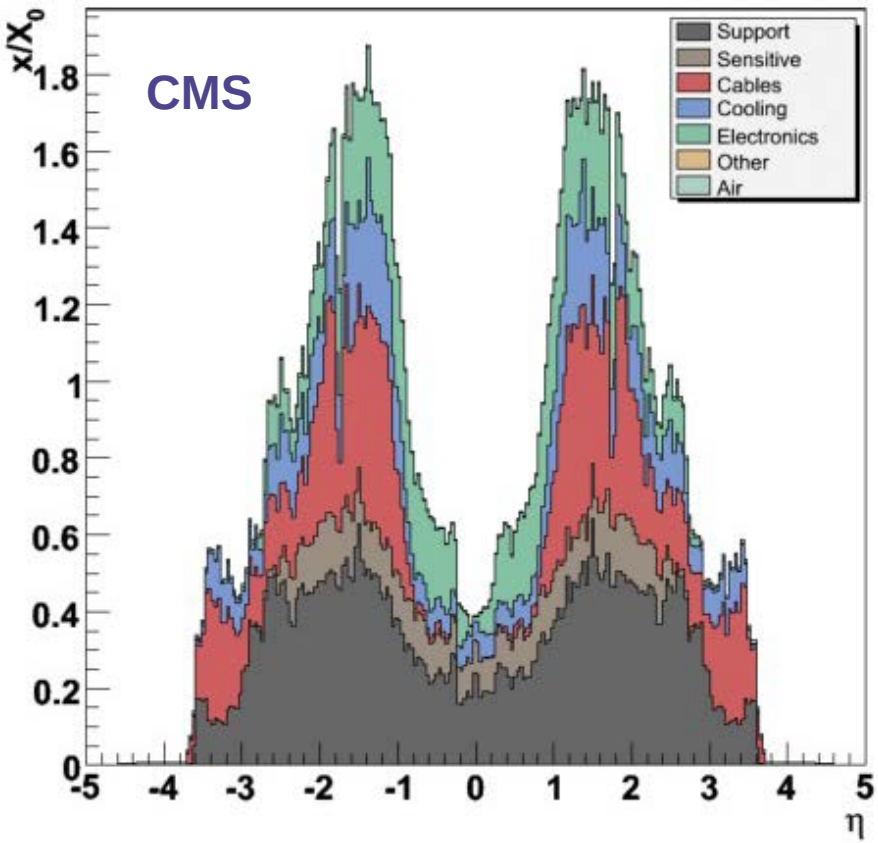

33 kW in the detector … and as much in the cables !





# Tracker power and material budget



# THE ALICE ITS UPGRADE PROJECT

Replace the inner tracking system with an entirely new detector in 2018-2019

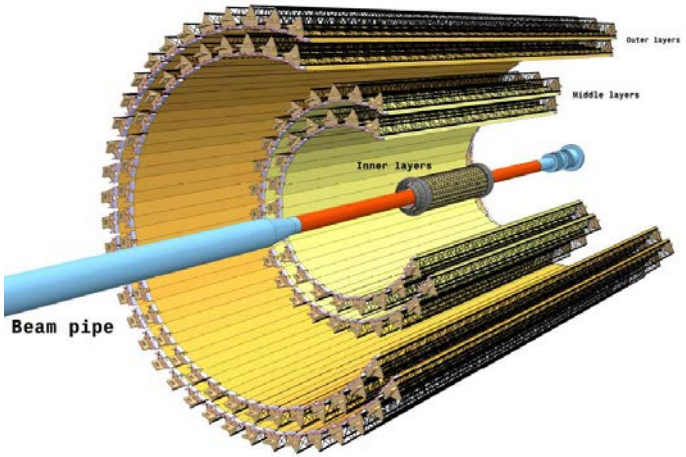
ALICE-TDR-17/CERN-LHCC-2013-024

Improve

- impact parameter resolution by a factor 3 in rφ, 5 in z
- standalone tracking efficiency and $p_T$ resolution at low $p_T$

New Layout 7 layers, 12.5 Gpixels in ~ 10 $m^2$

- $X/X_0$ 0.3 % (innermost layers)
- Pixel size: O(30x30) $\mu m^2$
- Inner layer radius 22 mm




Parameters

- Chip: 15 mm x 30 mm x 50 µm
- Spatial resolution ~ 5 µm
- Power density < 100 mW/$cm^2$
- Integration time < 30 µs
- Max required radiation tolerance : TID 700 krad & NIEL$10^{13}$ 1 MeV $n_{eq}/cm^2$

Thin sensors, high granularity, large area, moderate radiation

➔ Monolithic silicon pixel sensors

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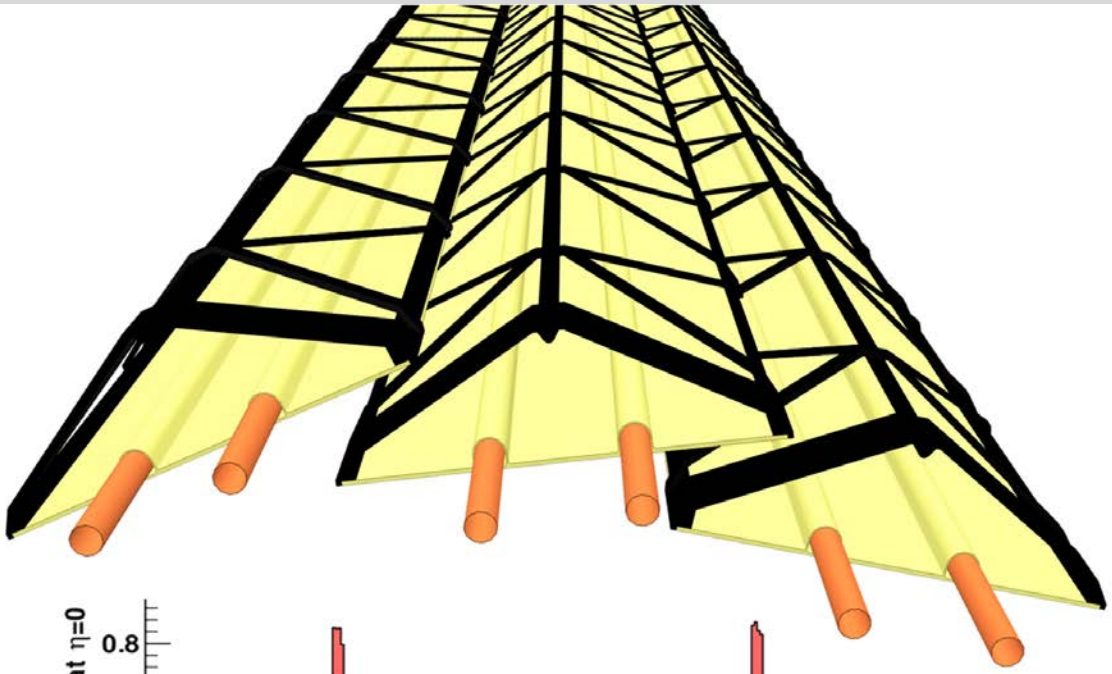
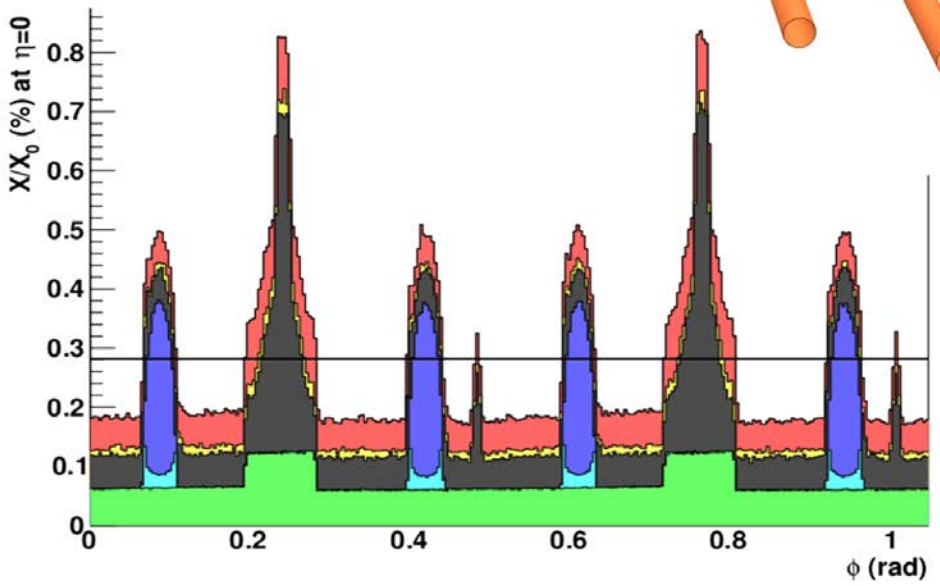
# ALICE ITS UPGRADE: MATERIAL BUDGET: INNER BARREL





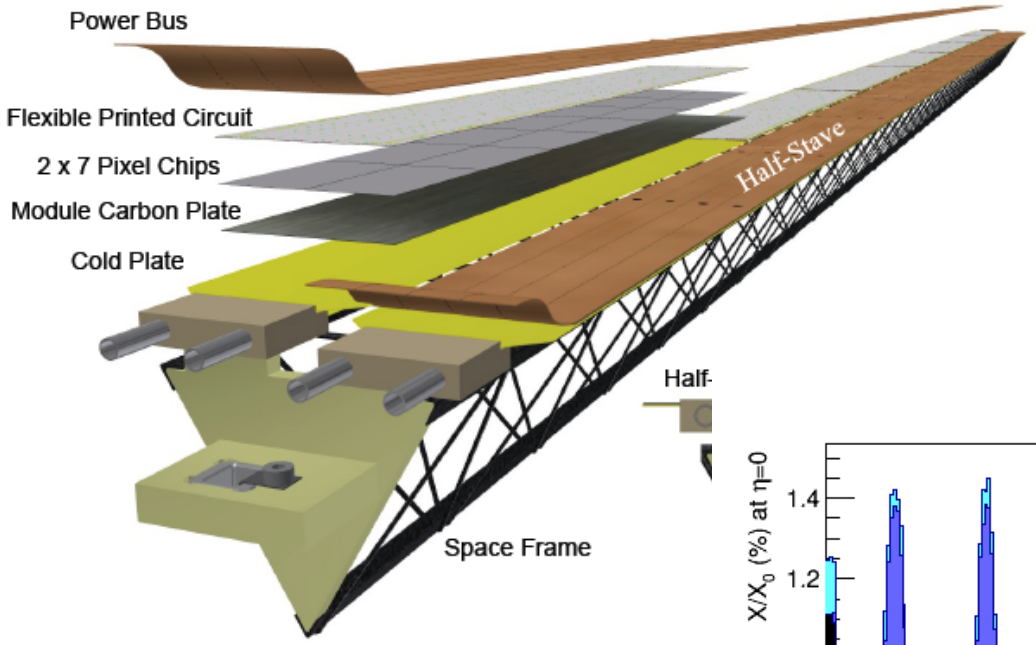

Power density specification :
<100 mW/cm²

Flex Printed Circuit (22%)
Glue (5%)
Carbon Structure (33%)
Water(13%)
Cooling pipes wall (2%)
Pixel Chip (26%)

Mean X/X0 = 0.282%

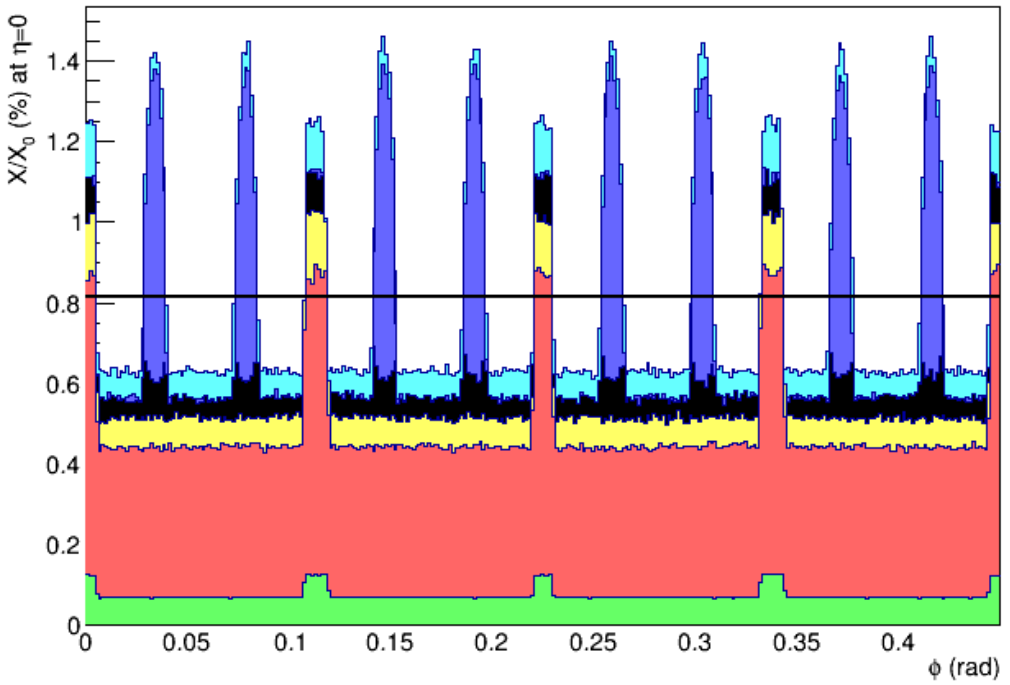
Mechanics: C. Garguilo et al (see also his ECFA 2014 presentation)

# ALICE ITS UPGRADE: MATERIAL BUDGET OUTER BARREL




Carbon Structure (9.1%)
Water (14.2%)
Cooling Pipe Walls and Cold Plate (8.0%)
Glue (9.5%)
Flex Cable (50.1%)
Pixel Chip (9.2%)

**50 %**




Reduce power consumption to reduce material budget

Mechanics: C. Garguilo et al (see also his ECFA 2014 presentation)

# Low power for low material

- Power consumption : 3 components

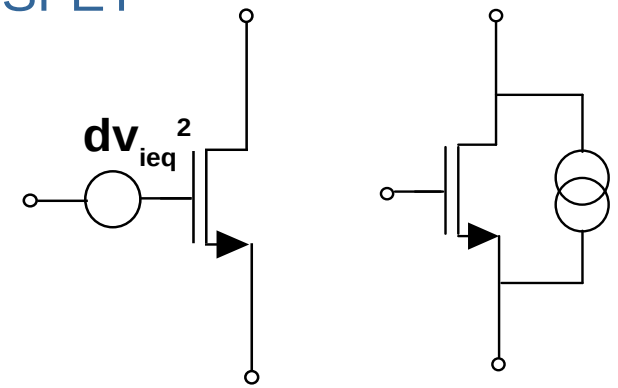
- Analog:
  - Determined by collected charge over capacitance (Q/C) in the pixel => pixel sensor optimization

- Digital:
  - Determined by on-chip architecture & cluster size

- Data transmission off-chip:
  - Clustering algorithm important to reduce data on-chip
  - Very high granularity will increase number of bits per hit, but not more than ~2x

# ANALOG POWER CONSUMPTION

NOISE SOURCES IN A MOSFET EQUIVALENT WITH :




$$di_{eq}^2 = g_m^2 dv_{eq}^2$$

WHERE:

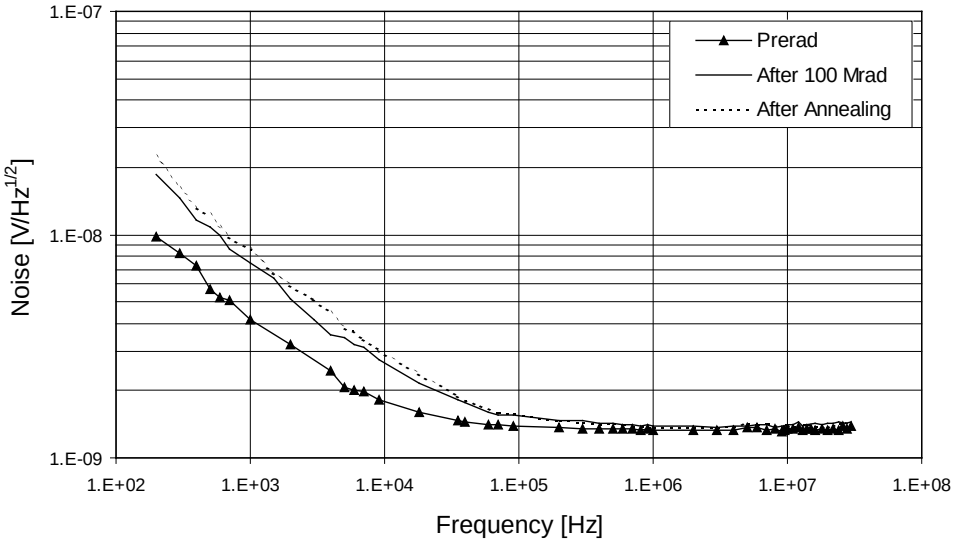
In weak inversion (WI):

$$g_m \sim I \qquad dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 2kTn/g_m)df$$

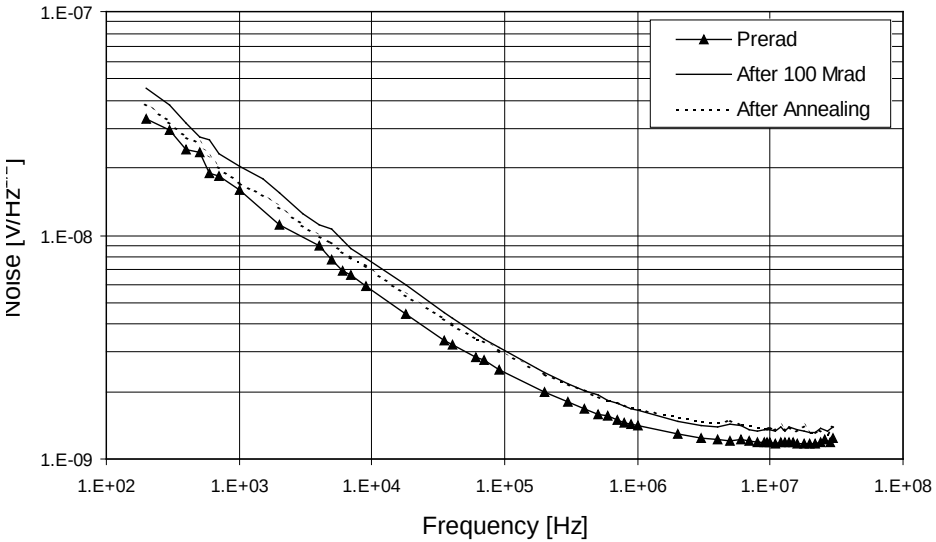
In strong inversion (SI) :

$$g_m \sim \sqrt{I} \qquad dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 4kT\gamma/g_m)df$$

# Noise sources in a FET




PMOS




NMOS

Note : Radiation tolerance (0.25 μm CMOS) !

Deeper submicron generally even more rad tolerant

# Signal to noise ratio and analog power consumption

$$\frac{S}{N} \sim \frac{Q/C}{\sqrt{gm}} \sim \frac{Q}{C}\sqrt[m]{I} \sim \frac{Q}{C}\sqrt[m]{P} \; with \; 2 \leq m \leq 4$$

or $$P \sim \left\{\frac{S}{N}\frac{N}{Q}\frac{Q}{C}\right\}^{m} \; with \; 2 \leq m \leq 4$$

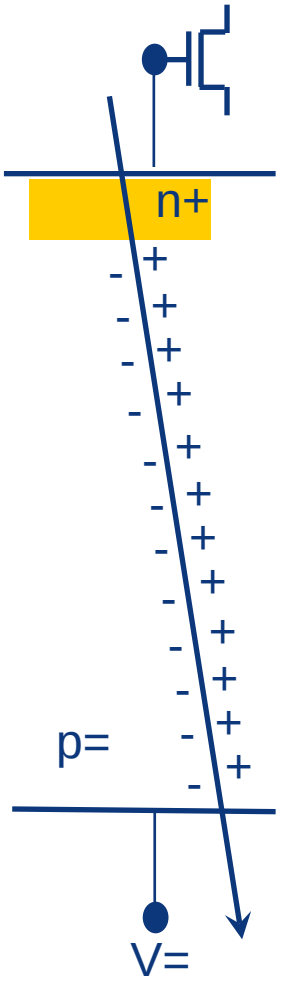
For constant S/N: $$P \sim \left[\frac{Q}{C}\right]^{-m} \; with \; 2 \leq m \leq 4$$

Signal charge/detector capacitance (Q/C) is THE figure of merit for the sensor determining the analog performance/power consumption and the S/N crucial for position resolution

m = 2 for weak inversion up to 4 for strong inversion

# High Q/C for low analog power

Transistor noise ≈ 0.16 mV at 40 MHz BW for 1 uA
(1uA/100x100 um pixel = 10 mW/sq cm)




$$\frac{S}{N} = 25 \Rightarrow \frac{Q}{C} = 4mV = \frac{4\,fC}{1\,pF} = \frac{0.4\,fC}{0.1\,pF} = \frac{0.04\,fC}{10\,fF}$$

| | | | |
|---|---|---|---|
| Collection depth | 300 μm | 30 μm | 3 μm |

doubling Q/C allows
(at least) 4x power reduction for same S/N

*Monolithic* →

*For Alice ITS upgrade:* $\frac{Q}{C} > \frac{0.2\,fC}{2.5\,fF} = 80mV$

distributed over a few pixels…

Conventional 300 μm thick strip detector: 4fC/20pF=0.2mV…

# MONOLITHIC ACTIVE PIXEL SENSOR FOR THE ALICE ITS UPGRADE

Replace the inner tracking system with an entirely new detector in 2018-2019

ALICE-TDR-17/CERN-LHCC-2013-024

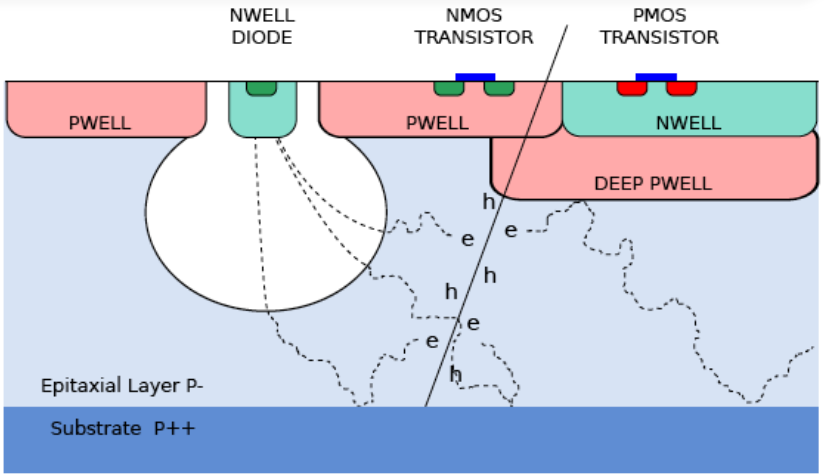
Thin sensors (50 μm), high granularity (~30 x 30 $\mu m^2$), large area (10 $m^2$), moderate radiation (TID 700 krad & NIEL$10^{13}$ 1 MeV $n_{eq}/cm^2$)

➔ Monolithic silicon pixel sensors

## Technology choice

TowerJazz 180 nm CMOS imaging process

- Deep Pwell
- Gate oxide < 4 nm good for TID
- 6 metal layers
- 15…40 μm 1…8 kΩcm epitaxial layer
- Epi not fully depleted




## Chip development

- Since end 2011, 4 MPWs and 4 engineering runs, 5th to be submitted in April.
- Small scale prototypes for sensor optimization and radiation tolerance verification
- Full scale prototypes recently fabricated: lab and beam tests ongoing also on:
  - irradiated
  - thinned devices
  - thinned devices soldered on flex

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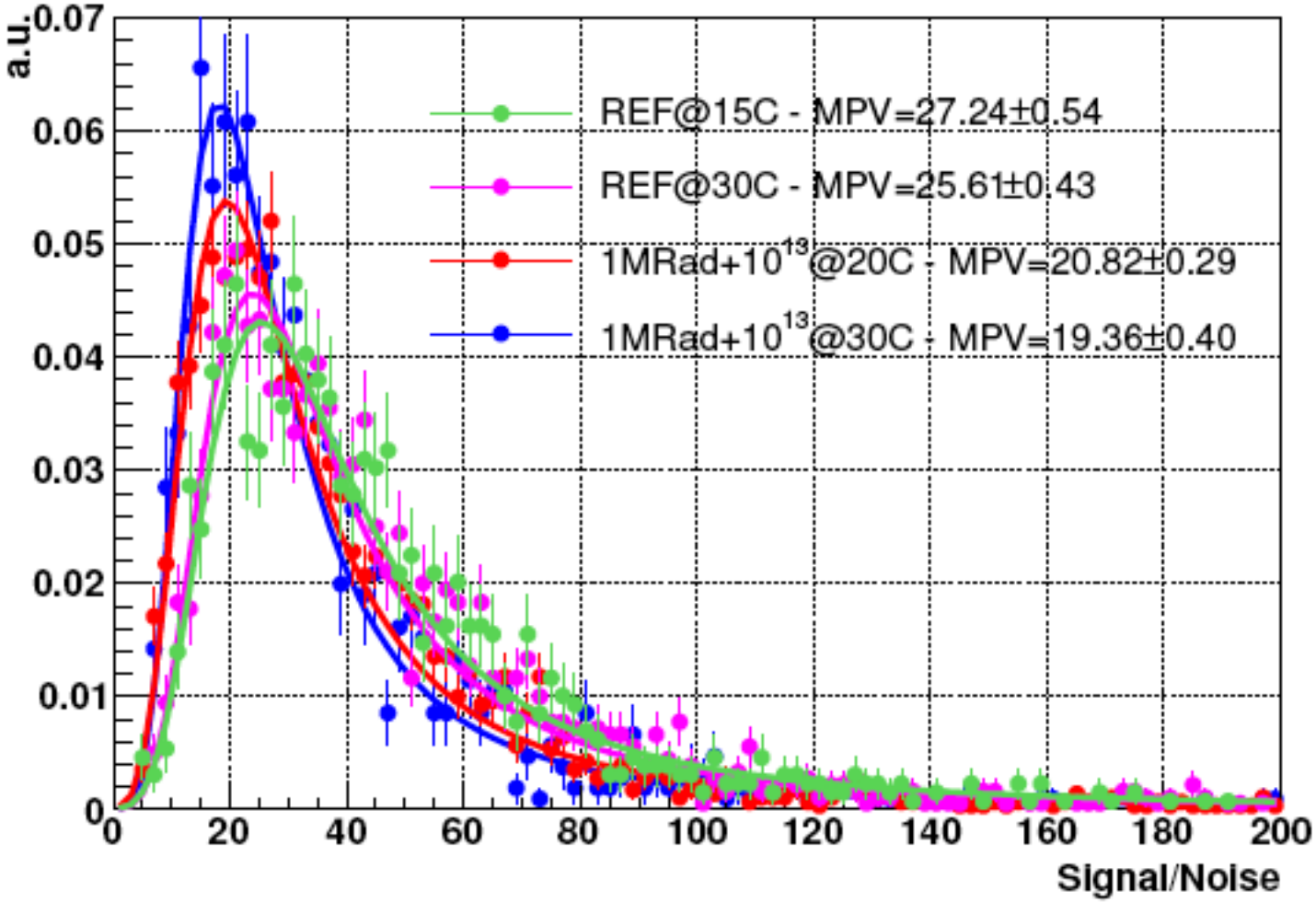
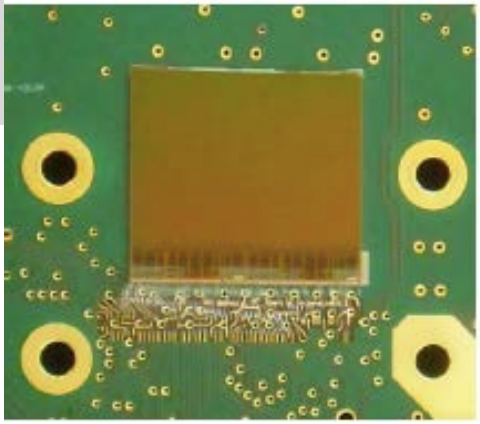
# RADIATION TOLERANCE

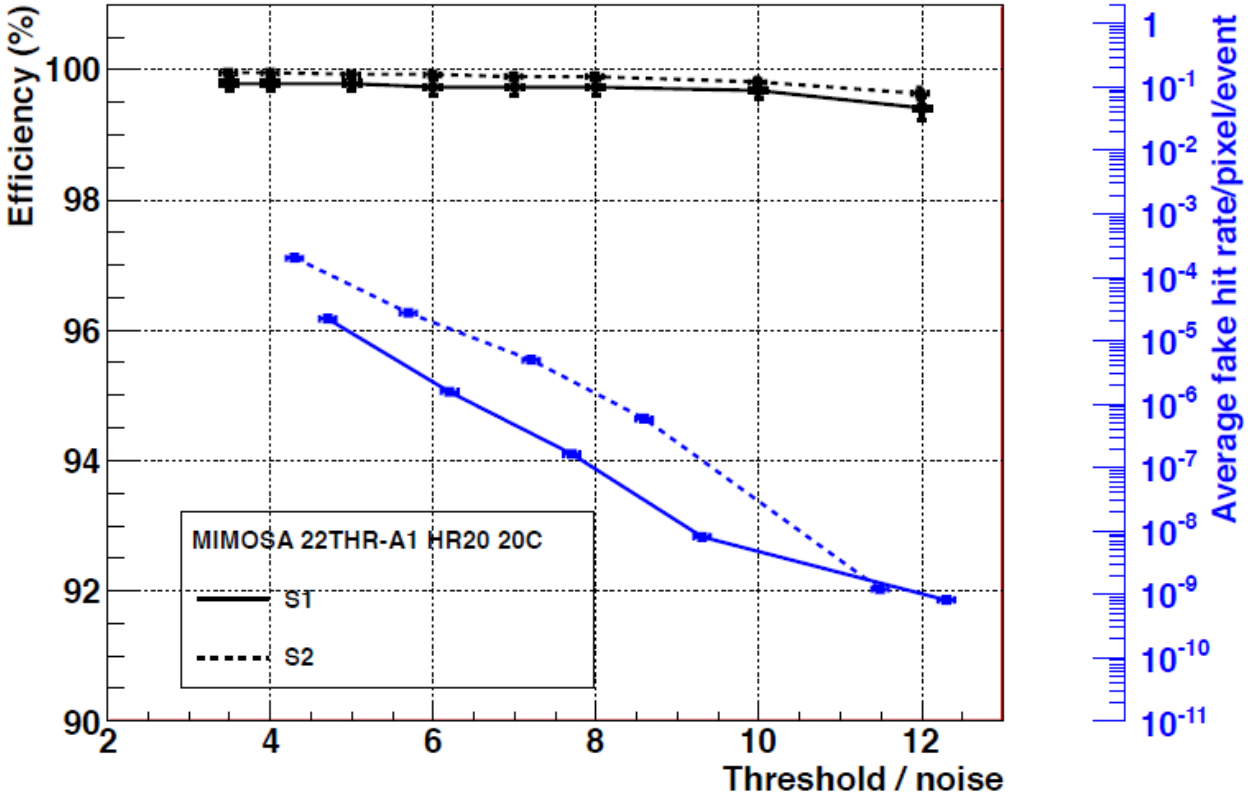



Example: SNR of seed pixel measured with MIMOSA-32 ter at the CERN-SPS at two operating temperatures, before and after irradiation with the combined load of 1 Mrad and $10^{13}$ 1 MeV $n_{eq}/cm^2$

# MISTRAL



- Rolling shutter: evolution of STAR like development
- MISTRAL full scale prototype functional
  - lab tests promising, ENC 15-20e
  - preparing for test beam
- Beam test results:



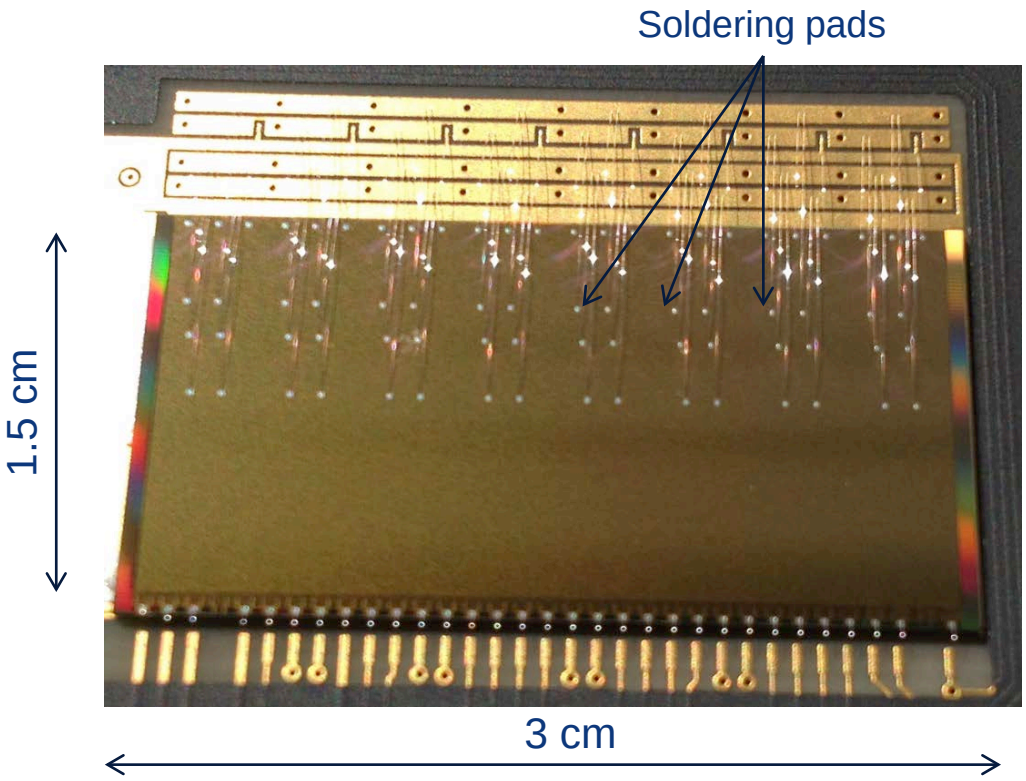

Efficiency above 99 % with fake hit rate below $10^{-5}$ achievable

# ALPIDE IN ALICE ITS UPGRADE

ALPIDE

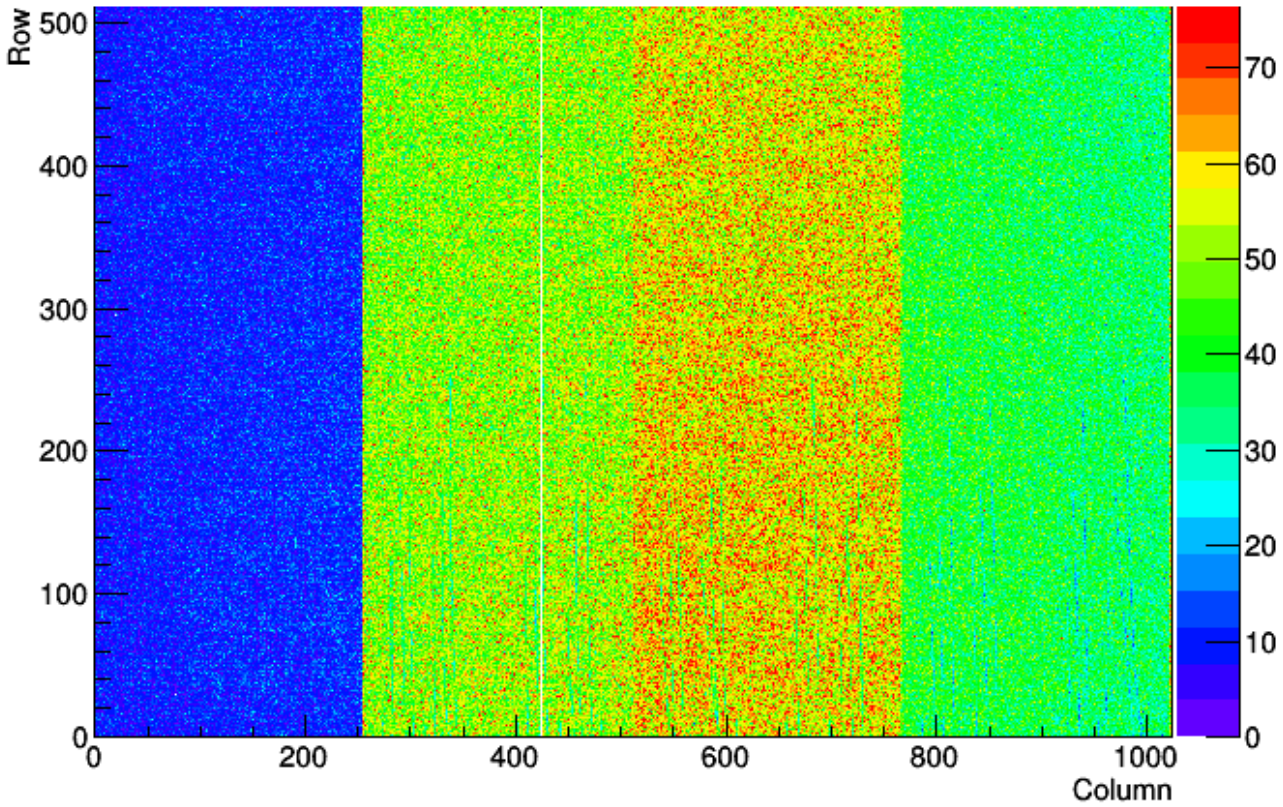
- Q/C > 80mV (>0.2fC/2.5fF = 80mV) spread over a few pixels

  (18 μm collection depth and 2.5fF with charge on a single pixel)
- Q/C optimization allowed in-pixel amplifier/comparator ~ 40nW (~5 mW/cm$^2$)
- Hit driven readout (priority encoder)
- Final chip expected ~150 mW/chip or < 40 mW/cm$^2$ (note important fraction of digital)



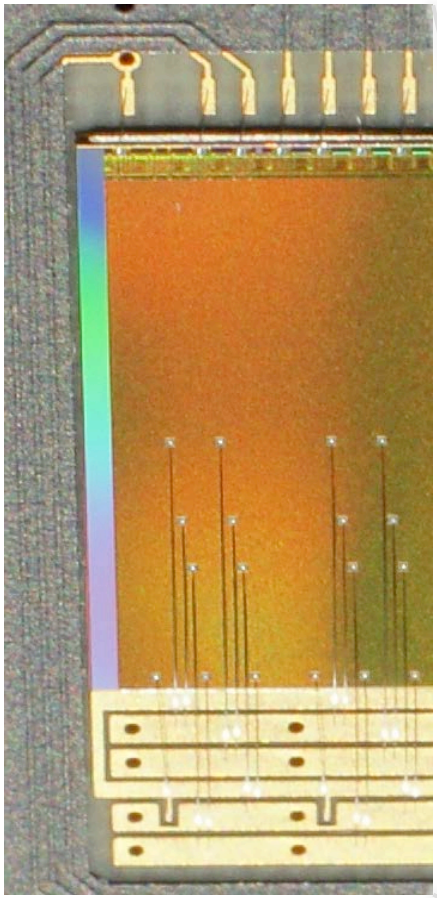
# $^{55}$Fe SOURCE MEASUREMENT (5.9 keV photons)

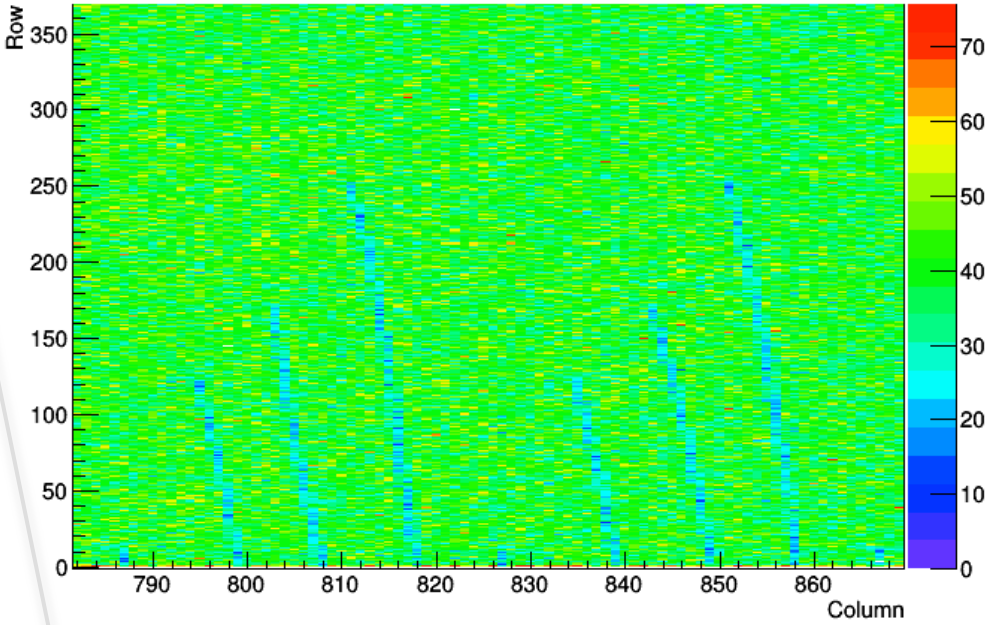
- Measurement with $^{55}$Fe source (5.9 keV photons)

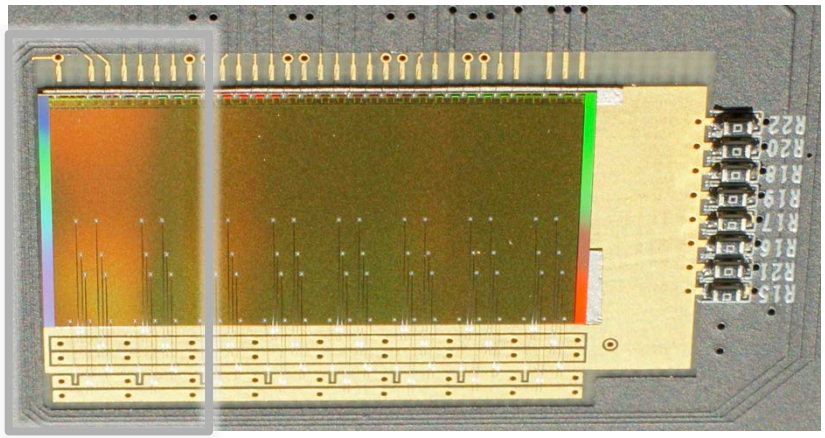



- Entire chip (apart from 1 bad column) sees source.
- Difference between 4 different pixel types as expected; for line-structure see next slide

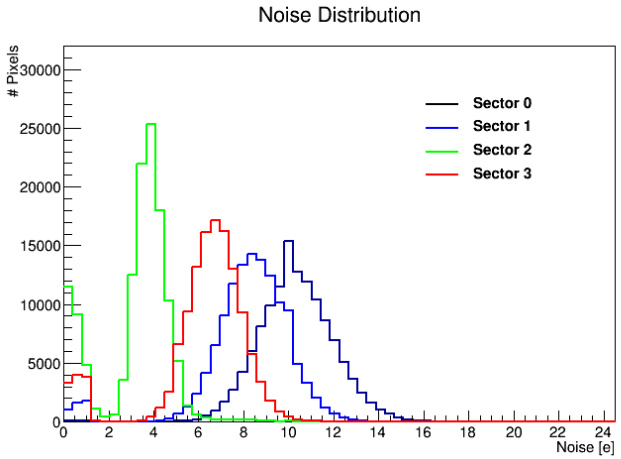
# RADIOGRAPHY OF WIREBONDS

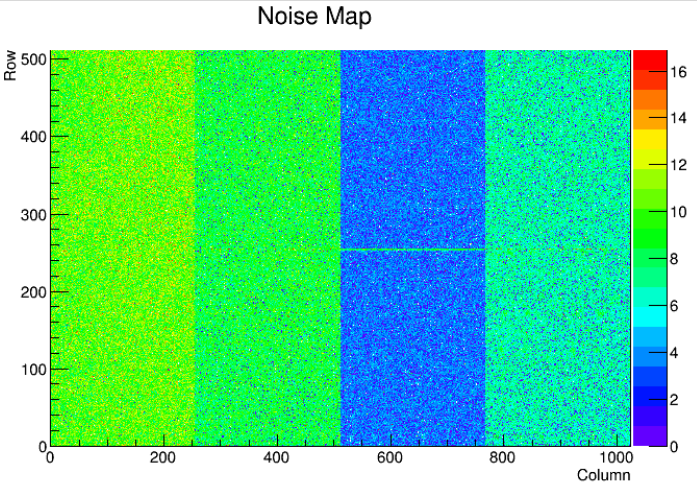


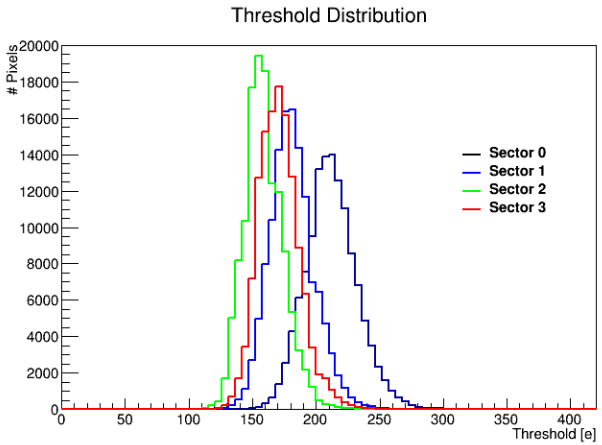


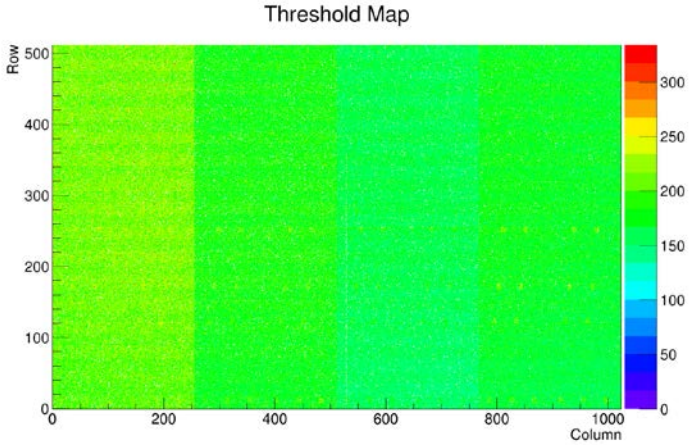



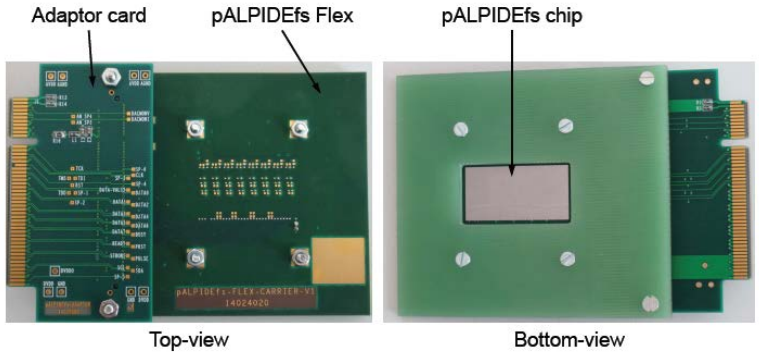
# THINNED ALPIDE SOLDERED ON FLEX



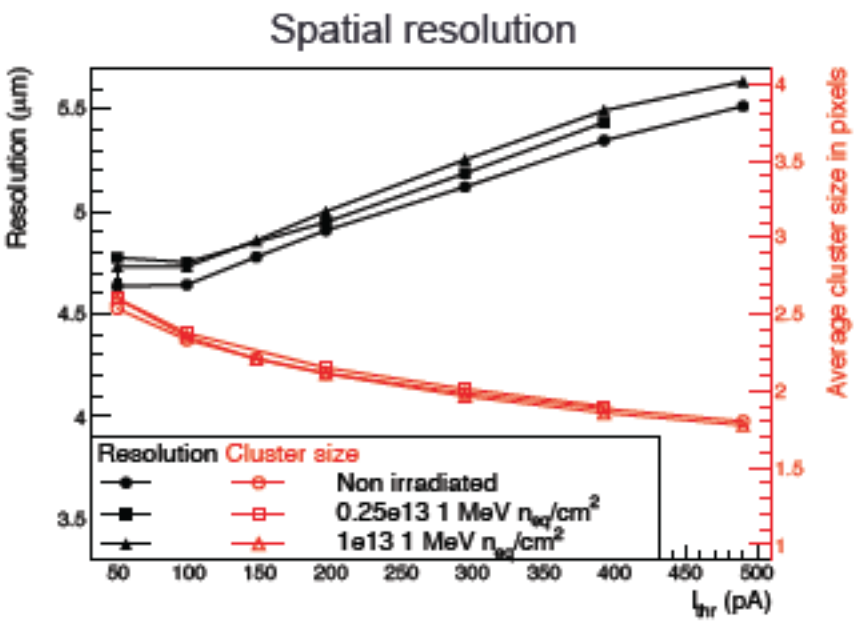



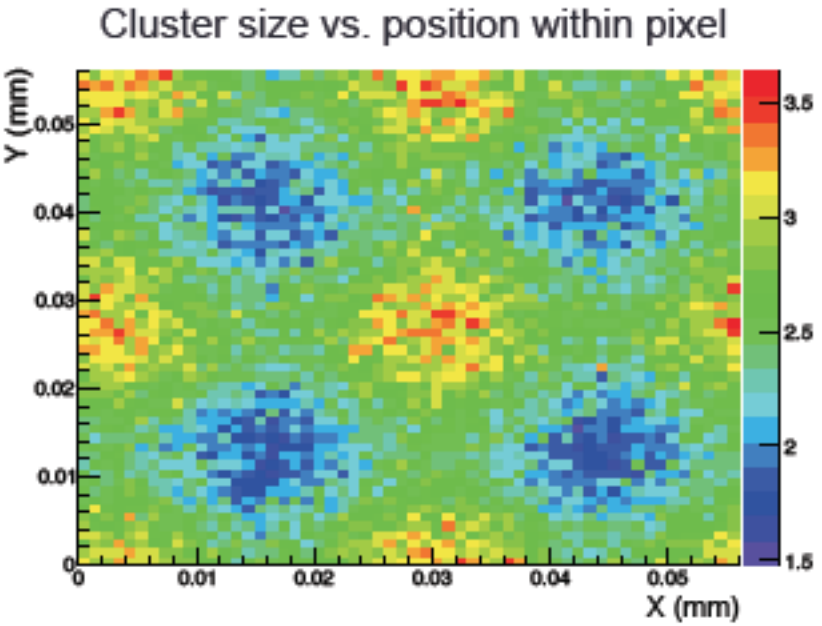




- Behavior similar as before thinning
- Band structure reflects different design options in the prototype chip
- Noise << Threshold spread ~ 18 e

CERN ALICE

# POSITION RESOLUTION AND CLUSTER SIZE

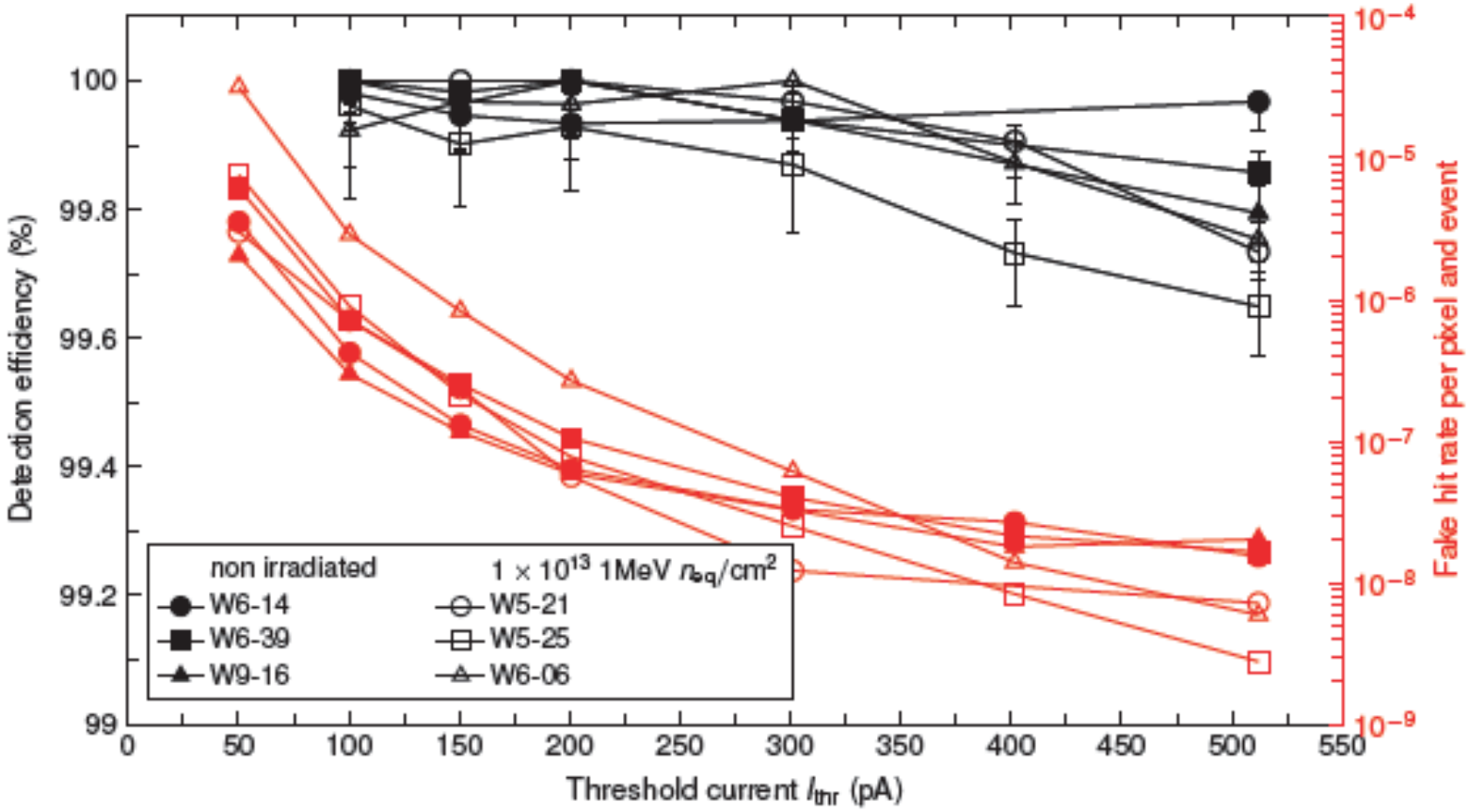


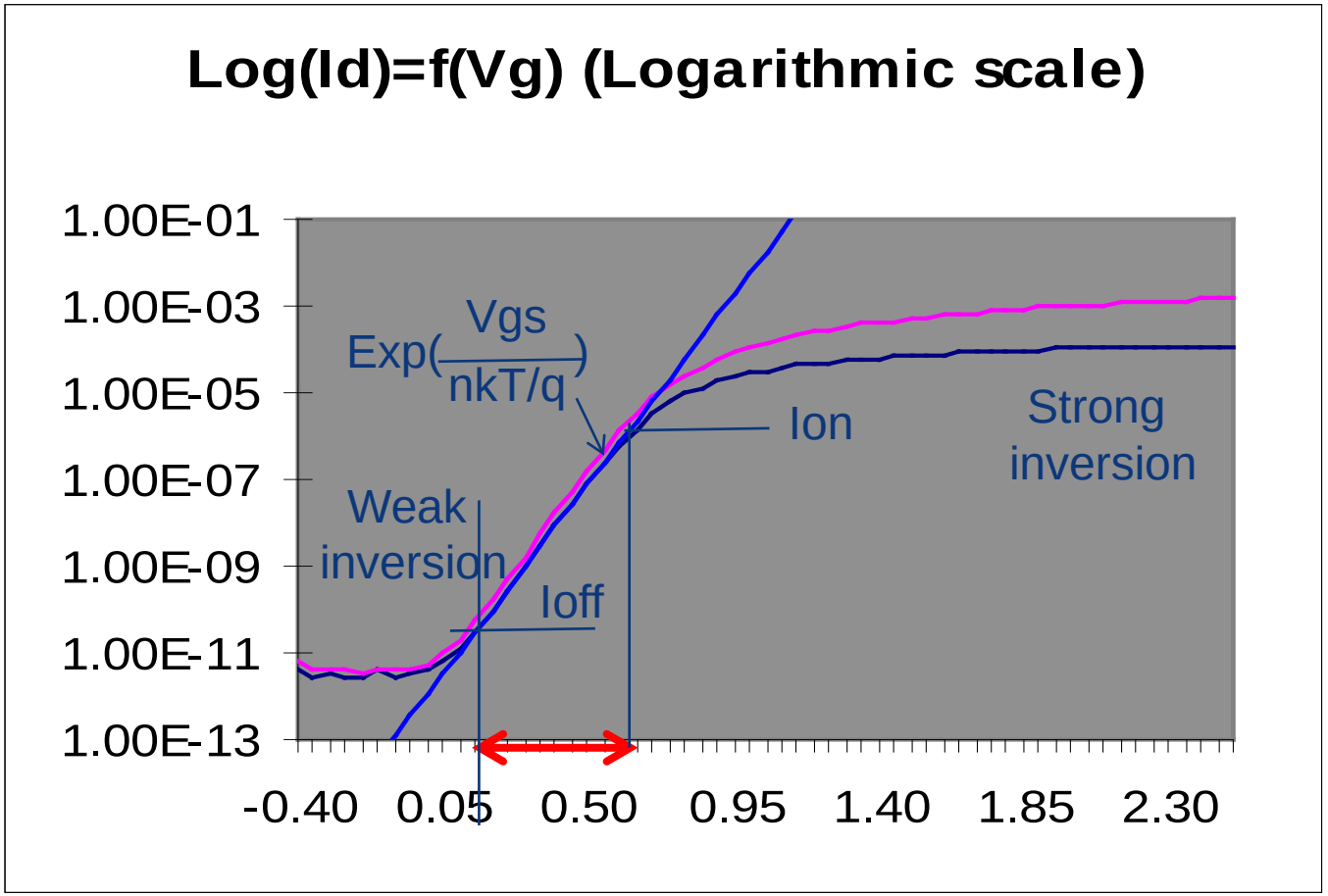

$\sigma_{det} < 5$ μm is achieved with sufficient margin of operation

- Measurements at PS: 5 – 7 GeV π
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25 x $10^{13}$ and $10^{13}$ 1MeV $n_{eq}$ / cm² (10 x load expected in 6 years)

# EFFICIENCY AND FAKE HIT RATE



# DIGITAL SIGNAL by further optimization ?




Slope in weak inversion 60-90 mV/decade,

for Ion/Ioff=$10^4$ on a single pixel => 250-360mV

Would practically eliminate analog power consumption

# (TOO) SIMPLE SIMULATION

*~ 300mV at input with*

*2 nA total standby current*

*(1nA in input transistor)*

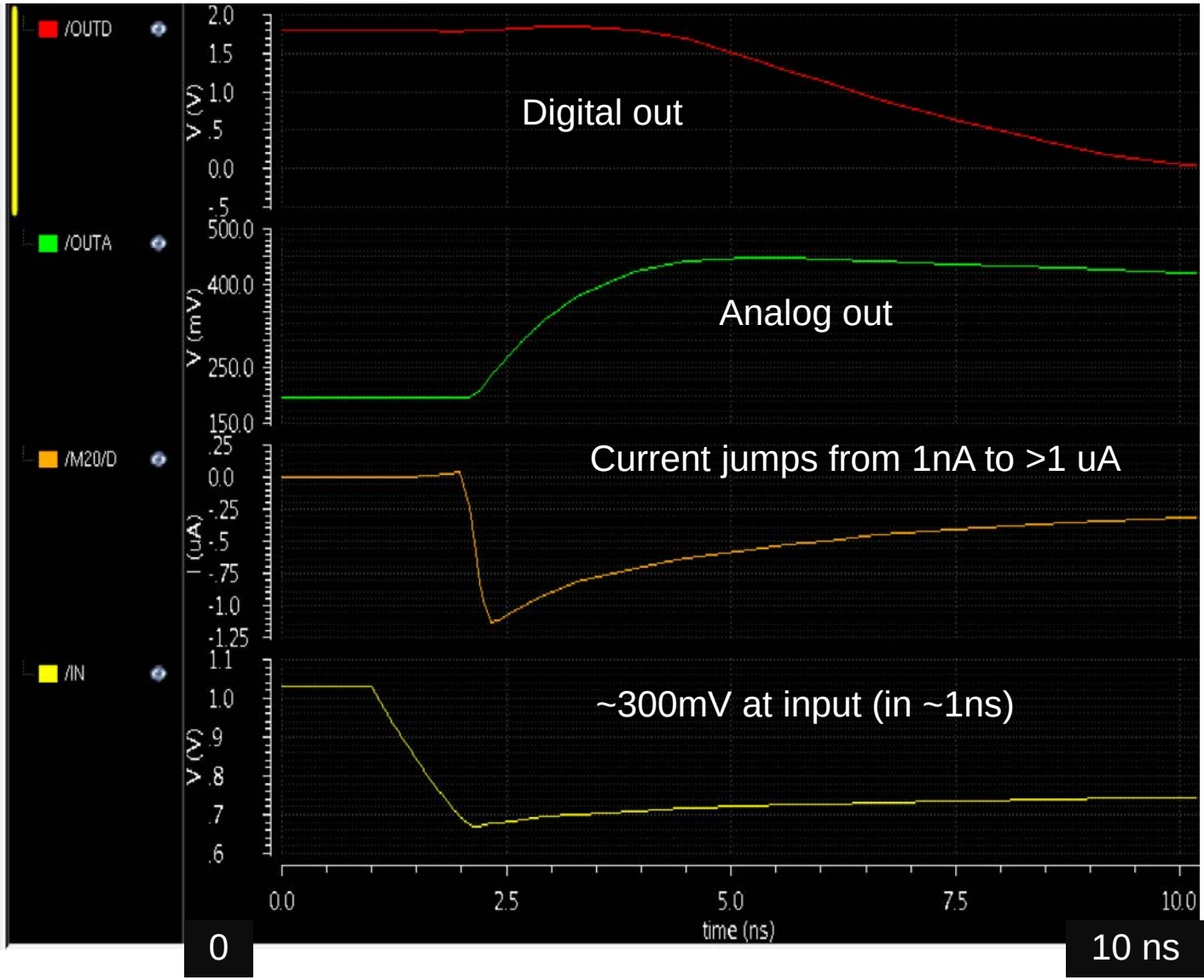
*=>*

*Just to demonstrate that very large Q/C*

*offers speed and low standby current…*

*1nA/pixel = 1mA/cm$^2$*

*for 10µm x 10µm pixel*

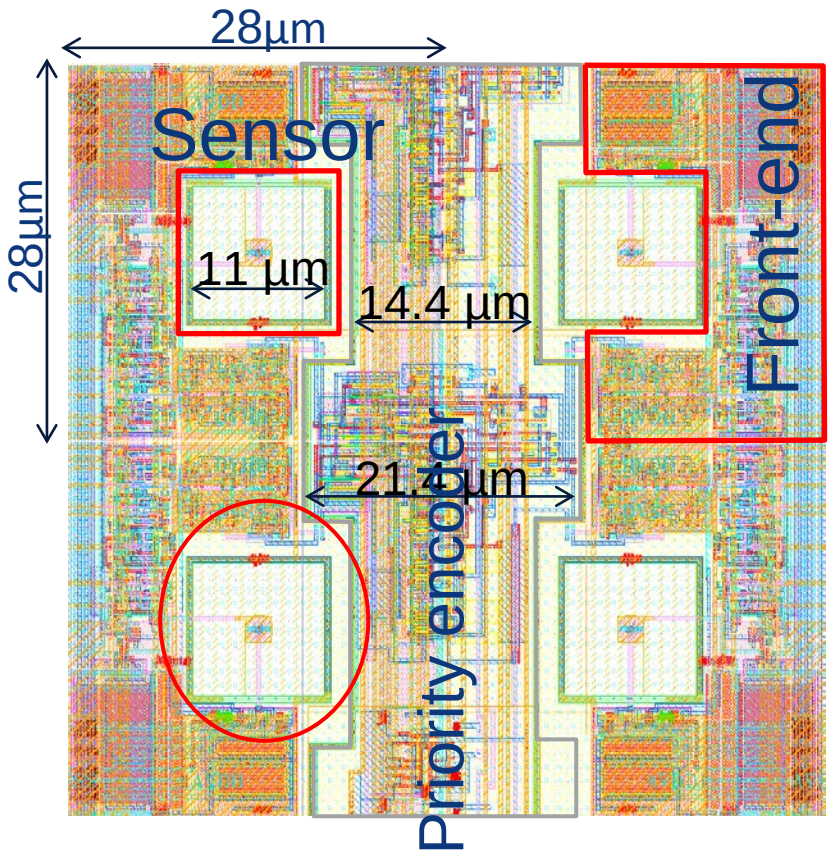


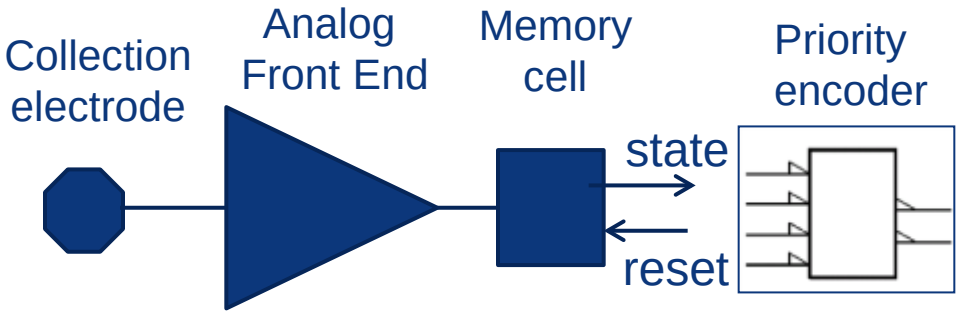
# NOISE FOR LONGER INTEGRATION TIMES

For integration times of many tens of microseconds:

- Noise often leakage current dominated (shot noise), but significant progress (4T cells, leakage reduction)
- Impressive noise numbers (ENCs of ~1 e or even below using multiple sampling of reset and signal level)
- For high energy physics longer integration times not always applicable, also investigating different architectures for lower power (see next slides)

# Binary Front End + Architecture : eg Priority Encoder




Binary Frontend (~ 40nW or ~5mW/cm$^2$ for 28x28 micron pixels) allows other readout architectures

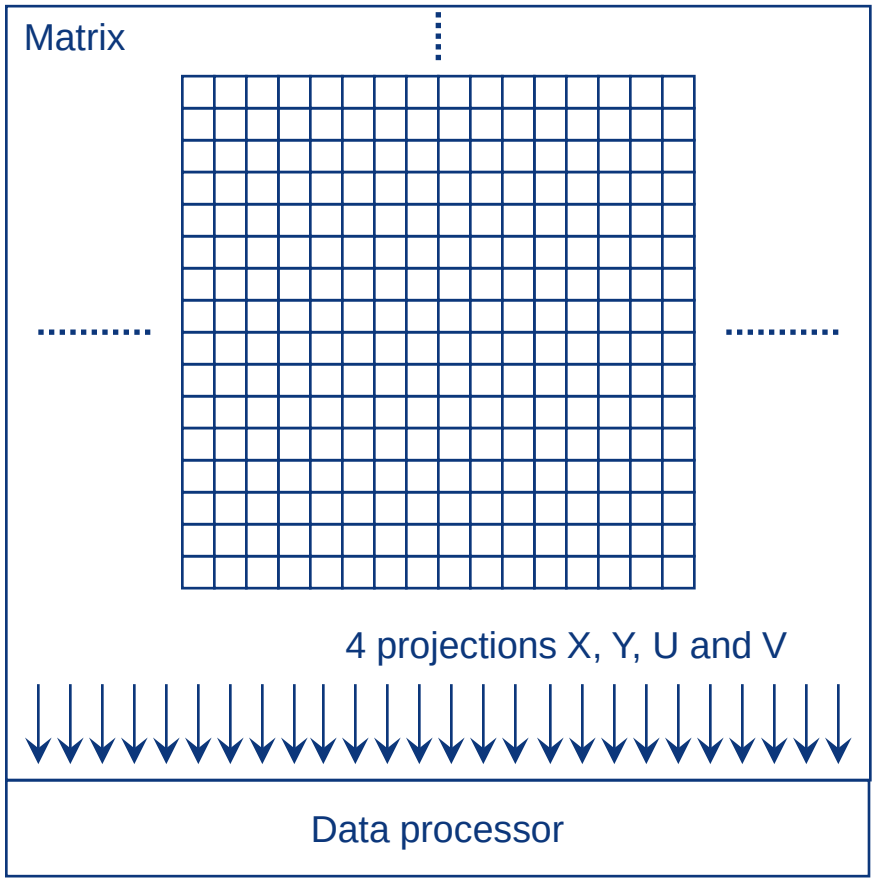
Signal routing on 4 metals instead of 6 to accommodate the pads over the matrix.

0.18 micron technology, much smaller if in finer linewidth technology -> 10 x10 micron …

Radiation tolerance sufficient for Alice,

expect much better if full depletion of the epitaxial layer would be reached

# ARCHITECTURE FOR SIMPLE IN-PIXEL CIRCUIT

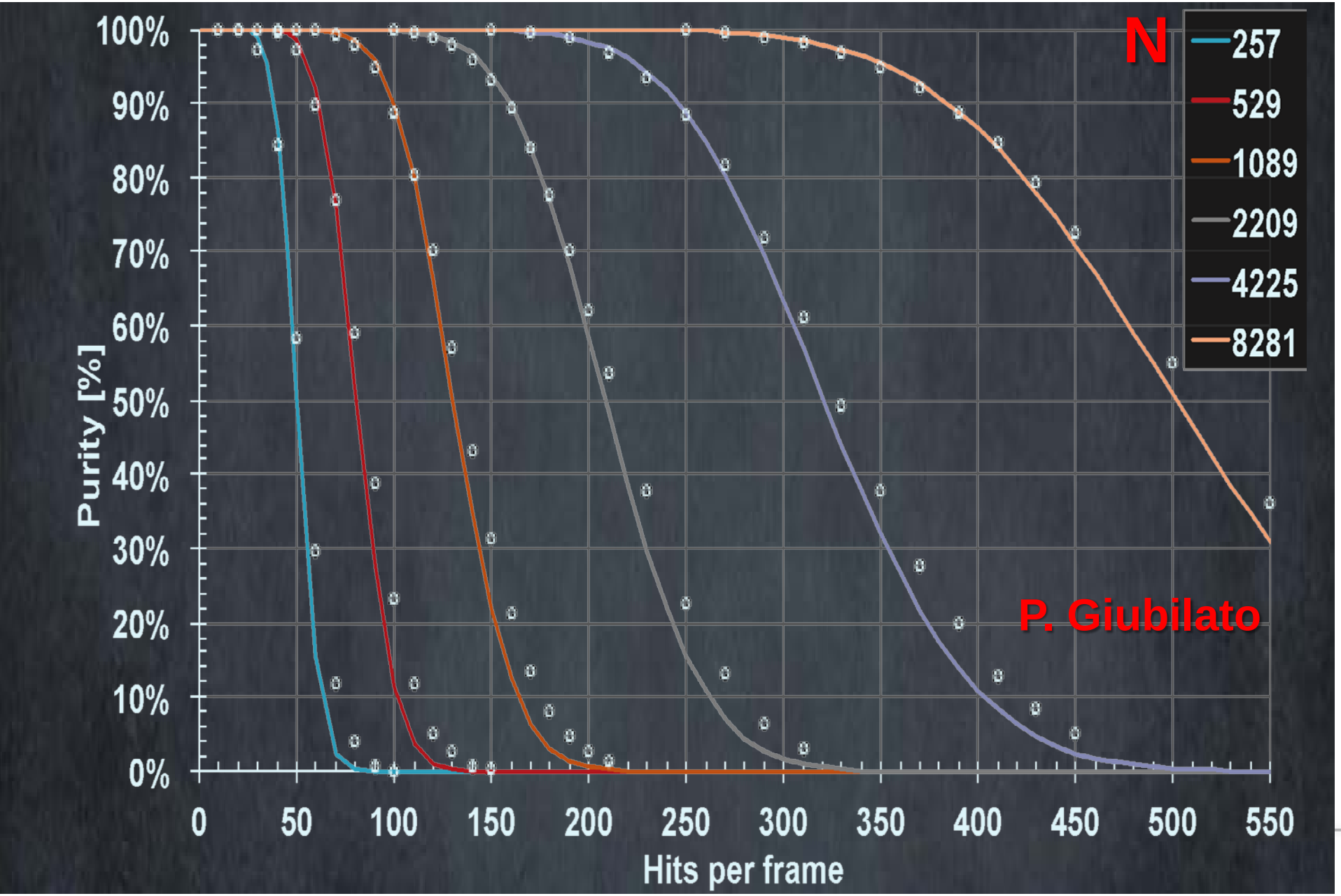



P. Giubilato Pixel 2012 : Orthopix

- Reduce number of signals using projections (also reduce power !)
- Avoid clock tree in the matrix
- Minimize ambiguities by requiring orthogonal projections (maximize information)
- No inefficiencies, but ambiguities at large occupancies
- Purity = percentage of hits that can unambiguously reconstructed in one layer
- Avoid clock tree in the matrix

For 4 projections reduction from $N^2$ to 4N

# PURITY OF RECONSTRUCTION



# DATA TRANSMISSION ON-CHIP

- Example FCC-hh: inner layer: 30 bits/cluster * 6.4 clusters/cm$^2$ * 200 MHz = 40 Gb/s/cm$^2$
- On-chip (even over some parallel lines) over a distance of 1 cm:
  - Required power = f*CV$^2$ = 40Gb/s * 1cm * 0.2fF/um * 1V$^2$
    = 40Gb/s * 2pF * 1V$^2$ = 80 mW…
  - Clock tree power = 200MHz * 1000 * 2pF * 1V$^2$ = 400 mW -> power prohibitive if clock is distributed to every pixel
  - Need to :
    - optimize data transmission even on-chip
    - avoid distributing the clock to every pixel
- Between chips for the outer layers
  - Need chip-to-chip communication
  - Data rate much less critical, but noise occupancy can easily dominate data rate

# POWER OPTIMIZATION OF ON-CHIP DATA TRANSMISSION

- In the previous example 30 bits/cluster over 1 cm = 80 mW
- For orthopix 4 bits/hit pixel, if on average 2 pixels hit/cluster= 8 bits per cluster instead of 30 bits => power reduction by a factor 4
- Very deep submicron CMOS can offer very large line densities. This can be exploited to reduce power consumption, but more work is necessary.
- Line density decreases drastically going off-chip, need some type of serialisation, and work on power, see next slide

# DATA TRANSMISSION OFF-DETECTOR

- Present developments for HEP: significant power penalty to be SEU robust
  - P. Moreira et al. : Low Power GBT :

    500mW for 9.6Gb/s (65nm) (GBT 2 W(130nm)) (including many features)
  - V. Gromov et al. : Velopix: (TWEPP2014)

    60 mW for 5.12 Gb/s transmission (+ PLL 30 mW) over 70 cm flex (130nm)
  - TDCpix (NA62):

    4*87mW (serializer) + 110 mW (PLL) for 3x3.2=12.8 Gb/s (130nm)

    TDCpix (NA62):
- General R&D making good progress:

ISSCC 2013 / SESSION 2 / ULTRA-HIGH-SPEE

2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS

Amr Amin Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang

University of California, Los Angeles, CA

| Block | Power (mW) | Fraction (%) |
|---|---|---|
| VCO | 26.6 | 30.2 |
| Divider Chain | 18 | 20.5 |
| Buffer/PFD/CP | 2 | 2.3 |
| Predriver/Driver | 26.4 | 30 |
| Serializer | 15 | 17 |
| Total | 88 | 100 |

Important: data concentration & physical volume for material budget

# TOWARDS MORE RADIATION TOLERANCE IN MONOLITHIC

Epitaxial layer in the ALICE ITS sensor is not fully depleted resulting in moderate radiation tolerance

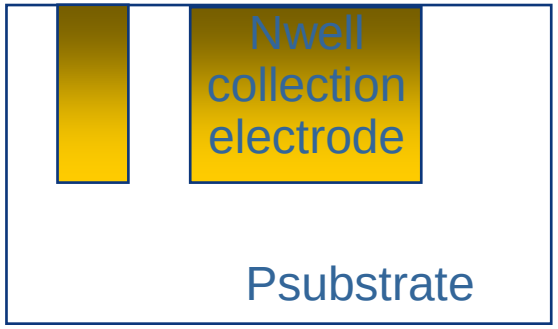
For higher radiation tolerance (and speed): full depletion, charge collection by drift

- Junction on the front with circuit in a well: in principle possible, but requires high circuit well voltage and ac coupling. Easier with simple circuit.
  *(eg: Dulinski et al (IPHC/Bonn) Pegasus: CPIX14)*
- Circuit in collection electrode: cfr HV/HR CMOS (see next presentation) or Lepix, radiation tolerance demonstrated, but need simple circuit to maintain reasonable C (can only include front end and put rest of the circuit in separate readout chip).
- Junction on the back side: works *(slides 48-50)*, but incompatible with standard foundries. Now some processing alternatives become available, but radiation tolerance and termination of the back side junction still needs verification *(eg. S. Lauxterman, IPHC/Bonn ESPROS, RAL TowerJazz…: CPIX14)*
- Silicon on Oxide: significant progress, challenges: charging of the oxide, circuit-sensor interaction *(eg: Y. Arai et al. Lapis and CERN/Bonn XFab: CPIX14)*

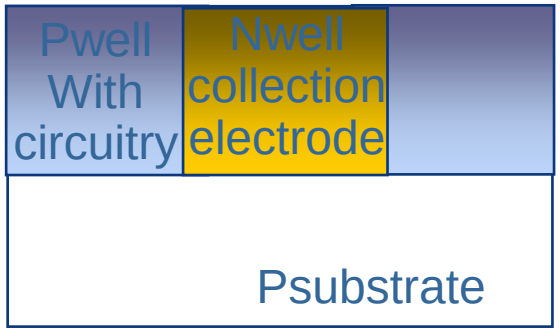
Essential to maintain good Q/C for low power consumption
(otherwise not realistic for the outer layers)

# DEVICE DESIGN challenge

Collect only on collection electrode, not elsewhere

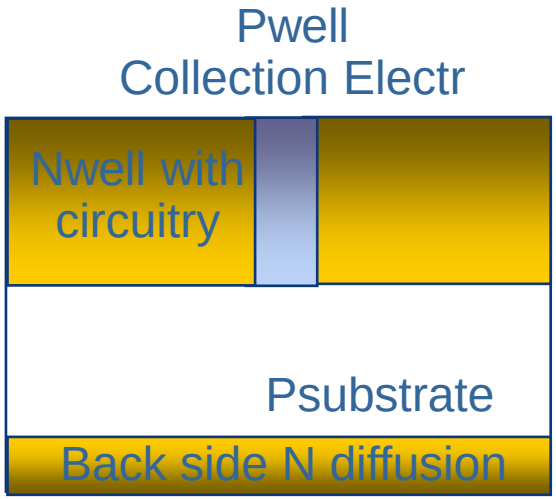



- Additional N-diffusion will collect and cause loss of signal charge
- → Need wells to shield circuitry and guide charge to the collection electrode for full efficiency




Wells with junction on the front

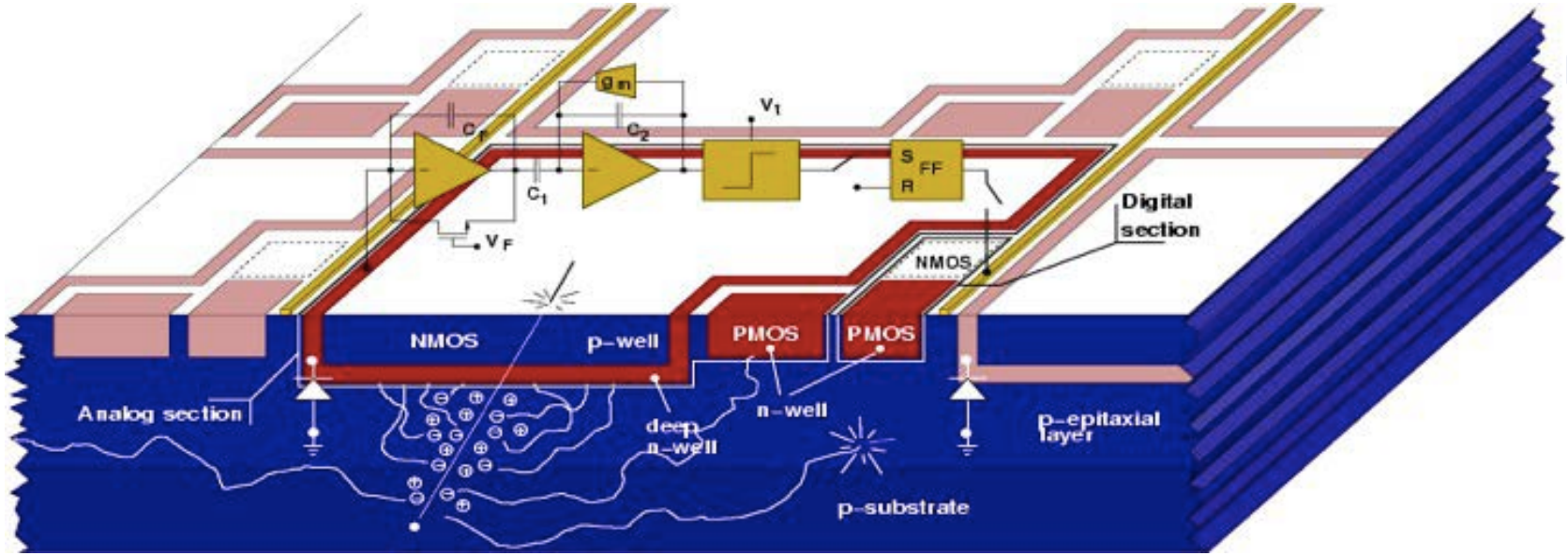
- Uniform depletion with small Nwell and large Pwell difficult
- Large fields or important diffusion component (MAPS)



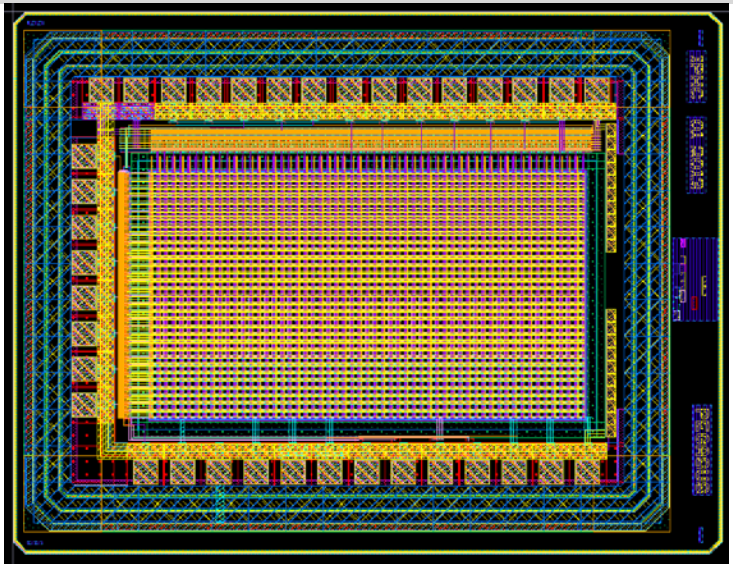

Wells with junction on the back. Need full depletion

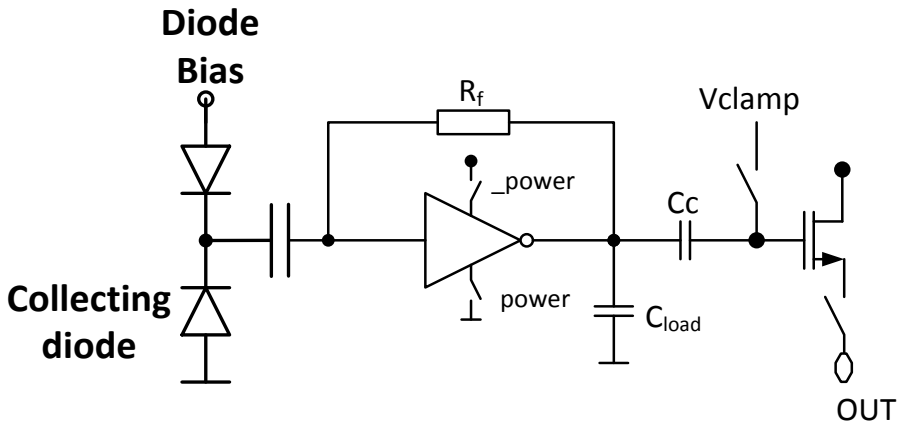
# No shielding well

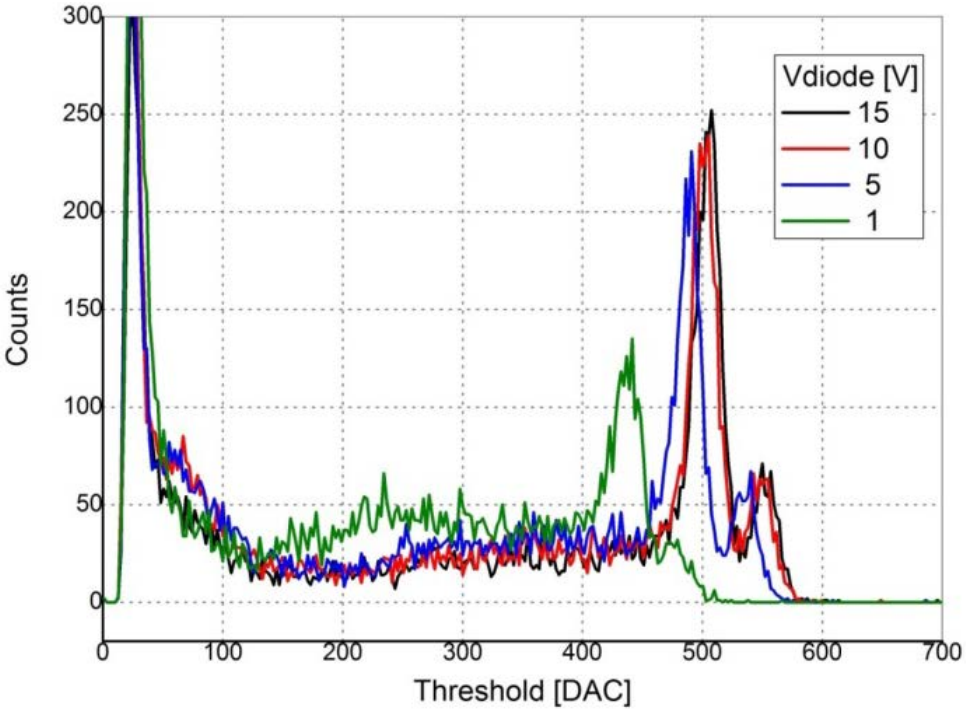

- G. Vanstraelen (NIMA305, pp. 541-548, 1991)
- V. Re et al., superB development: Nwell containing PMOS transistors not shielded it



# JUNCTION ON THE FRONT example PEGASUS





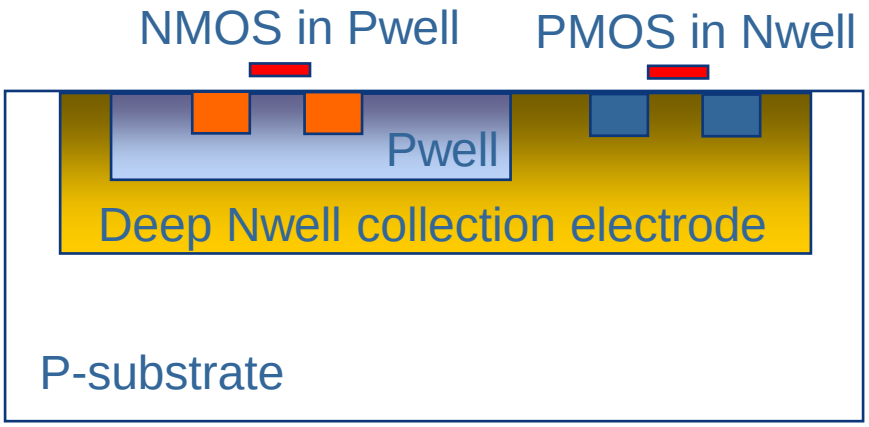




180nm CMOS (Tower)
Various types of epi in submission
Test result shown on 18 µm thick epi
25 x 25µm$^2$ pixels
Matrix - 56x32 with 4 versions of pixels

- Two source followers
- Two amplifiers

High biases
ENC 25 e-

# FULL DEPLETION FOR RADIATION HARDNESS




All circuitry in the collection electrode

- Can be done in any CMOS technology with deep Nwell (triple well)
- Apply high reverse substrate voltage (eg -60 V)
- Well protects transistors from HV
- Charge is collected by drift, good for radiation tolerance

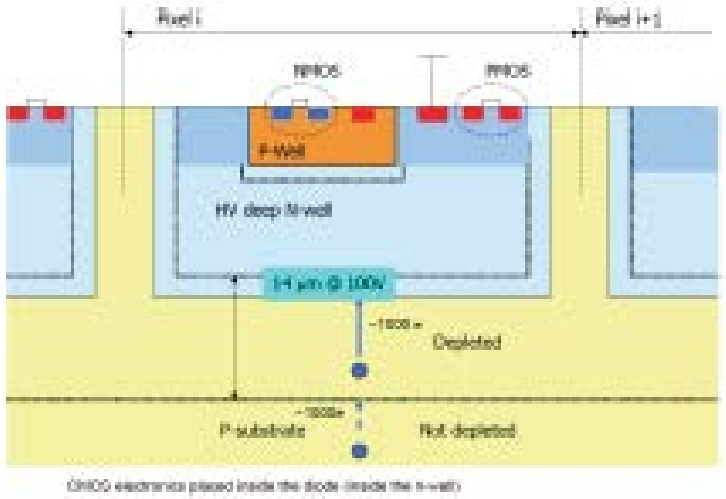
- Risk of coupling circuit signals into input
- In-pixel circuit simple in small collection electrode for low C by
  - 'rolling shutter' readout as in MAPS,
  - special architectures (eg LePIX), or
  - smart detector in hybrid solution (cfr ATLAS, I. Peric, D. Muenstermann)

# HV CMOS with deep N-well collection electrode

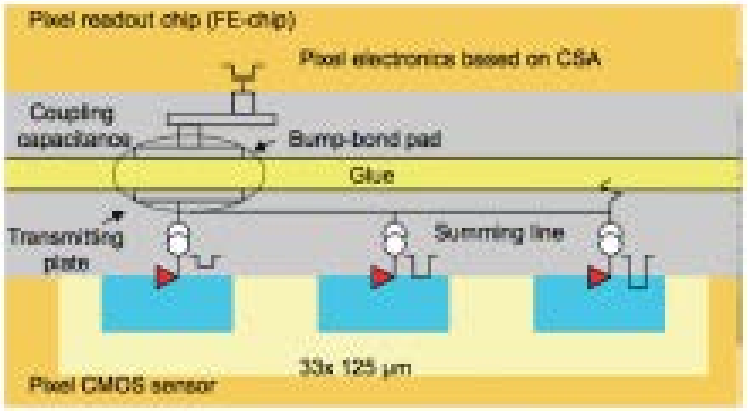
- Implemented in 0.18 and 0.35 µm CMOS
- Substrate resistivity low 10 Ωcm
- High reverse substrate voltage (eg -100 V)
- ~ 14 µm homogeneous depletion
- Charge is collected by drift, tests with glue bonded FEI4 indicate radiation tolerance up to $10^{16}$ $n_{eq}/cm^2$

- Can either have simple circuit in monolithic or more complex using glue bonding

Cfr G. Darbo's presentation

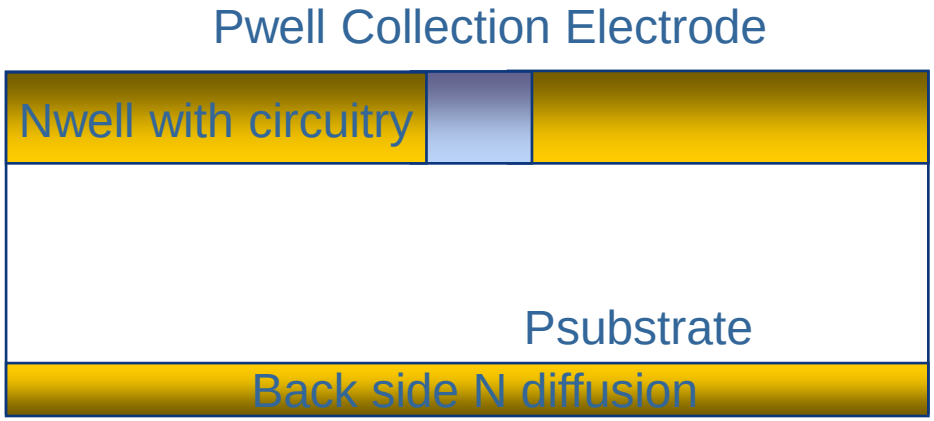



D. Münstermann, VERTEX 2013

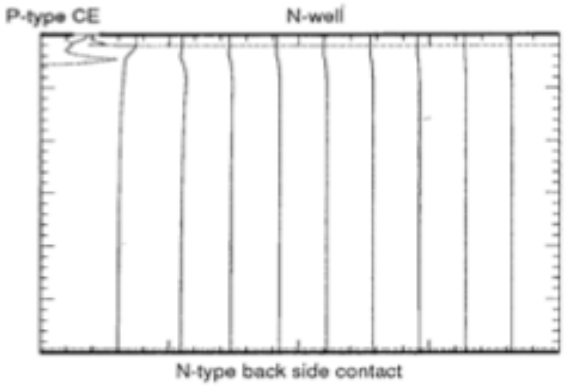



D. Münstermann, VERTEX 2013

# FULL DEPLETION WITH JUNCTION ON THE BACK

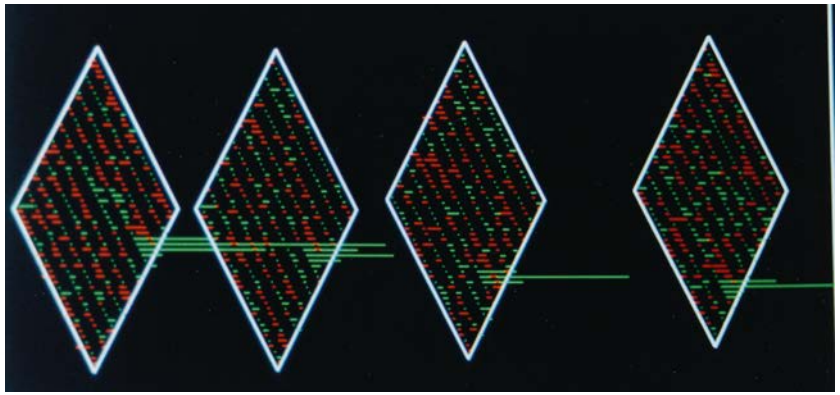



Only a few V on the Nwell diverts the flow lines to the collection electrode

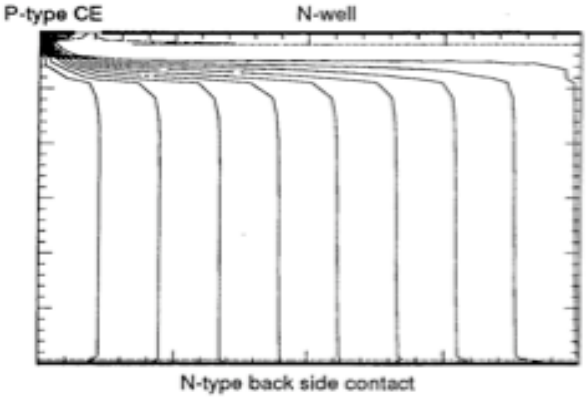



Vnwell = 0 V

- Need full depletion
- Double-sided process for junction termination, not really compatible with standard foundries



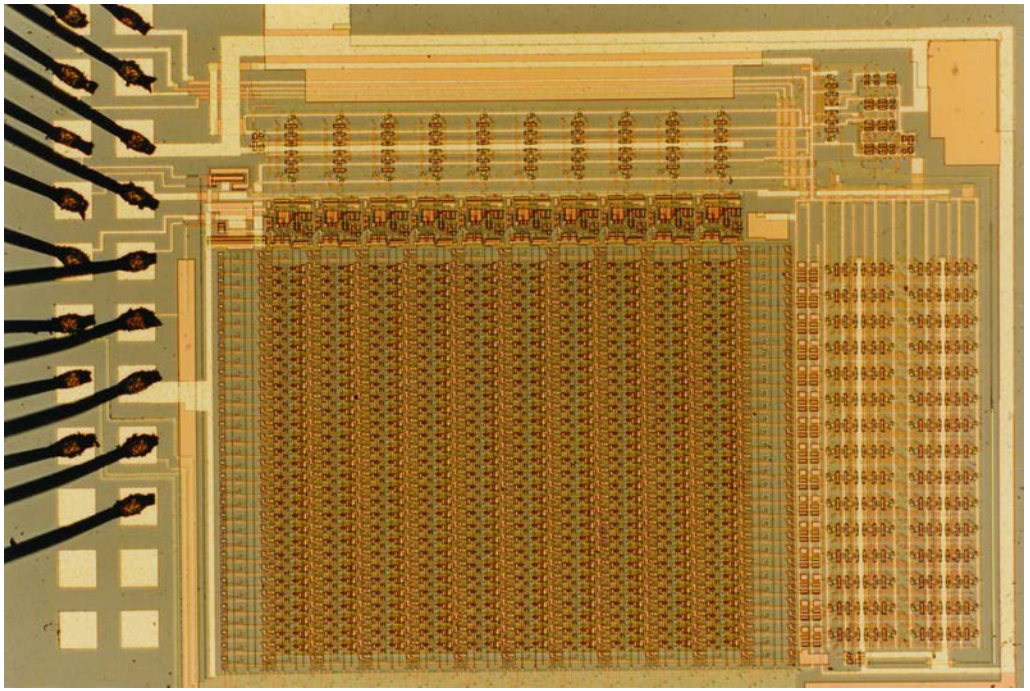
*C. Kenney, S. Parker (U. of Hawaii), W. Snoeys, J. Plummer (Stanford U) 1992*

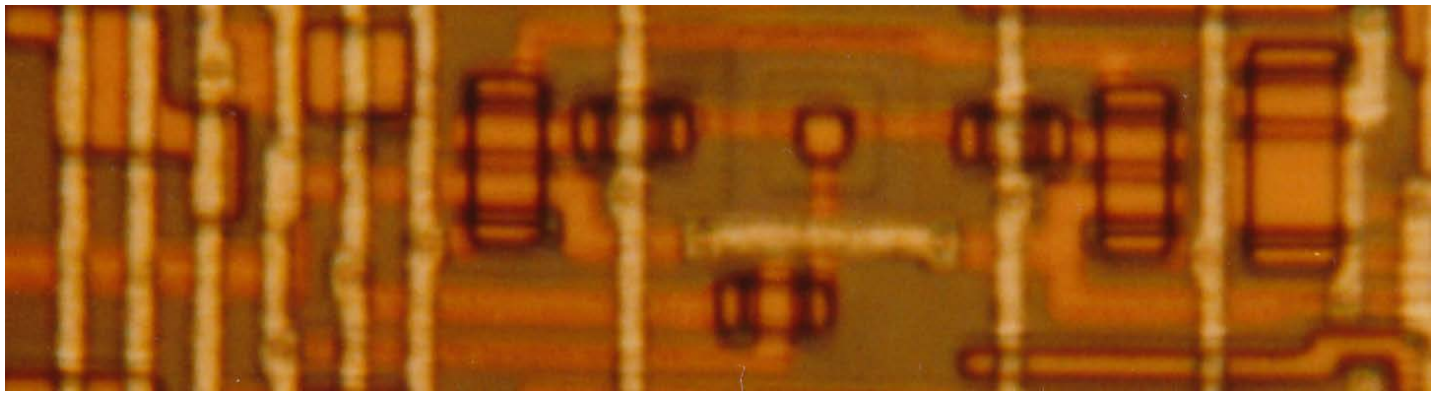



Vnwell = 2 V

# Point resolution: larger pitches

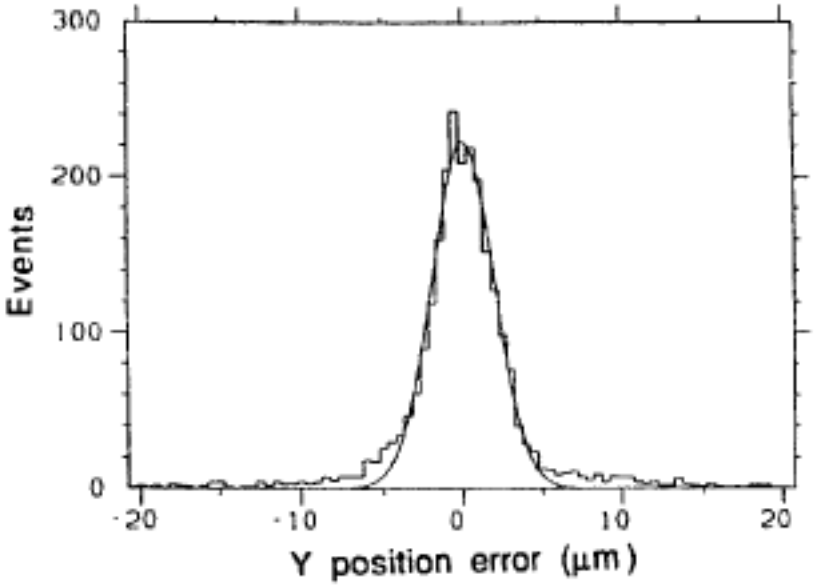
2 μm CMOS

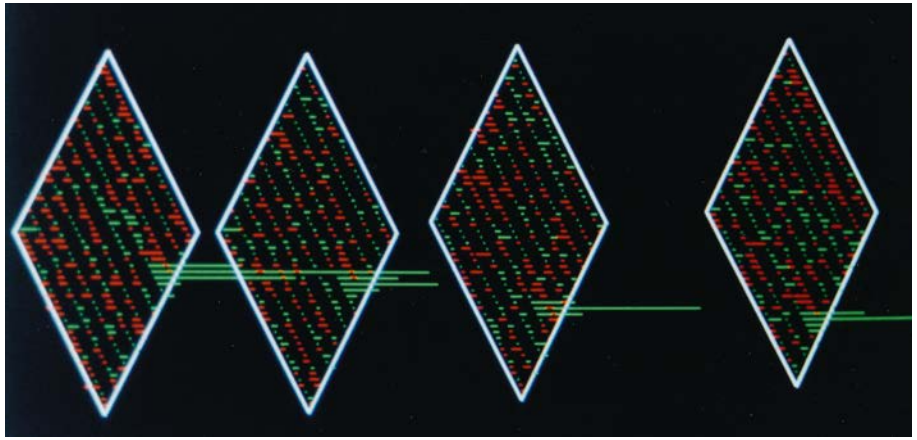


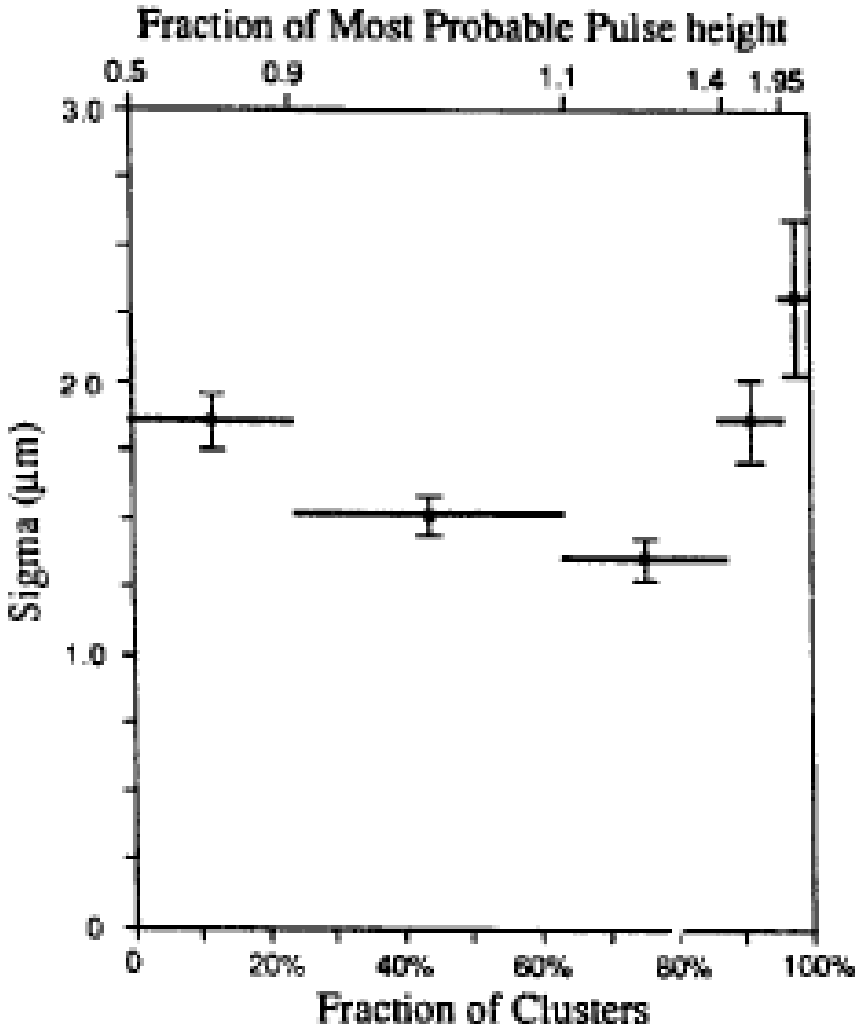



C. Kenney et al. NIM A 342 (1994) 59-77

# Point resolution: larger pitches

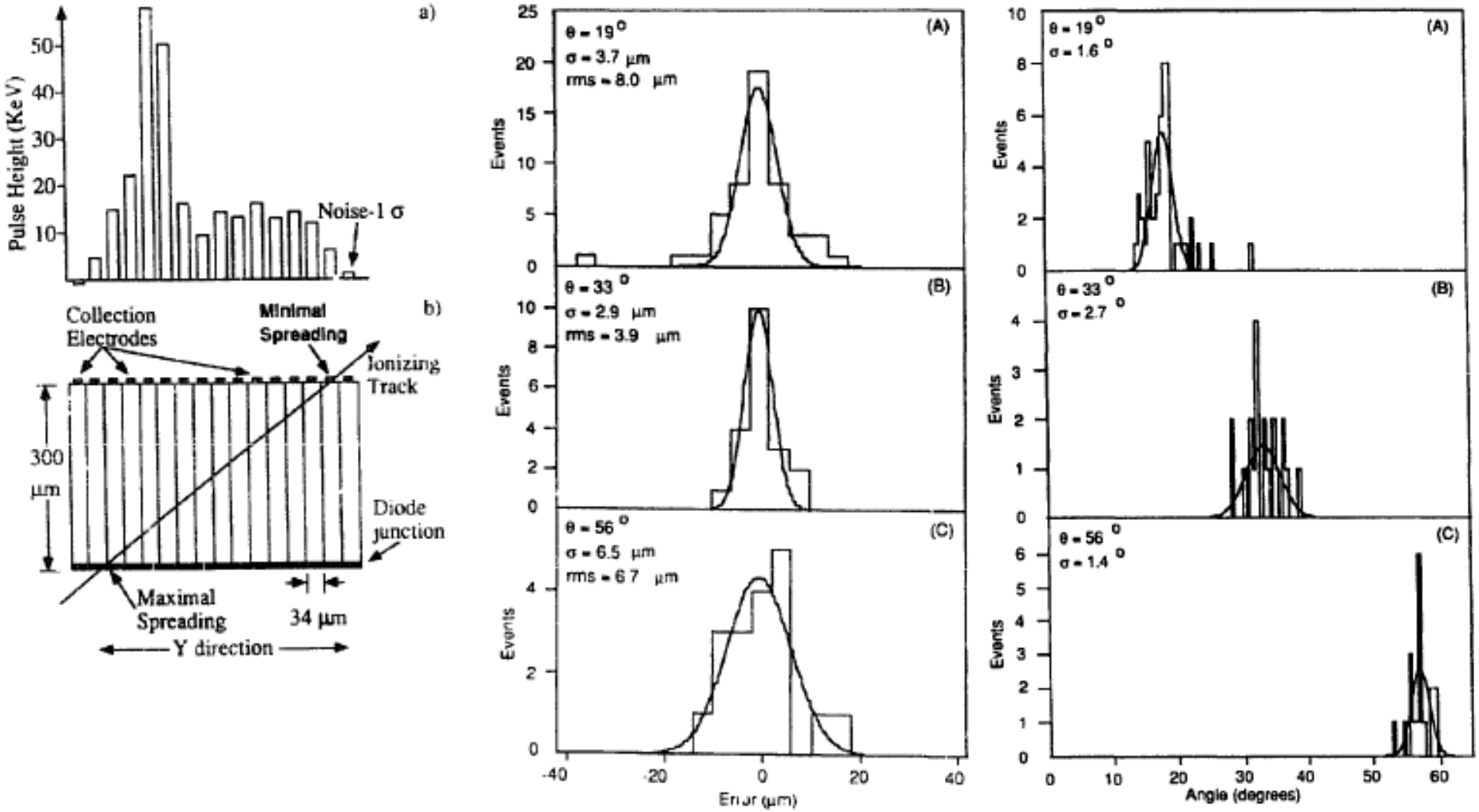





$Q_{most\ probable}$ = 4fC C=26fF P-type 1E12 $cm^3$ $S/N_{single\ ch}$= 150/1

# Point resolution: tracks at an angle




Average of extreme pixels in the cluster gives better results

In this case signal (and S/N) for a single channel reduces with track inclination

# SINGLE POINT RESOLUTION

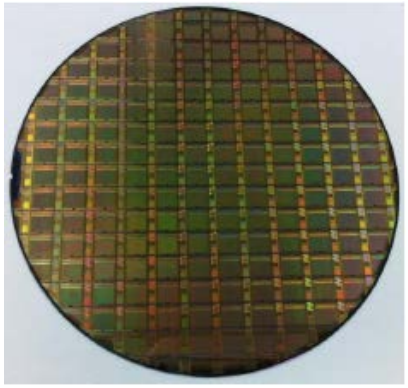
- Thick detectors have approached ~ 1µm point resolution using analog interpolation with better signal to noise than thin detectors due to a larger signal and the more prominent charge sharing, but position resolution often reduces for severely inclined tracks due to the reduced S/N.

- Thinner detectors may need increased granularity to achieve such resolution, especially with binary readout on the condition they achieve sufficient S/N. The evolution of CMOS technology should provide sufficient density for granularities of 10x10 microns or even less.

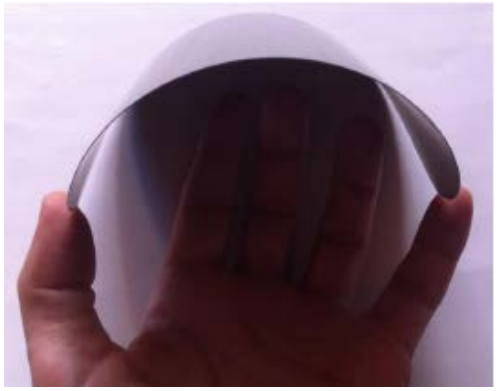
- Unless S/N is very large, detector depth and pixel pitch should be comparable to avoid S/N degradation and hence resolution for inclined tracks.

- High granularity realistic over large surface ? -> main challenge is digital power consumption

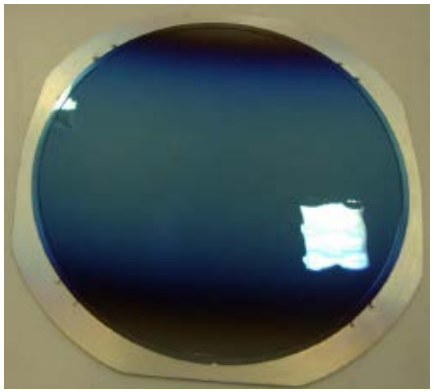
# OTHER WAYS TO OBTAIN JUNCTION ON THE BACK



Finished CMOS wafer on high resistivity



Wafer thinned to 50 um



Thinned wafer with anti-reflective coating

Chip mounted in camera

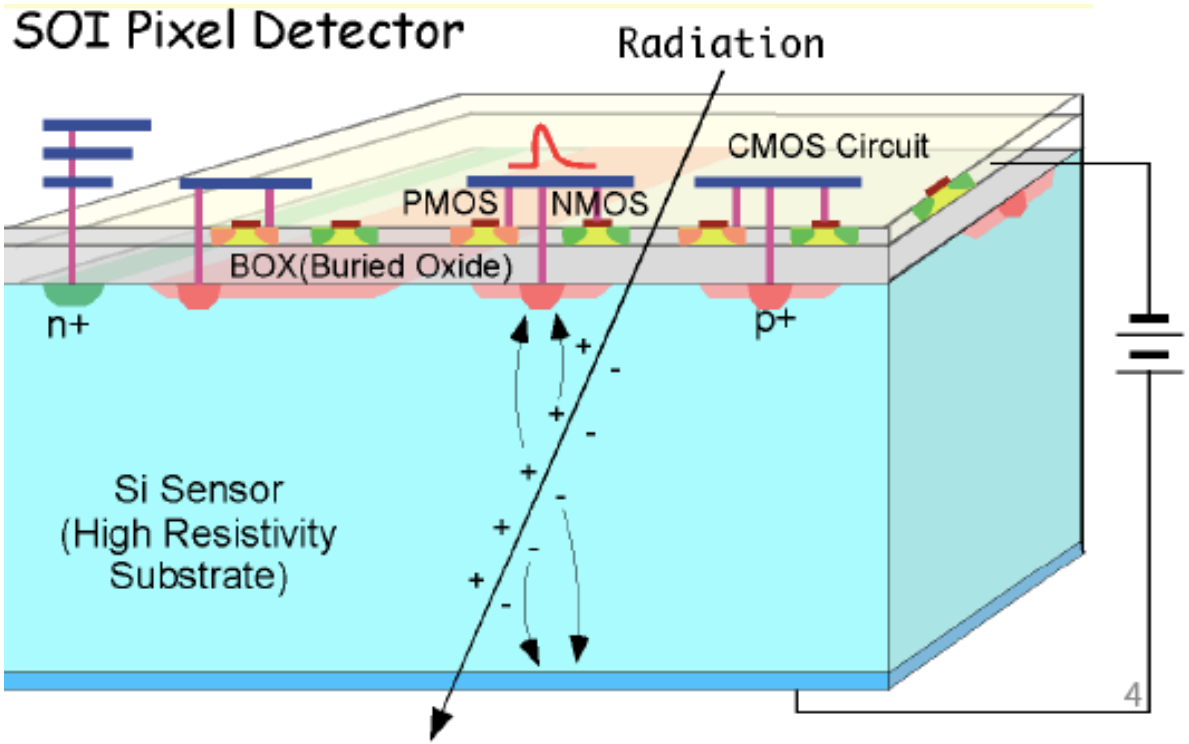
Example: post CMOS wafer thinning & back-side processing

S. Lauxterman CPIX14

Image (raw data)

- several similar developments
- other possibility epi of opposite type as substrate
- In general:
  - Watch die edge/junction termination
  - Radiation tolerance to be investigated/confirmed

# Silicon on Insulator (SOI)




Y. Arai et al

Very impressive technology development … offers good Q/C

BOX causes reduced radiation tolerance, double BOX likely to improve this.

# Just a few remarks on PROCESSING

- CMOS standard processing now on 200 or 300 mm diameter wafers
- Processing very high resistivity silicon has some particularities:
- High resistivity (detector grade) to be found at larger diameter
- Float-zone silicon has many less impurities/defects than Czochralski. These defects pin down dislocations, rendering the material more robust. Float-zone material is MUCH MORE FRAGILE
- Several process steps can introduce impurities increasing detector leakage
  - Work at higher leakage current (often quickly dominated by radiation induced leakage anyway)
  - Try to make certain steps cleaner
  - Use gettering techniques, which during processing render defects more mobile and provide traps for these where they are no longer harmful.

More technologies interesting for particle detectors become available
also with high resistivity epitaxial layers
3D assembly might provide 'holy grail' of monolithic
significant progress recently(eg SOI development, quadruple well technology)

# MONOLITHIC DETECTORS

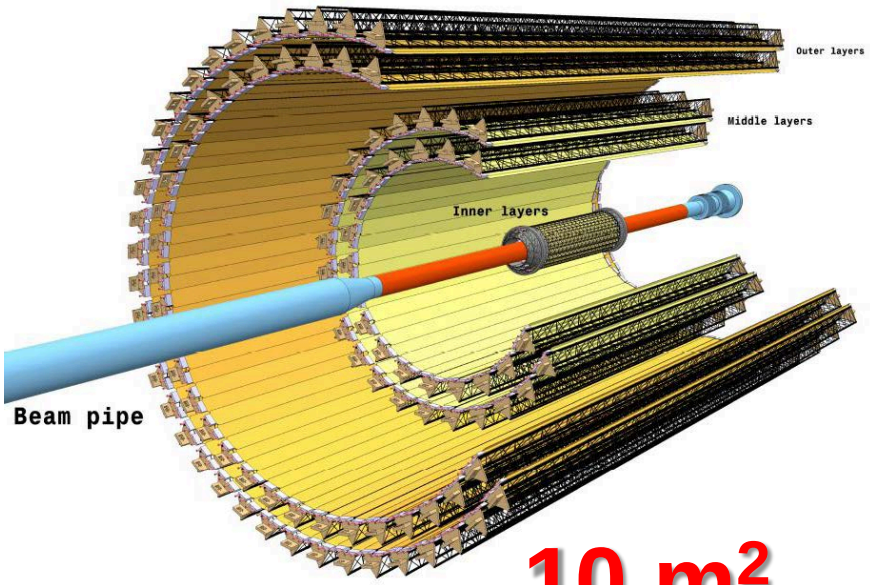
- Clearly have transformed the world of photography and imaging in general
- Very significant progress even recently, eg subelectron noise by multiple correlated sampling (eg. S. Kawahito, pixel2012).
- Presented noise performance, the possibility to simulate and design the device, different approaches for the device, the influence of reverse bias on radiation tolerance and cluster size

- In High Energy Physics:
  - Already adopted for two experiments (Belle-II and STAR)
  - Now also adopted at LHC for ITS upgrade in Alice using quadruple well technology, less stringent requirements for radiation tolerance and speed, but high occupancy numbers
  - A possible option in CMS, in Atlas HV CMOS also considered for use as a smart sensor -> next presentation

# MONOLITHIC DETECTORS for HEP

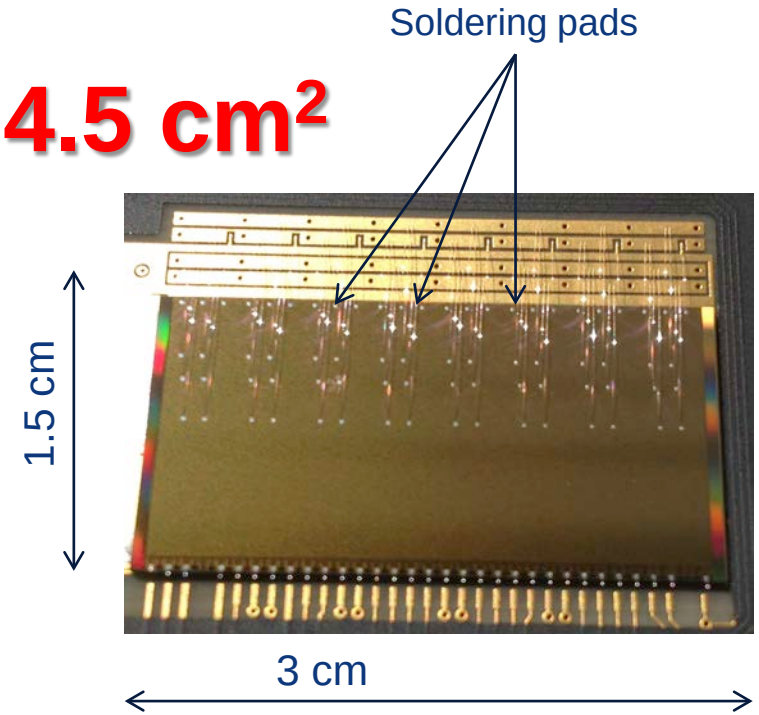
- More processes interesting for high energy physics become available
- Power consumption: Approaching digital signal from particle hit => ultimately eliminate analog power
  - Need sufficient and uniform depletion/collection depth and small collection electrode for sufficient Q/C
  - Need appropriate architecture to match or improve present day power consumption (Pixels ~200 mW/cm$^2$,trackers ~20 mW/cm$^2$). Clock distribution to every pixel will eat significant fraction of the total power budget
  - Need to reduce power to transmit the data off-chip, may well be ultimate limit.
- Radiation tolerance very challenging for inner layers but promising results with HV CMOS and other developments
- Not ready at the time of LHC detector construction, but might get there for some of the upgrades.

# ALICE ITS UPGRADE: 12.5 Gpixels




**10 m²**

**4.5 cm²**

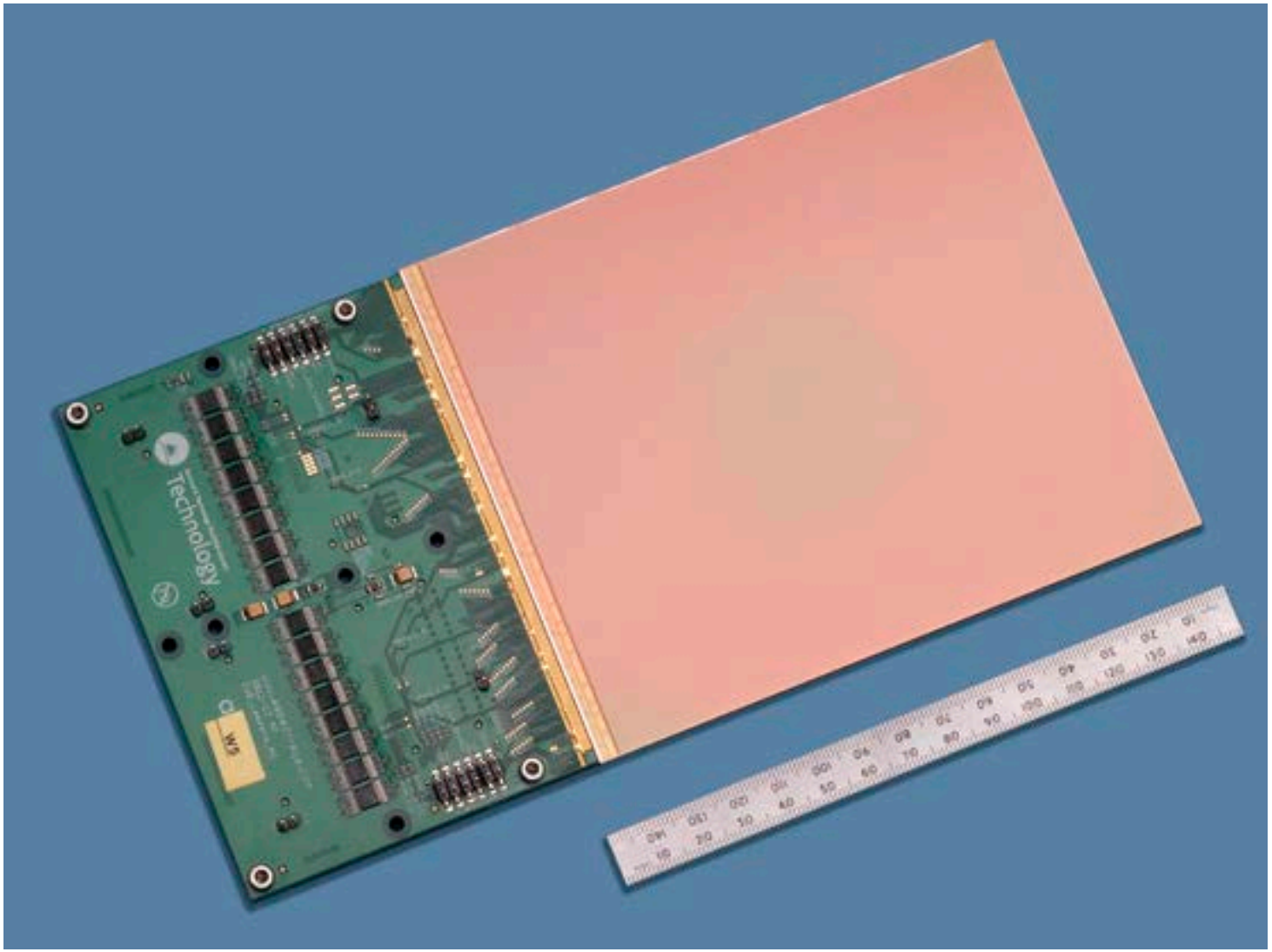



- Construct 7 layers (3 inner layers, 4 outer layers) 10 $m^2$ from 4.5 $cm^2$ chips
- Would like to increase size of building block…
- ~ 500 000 pixels of 28 x 28 $\mu m^2$

# WAFER SCALE INTEGRATION by STITCHING

*Here 200 mm wafer*

*300 mm now in volume production ($10^6$ wafers/year/fab)*




*Courtesy: N. Guerrini, Rutherford Appleton Laboratory*

# Think about new assembly techniques

*Can we exploit flexible nature of thin silicon ?*

*Can we match or better approach volume production capability of semiconductor foundries (~3000 wafers a day) in our module assembly ?*

*Silicon Genesis:*
*20 micron thick Si wafer*

# THANK YOU

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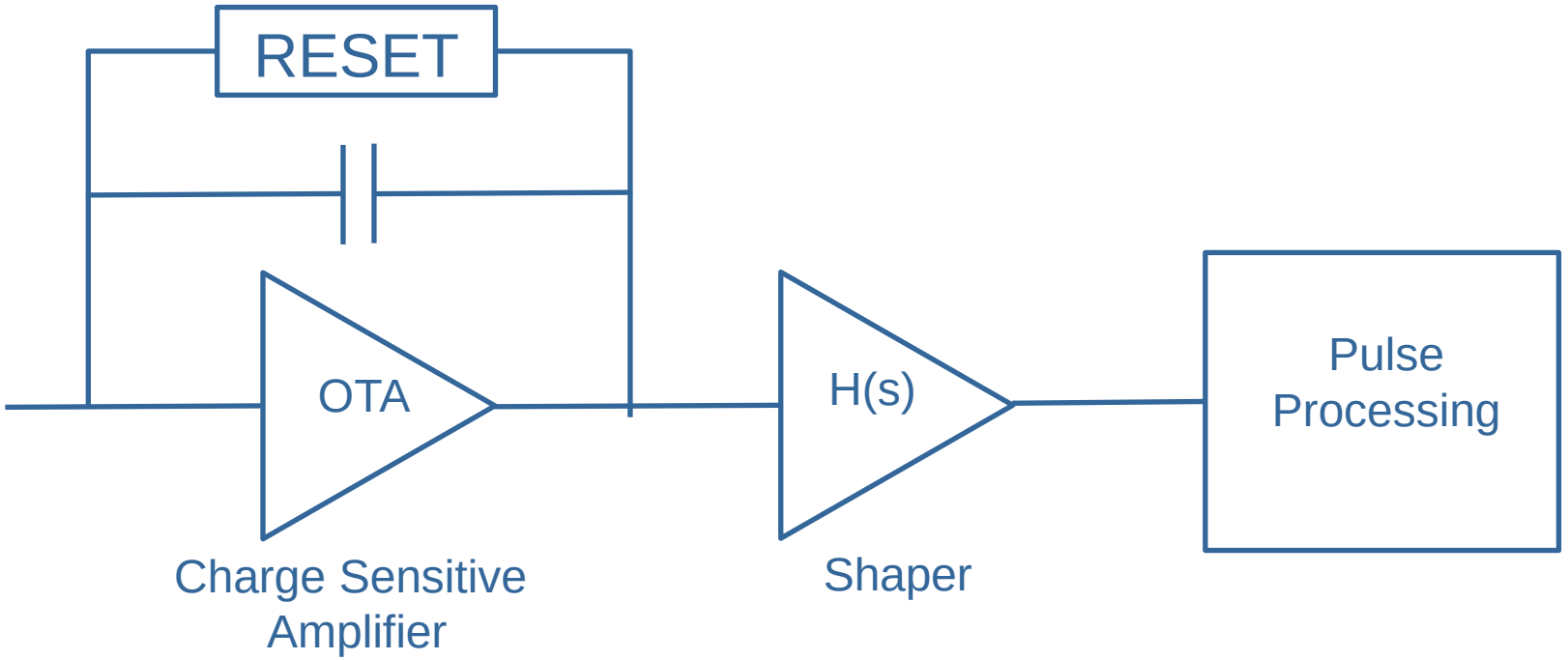
# BACKUP SLIDES

# Standard charge sensitive pulse processing front end
## (no integration over a fixed time)




ENC: total integrated noise at the output of the pulse shaper with respect to the output signal which would be produced by an input signal of 1 electron. The units normally used are rms electrons.

RESET: switch or high valve resistive element

# 'standard' front end noise equations

$$ENC_{TOT}^2 = ENC_d^2 + ENC_f^2 + ENC_0^2$$

*where*

Transconductance gm related to power consumption

thermal

$$ENC_d^2 = \frac{4\gamma kTC_t^2}{gmq^2\tau_s}.X(n) \qquad X(n) = \frac{B(\frac{3}{2}, n-\frac{1}{2})n}{4\pi}(\frac{n!^2\, e^{2n}}{n^{2n}})$$

1/fnoise

$$ENC_f^2 = \frac{KF_F}{C_{ox}^2 WL}\frac{C_t^2}{q^2}.Y(n) \qquad Y(n) = \frac{1}{2n}(\frac{n!^2\, e^{2n}}{n^{2n}})$$

shot noise

$$ENC_o^2 = \frac{2qI_o\tau_s}{q^2}.Z(n) \qquad Z(n) = \frac{B(\frac{1}{2}, n+\frac{1}{2})}{4\pi n}(\frac{n!^2\, e^{2n}}{n^{2n}})$$

Ref.: Z.Y. Chang and W.M.C. Sansen : ISBN 0-7923-9096-2, Kluwer Academic Publishers, 1991

# INFLUENCE OF SHAPER ORDER N

| n | 1.00 | 2.00 | 3.00 | 4.00 | 5.00 | 6.00 | 7.00 |
|---|---|---|---|---|---|---|---|
| X(n) | 0.92 | 0.85 | 0.95 | 1.00 | 1.11 | 1.17 | 1.28 |
| Y(n) | 3.70 | 3.41 | 3.32 | 3.28 | 3.25 | 3.23 | 3.22 |
| Z(n) | 0.92 | 0.63 | 0.52 | 0.45 | 0.40 | 0.36 | 0.34 |

- Ref.: Z.Y. Chang and W.M.C. Sansen : ISBN 0-7923-9096-2, Kluwer Academic Publishers, 1991
- Ref. 2 : V. Radeka “Low-noise techniques in detectors” Ann. Rev. Nucl. Sci. 1988, 38, 217-77
- Ref. 3 : E. Nygard et al. NIM A 301 (1991) 506-516

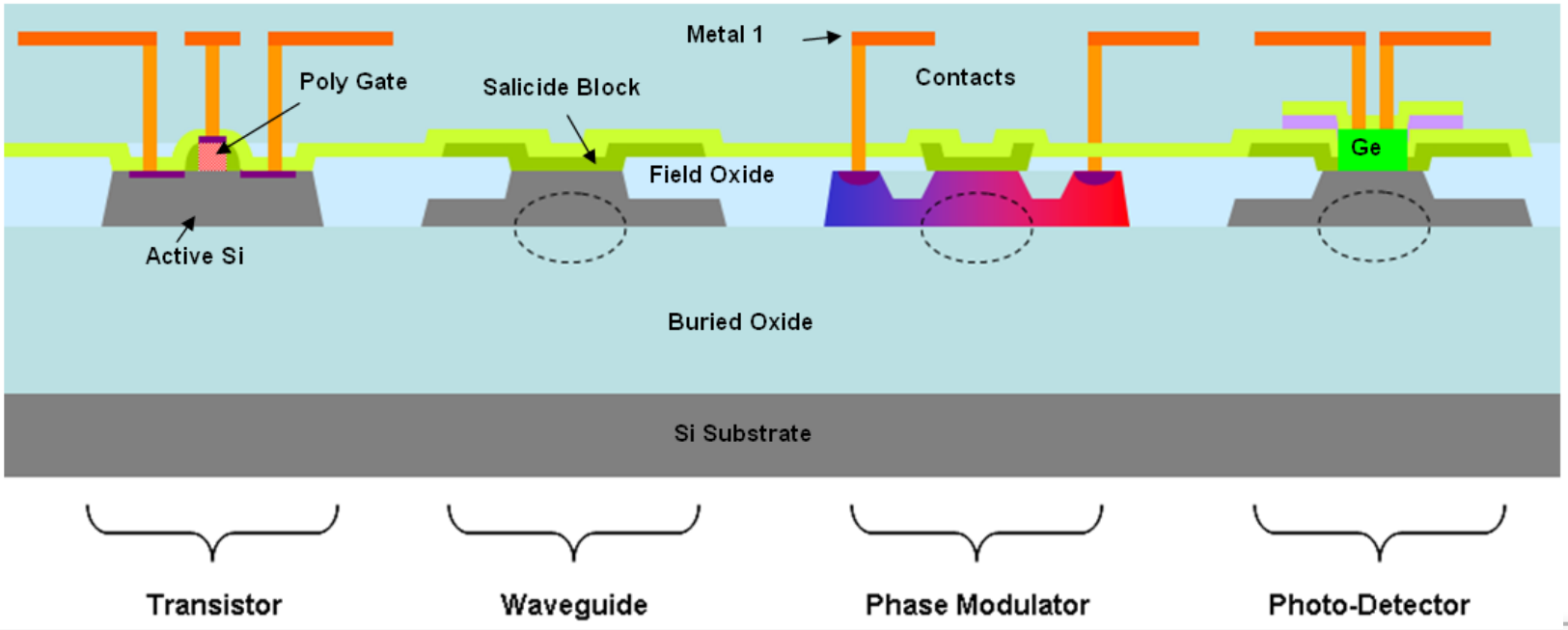
# SILICON PHOTONICS: A PARADIGM CHANGING TECHNOLOGY

Silicon

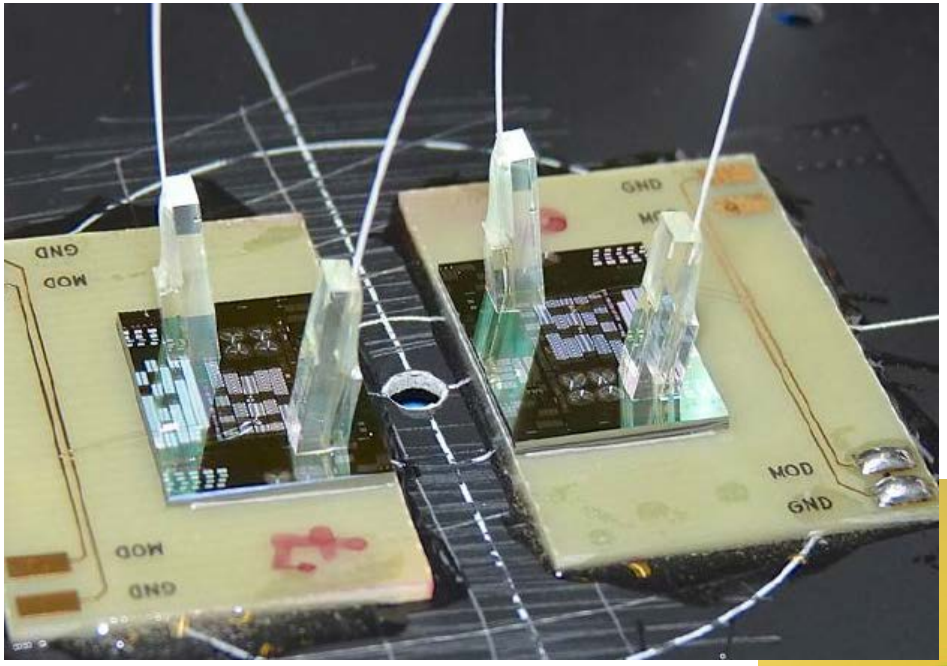
- Excellent optical material with high refractive index (but indirect bandgap)
- Widely available in high quality grade
- Can be processed with extreme precision using techniques from deep submicron CMOS techniques.

- So, why not build a photonic circuit in a CMOS Si-wafer

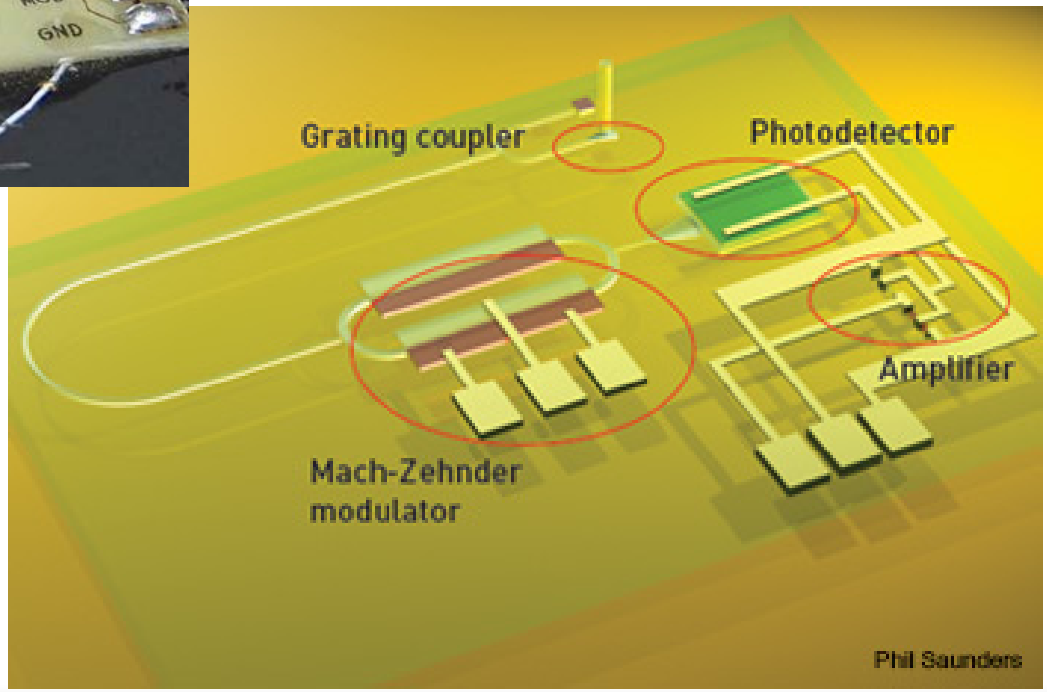
  (and eventually connect it to a CMOS signal processing circuit)



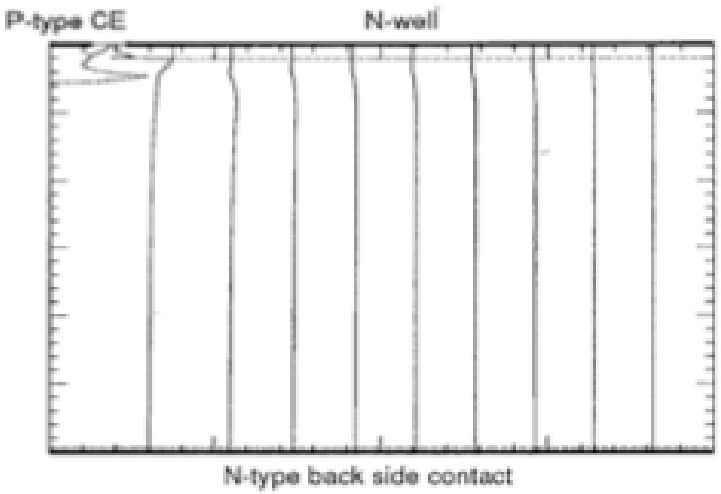
# SILICON PHOTONICS




First evaluations, designs and developments are now ongoing at CERN

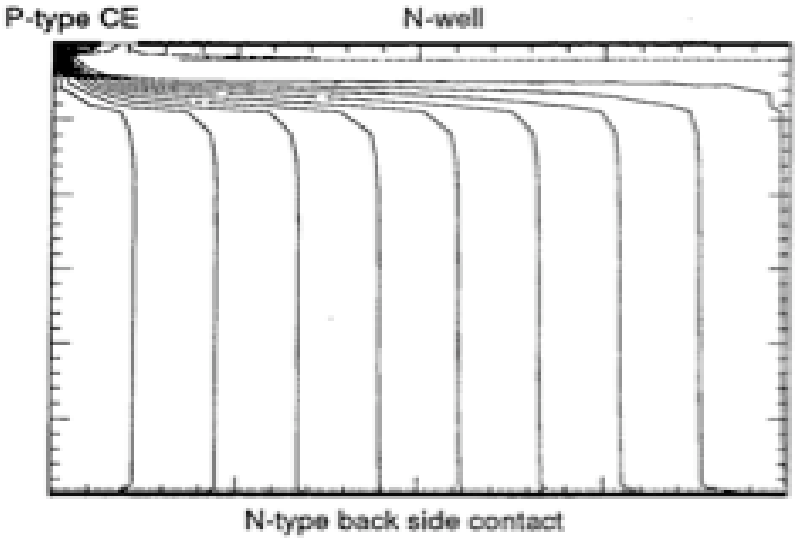


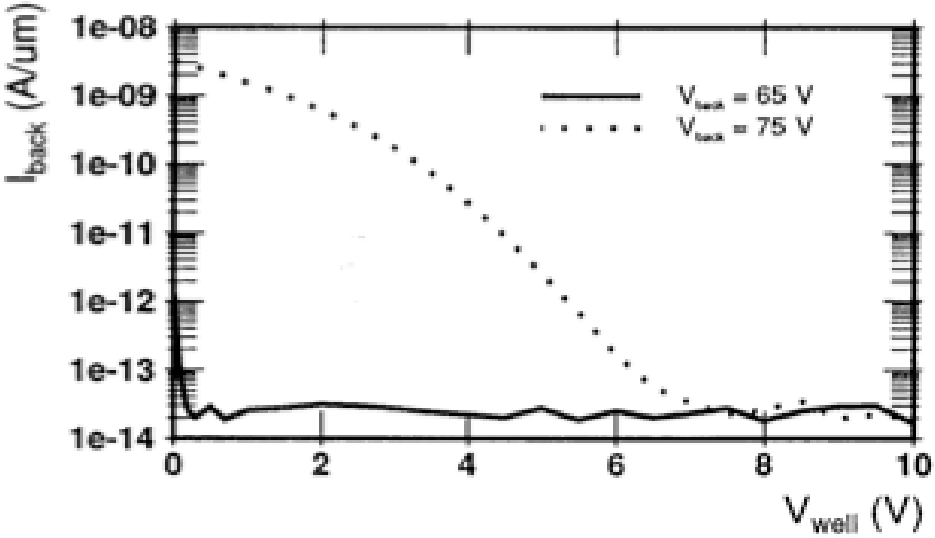
# USE OF A WELL with BACK SIDE JUNCTION
## Example of device design and simulation




- P-type collection electrode covers 1/10 of the width.
- Full depletion required (otherwise short between the collection electrodes)
- At zero well bias and full depletion punchthrough between Nwell and N-diffusion on the back

# USE OF A WELL with BACK SIDE JUNCTION
## Example of device design and simulation




- A few volts on the well (with 65 V on the back) diverts all flow lines to the collection electrode because a potential barrier is formed underneath the well.
- The back side to Nwell current drops by orders of magnitude as the punchthrough is eliminated.

# USE OF A WELL with BACK SIDE JUNCTION
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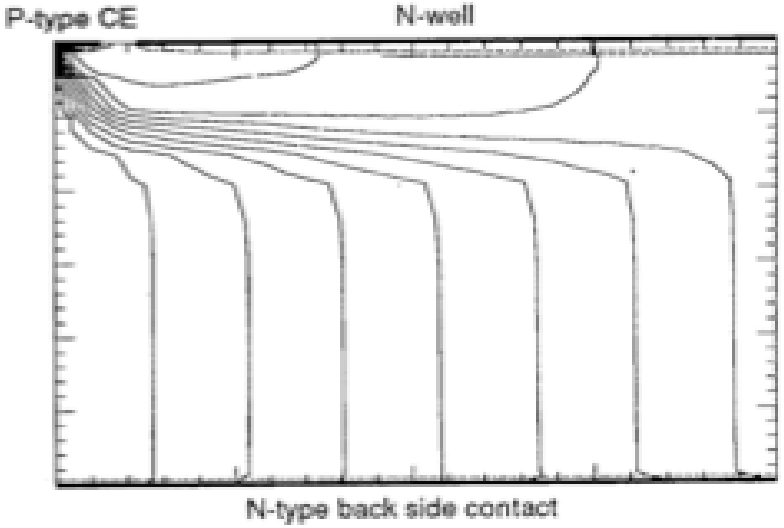


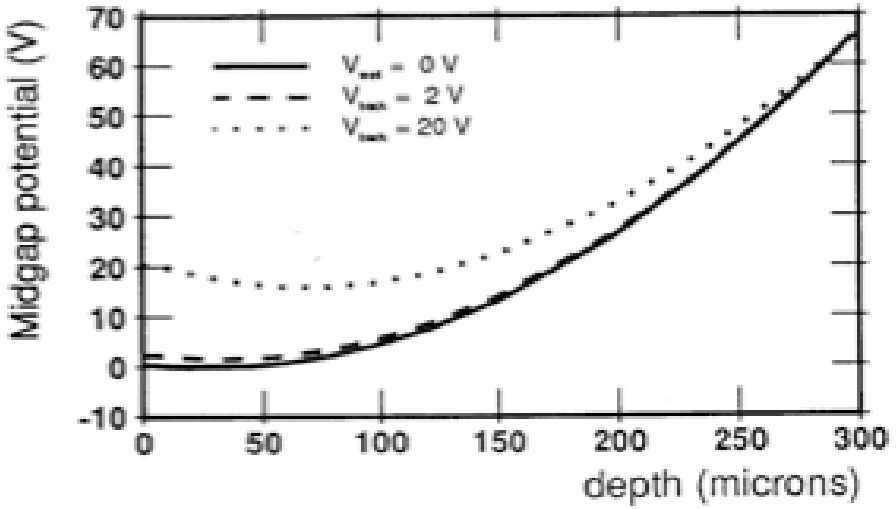


- Increasing the well bias increases the potential barrier and moves the potential valley deeper into the substrate

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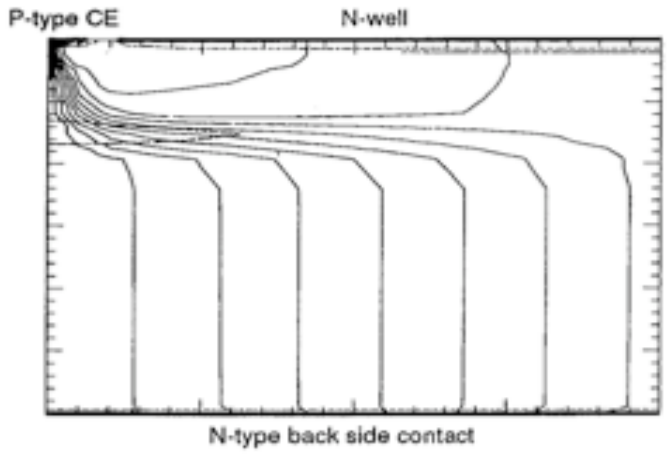


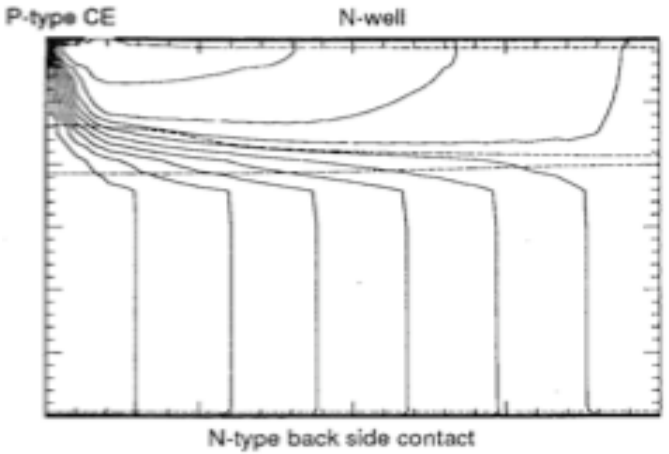


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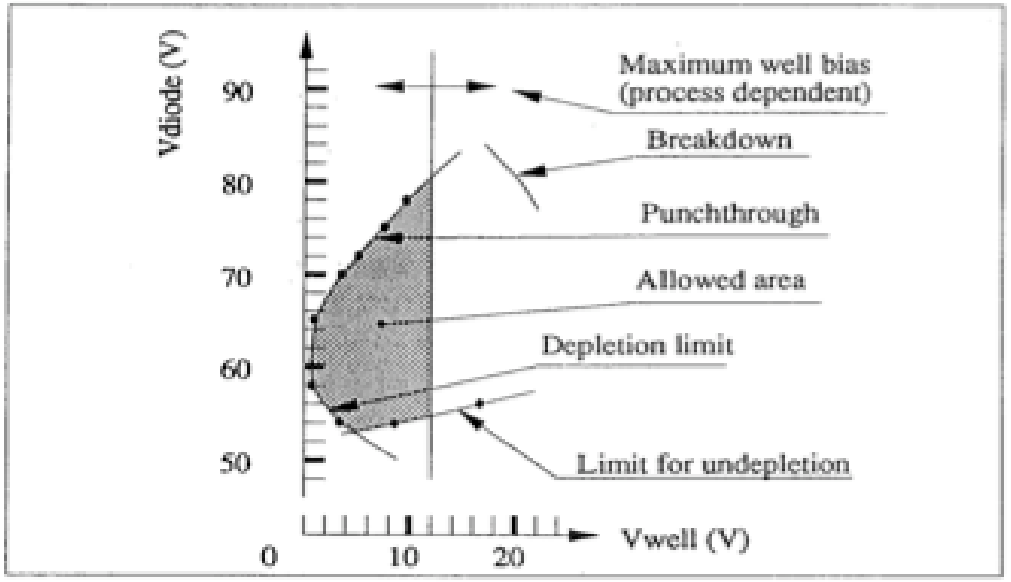
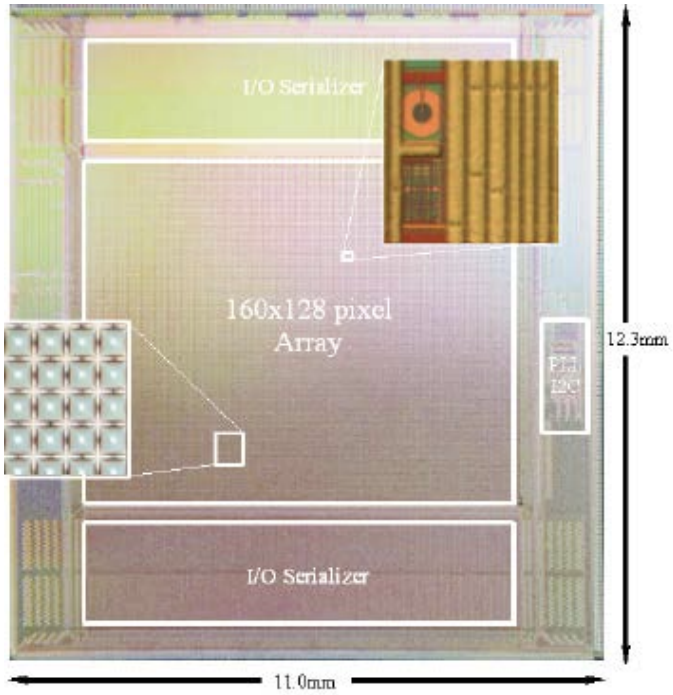
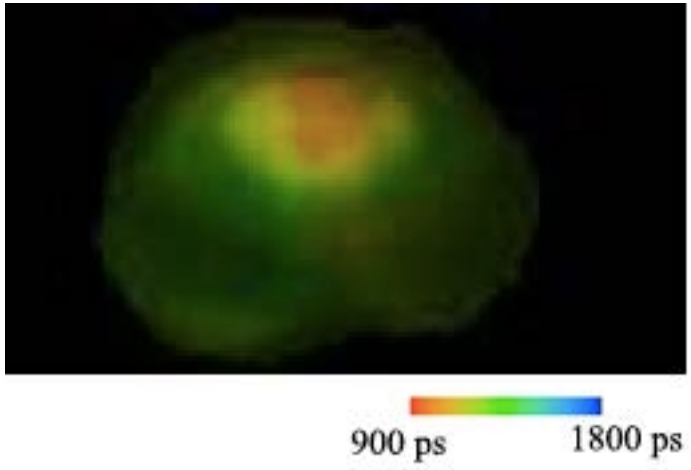



Operational limits

# Silicon Avalanche Diodes




- Single photon avalanche diodes (SPAD)
- E. Charbon et al ISSCC 2011

- Large and fast signals, radiation tolerance to be investigated further
- TOTEM experiment is looking at avalanche photodiodes as one of the possibilities to try to reach 10 picoseconds in its Roman Pots
- One nice development by Sebastian White et al.(separate APD matrix)