RD_FASE2 Pixel Common ATLAS/CMS

23 September 2014

G. Darbo – INFN / Genova

On behalf of ATLAS Tracker RD_FASE2

Slides to pick-up material for the presentation of common ATLAS / CMS Tracker R&D.

Indico agenda:

https://agenda.infn.it/conferenceDisplay.py?confId=8544

2014 Activities

- ***2014:*** *CSN1 funded (Feb and May) R&D Phase 2 activities for ATLAS & CMS inner trackers.*
  - Development of 3D and Active Edge sensors with FBK – 3 Batches (ATLAS/CMS)
  - Bump-bonding: development of Indium bumps (6" sensors) and produce modules
  - Develop a technology for pixel detector hybridization using ***C*** (dielectric) instead of ***R*** (bump-bonding) coupling
  - Completion of CO_2 test plant (combined ATLAS / LHCb)

Assigned on	Sezione	Category	ATLAS/CMS/COMMON	Assigned	Description
Feb 2014	GE	3D	COMMON	21 000	Wafer for 3D sensors (common with CMS)
Apr 2014	GE	3D	COMMON	44 000	3 processes at FBK: 2 committed with MEMS3
May 2014	GE	HV	ATLAS	13 000	HV-CMOS Hybridization + 3 FE-I4B wafers
May 2014	MI	BB	ATLAS	27 000	BB of 3D (IBL design on 6") + 3 FE-I4B wafers
May 2014	MI	CO2/μ-CH	ATLAS	20 000	TRACI: co-funded with LHCb
				125 000	

2015 Activities

***2015:** Activities and line of funding*

- **Continue with 3D Sensor plan:** produce modules, test in lab and TB, irradiate, procure sensors for next FBK run.
- **Bump-bonding:** for testing FBK sensors and to develop for future RD53 requirements (high-density bump-bonding with indium)
- **CO_2 cooling:** contribute to ATLAS stave R&D, thermal simulation and test with CO_2 plant
- **Multi-module R/O:** use leading experience of ROD designer (BO) to develop a 16 module table-top road for architecture study and for test-beam application.
- **Upgrade to USBPix3:** most diffused single module system based on USB. Upgrade also for use if HV/HR-CMOS
- **HV/HR-CMOS:** presented a new project in CSN5 (BO, GE, MI)
- **CHIPIX65:** INFN interface to RD53 collaboration – Approved as CSN5 Call (Sept.2013)

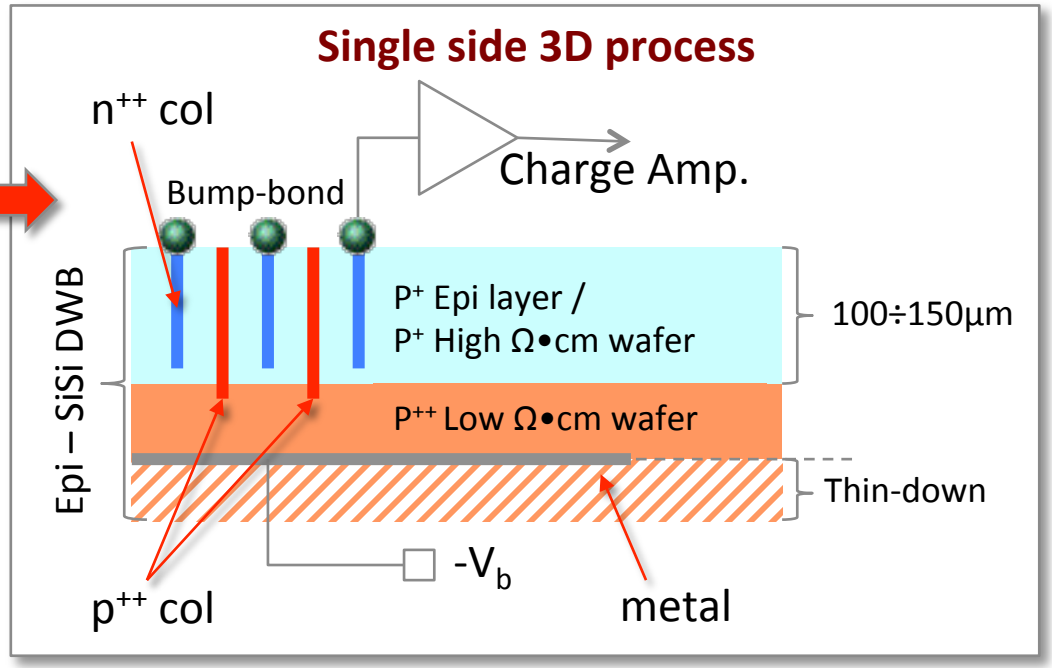
3D Sensors

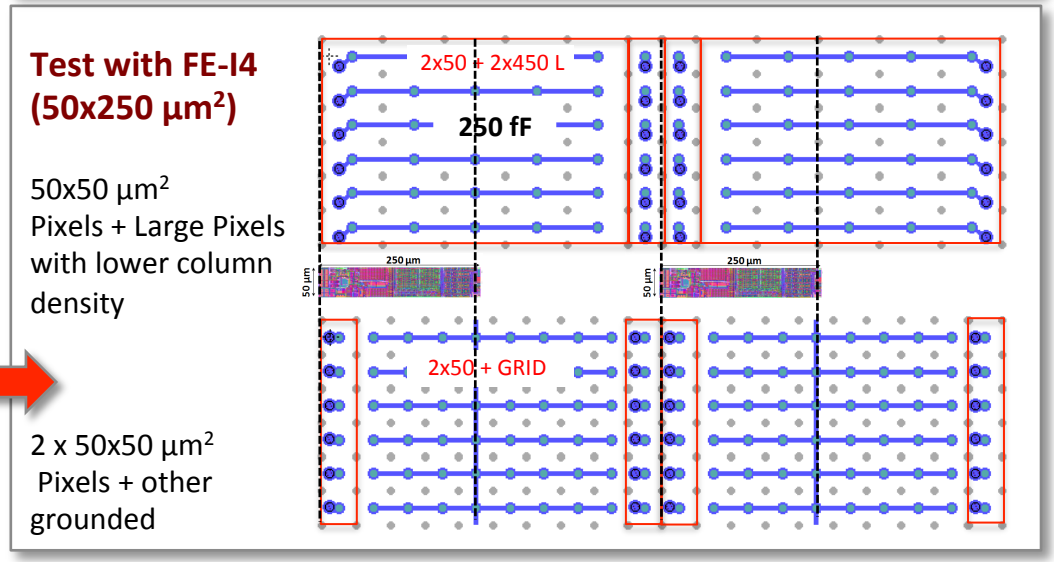
- *3D Sensor development with FBK*
  - p-bulk sensor on 6” wafers
  - Active volume: FZ on SiSi or Epi
  - Active thickness: 100/130µm
  - Single-side process, bias on back

- *Test with:*
  - Batch 1: FE-I4, PSI46
  - Batch 2: (2016) RD53 chip

- *INFN Collaboration*
  - INFN-FBK under MEMS3
  - ATLAS: CS, GE, MI, UD, TN
  - CMS: BA, FI, MIB, PG, PI, TO

- *ATLAS Collaboration*
  - Common chip floorplan with producers: CNM, SINTEF/SNC
  - Testing: ATLAS 3D Sensor WG





RD53 Chip – Requirements on 3D Sensor

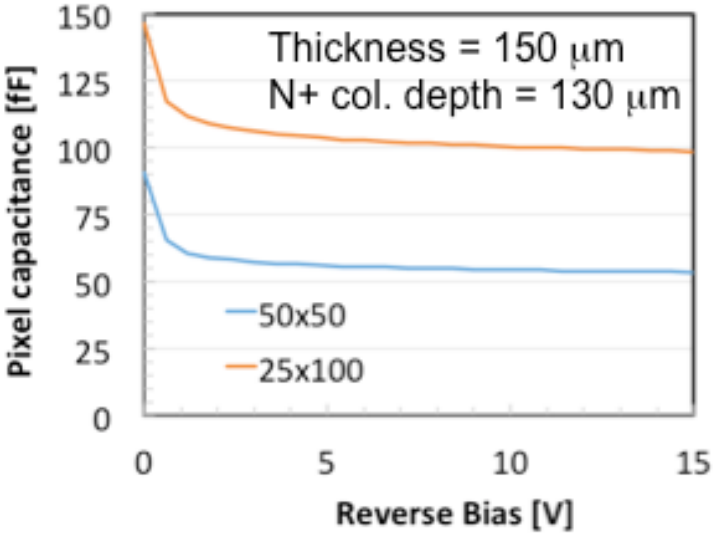
Next front-end chip generation (RD53 chip)

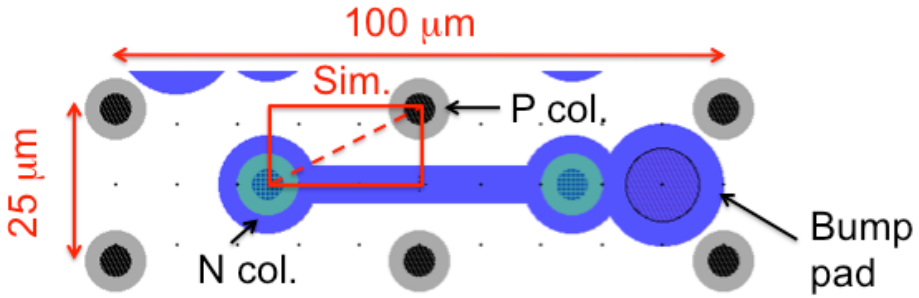
- 50x50 µm² pixels (also 25x100 µm²)
- $C_{DET} \leq 100$ fF
- $I_{leak} \leq 5$ nA/pixel (if no amp. compensation)
- Threshold: 1000 e (possible?)

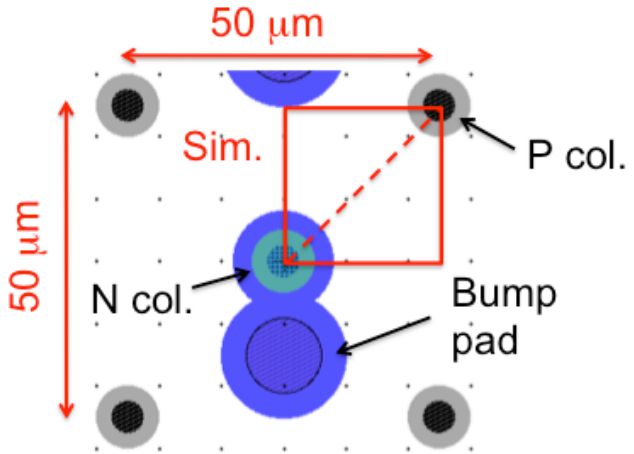
3D Sensors

- 50x50 µm² pixels best option (25x100 µm² difficult layout – too little clearances)
- Simulated capacitance (150 µm thick): 50 fF
- Expected charge 3200 – 3700 e (in 100 µm thickness) after $2x10^{16}$ n_{eq}/cm^2 – simulated and "extrapolated" values.

Ref. G.F. Dalla Betta, IFD 2014, Mar 2014, Trento, IT.







Ref. G. Darbo, Pixel2014, Niagara Falls, Sept. 2014.

3D Sensor Program – 2014/15

Planned 3 run at FBK in 2014 – Funded by CSN1 in Feb 2014

- Batch.1: DRIE process setting up for thin columns. Process in completion. Found that 5-6 µm are the best suitable column diameter.

- Batch.2: test planar process with SiSi DWB and Epi substrates. Layout completed, mask submission, wafer expected in 6 weeks.

- Batch.3: 3D single side process with SiSi DWB and Epi substrates. Layout in discussion. Compatible layout with other foundries (CNM) to simplify common test of devices.

Activity	2014												2015						No. of
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	Litho
Feasibility of <10µm columns																			3
Test SiSi DWB / Epi substrate - planar process																			5 + 1
3D full process on SiSi DWB / Epi substrate																			11
																		Total	***20***

Schedule presented in Feb'14.
Still up to date.
Need approval from MEMS3 committee of 3rd batch!

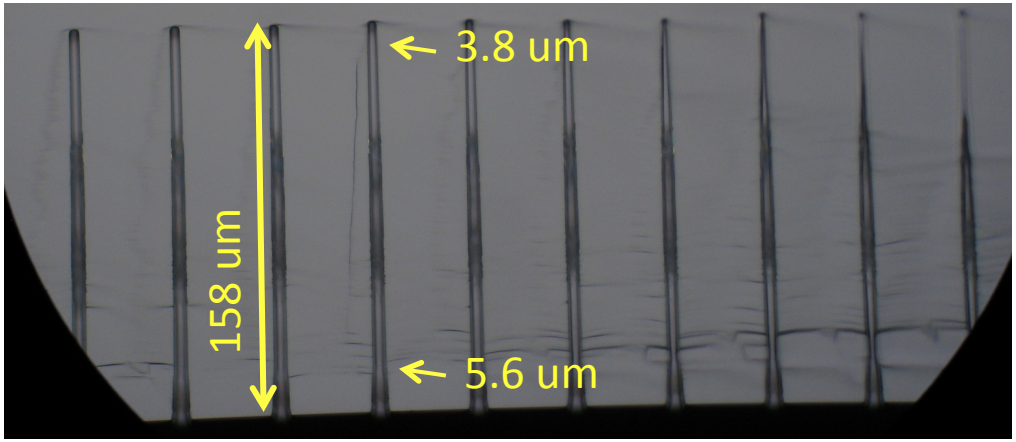
Note:

- A second 3D run is foreseen at the end of 2015 / early 2016 – layout matching RD-53 layout.

FBK: Status of Batches

- ***Batch 1:*** *study of columns*

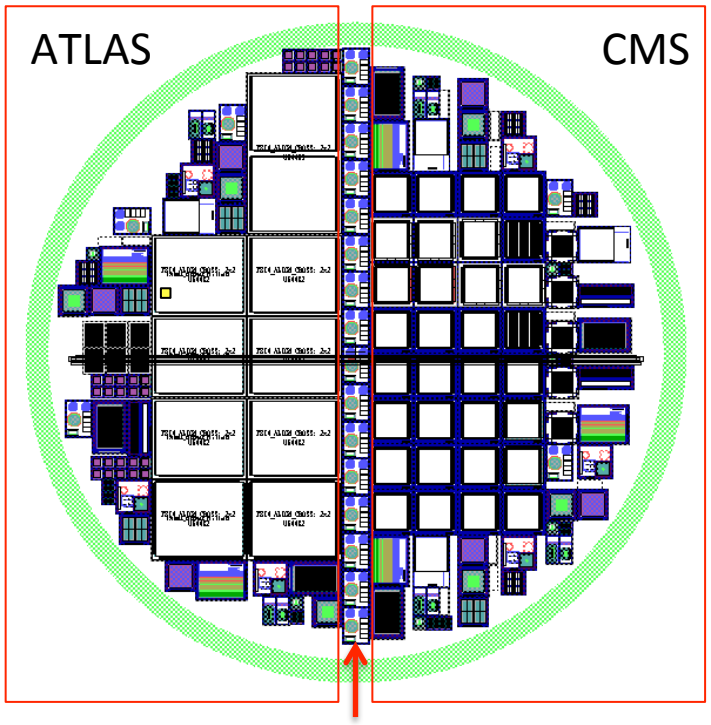
  In measurement



Ref.: M. Boscardin and S. Ronchin, FBK

- ***Batch 2:*** *study SiSi subtrates*

  Mask submitted



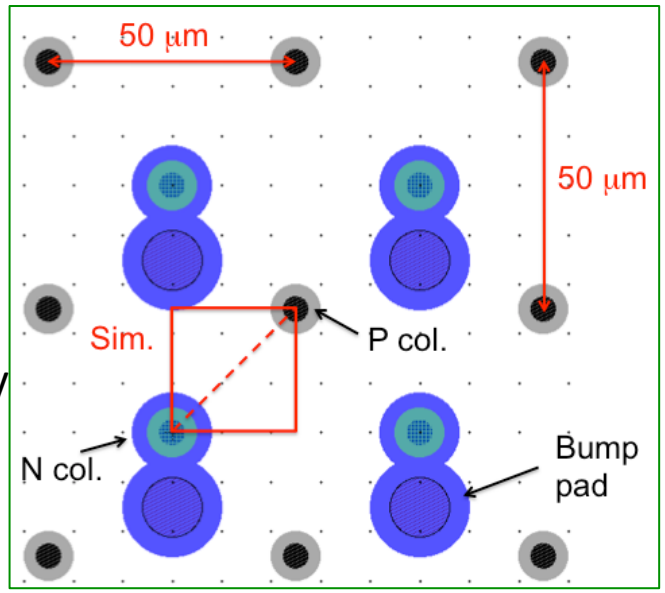
Test structures for Si-Si qualification

- ***Batch 3:*** *3D sensors*

Layout under study and Simulation of a 3D pixel cell

55 SiSi substrates from **Icemos** already available

Epi wafers from **Shinetsu** on order



3D – GE: Module Assembly, Irradiation, TB

- *Assembly 3D modules:*
  - To irradiate with p- and n-irradiation at $2x10^{16}$ n_{eq}/cm^2
    - FE-I4 heavily activate wit low energy neutron (from reactor) – Tantalum is present in technologies below 250 nm
    - FE-I3 has shown to resist neutron irradiation, no activation, better ToT measurement (7-bits instead of 4-bits)
  - Assembly using PCB (better for laser test) and flex hybrids
- *Irradiation plans with CMS and ATLAS 3D/Sensor community*
  - **Ljubljana** (reactor): can reach $2x10^{16}$, usable with FE-I3 – may need some gamma for p-spray activation (to increase breakdown)
  - **KIT** (Karlsruhe) 24 MeV protons (too high TID for reaching target NIEL dose – FE-I4 "suffers"),
  - **PS** (CERN) 24 GeV protons takes long time, but best equilibrium between TID/NIEL
- *Test beam: experience with EUDet telescope both in Desy and CERN*
- *Fund request:*
  - 10 k€ for module assembly, PCB, Irradiation, test-beam mechanics
  - consider ~ 30-40 modules assembled.

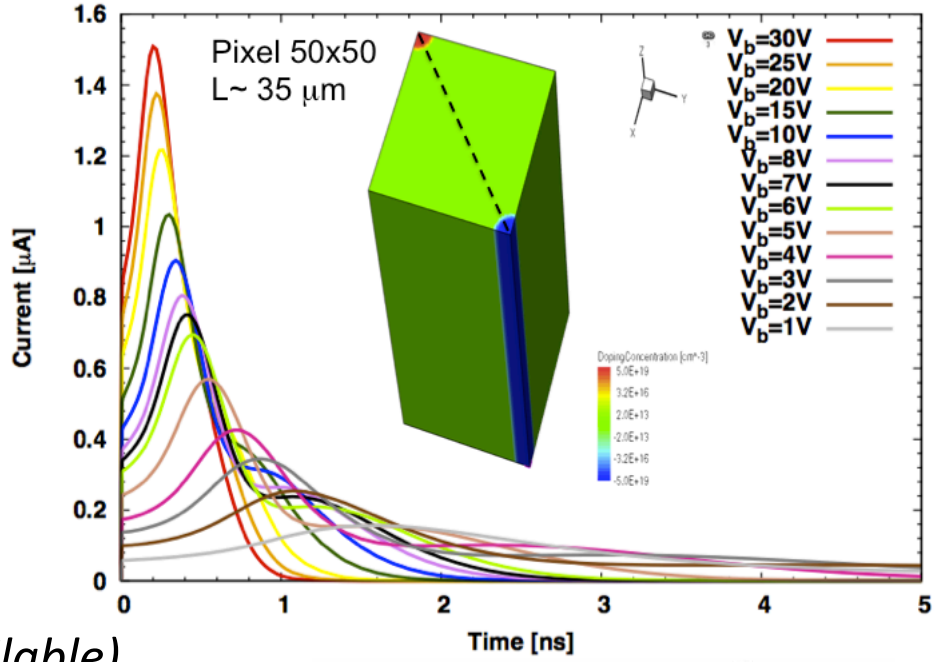
3D – TN: PicoScope

TN Involved in design, TCAD simulation and 3D diode structure measurements

- *New 3D design:*
  - electrode distance reduced
  - High speed signals (<1ns)

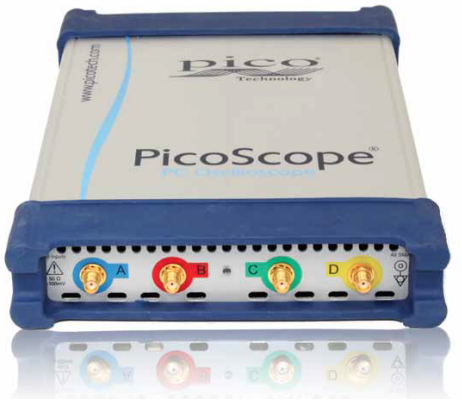
Need direct comparison between measurements and simulation to optimize design

TCAD simulation of mip on 50x50 pixel



- *Test on ad-hoc structures (OK)*
- *High speed laser (OK)*
- *High-bandwidth amplifier (OK)*
- *High sampling oscilloscope (not available)*

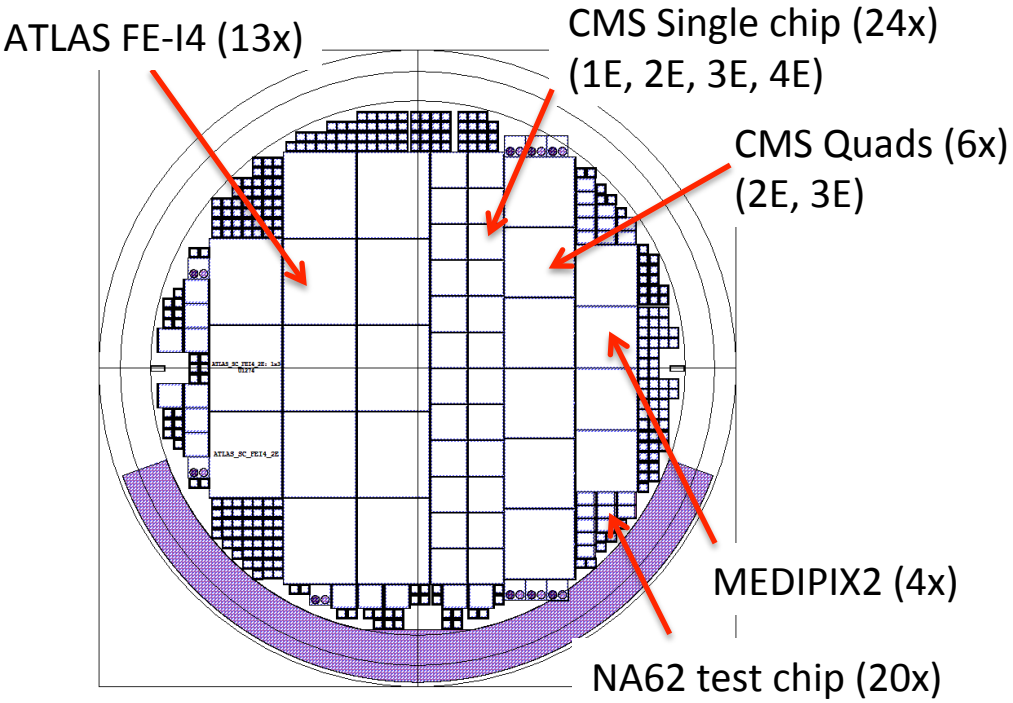
***PicoScope modules** (High speed A/D Converters with USB computer interface) are a valid sustainable cost alternative.*



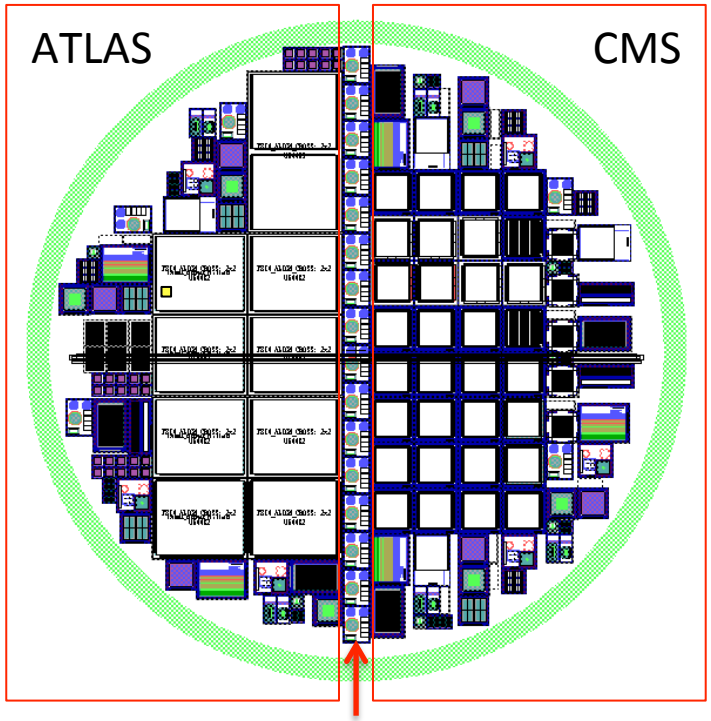
www.picotech.com

Bump-bonding Program

3D Double Side Batch



Planar ATLAS/CMS "Batch 2"



Test structures for Si-Si qualification

- *In program 4 sensor batches that would need BB in 2014/15:*
  - 3D double side – October - Funds (**MI**) assigned for 2014
  - Planar ATLAS/CMS Batch 2 – November – Funds (**TO**) assigned 2014
  - 3D and Active edge batches coming 2015 – no funds yet, fund request: **GE+FI**
  - Bumping at **IZM** and **Selex**: some money saving with available FE-I4/PSI with bumps from older productions
- *R&D on high density indium bumps*
  - Test on dummy wafers: high density (130k bumps/chip) – smaller bump <18μm diameter – fund request: **MI**

RD_FASE2 – "Richieste 2015"

Attività	Descrizione	BO	CS	GE	MI	TN	UD
3D	6" Wafer procurement (SOI, wafer bonding, epi)	-	-	-	-	10.0	-
	PicoScope 6407 Digitizer with 1.5 GHz probes and accessories.	-	-	-	-	8.5	-
BB	6" dummy wafers - test deposition on 6" and high-density bumps (150 k-bumps/chip)	-	-	-	20.0	-	-
	BB for 3D sensor test	-	-	24.0	-	-	-
MOD	Upgarde R/O Systems	-	2.0	2.0	2.0	-	2.0
	Module assembly and irradiation, RD on flex	-	-	10.0	-	-	-
MM-R/O	Multi module R/O	15.0	-	-	-	-	-
CO2/µCH	Develop µ-channel cooling	-	-	-	10.0	-	-
Total requested by ATLAS		**15.0**	**2.0**	**36.0**	**32.0**	**18.5**	**2.0**
		105.5					

- *Legend:*
  - ATLAS
  - Common ATLAS / CMS

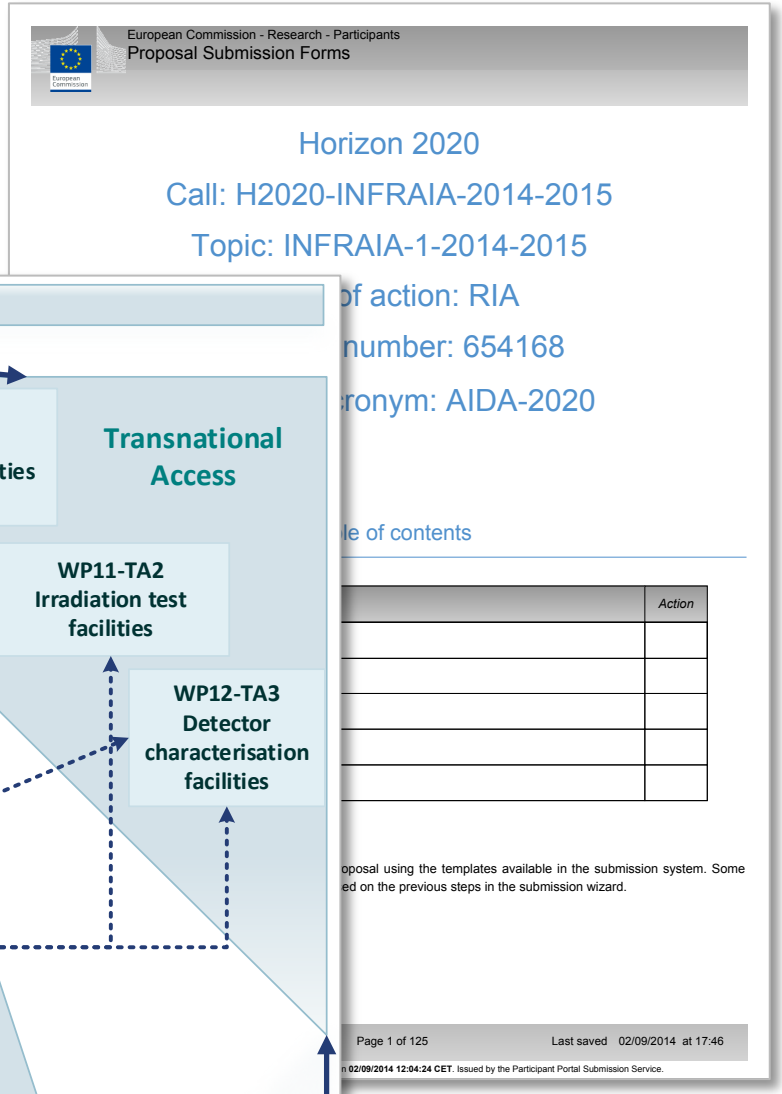
- *Trento:*
  - Request of **4 k€ of Travel Money** for test-beam participation and support.

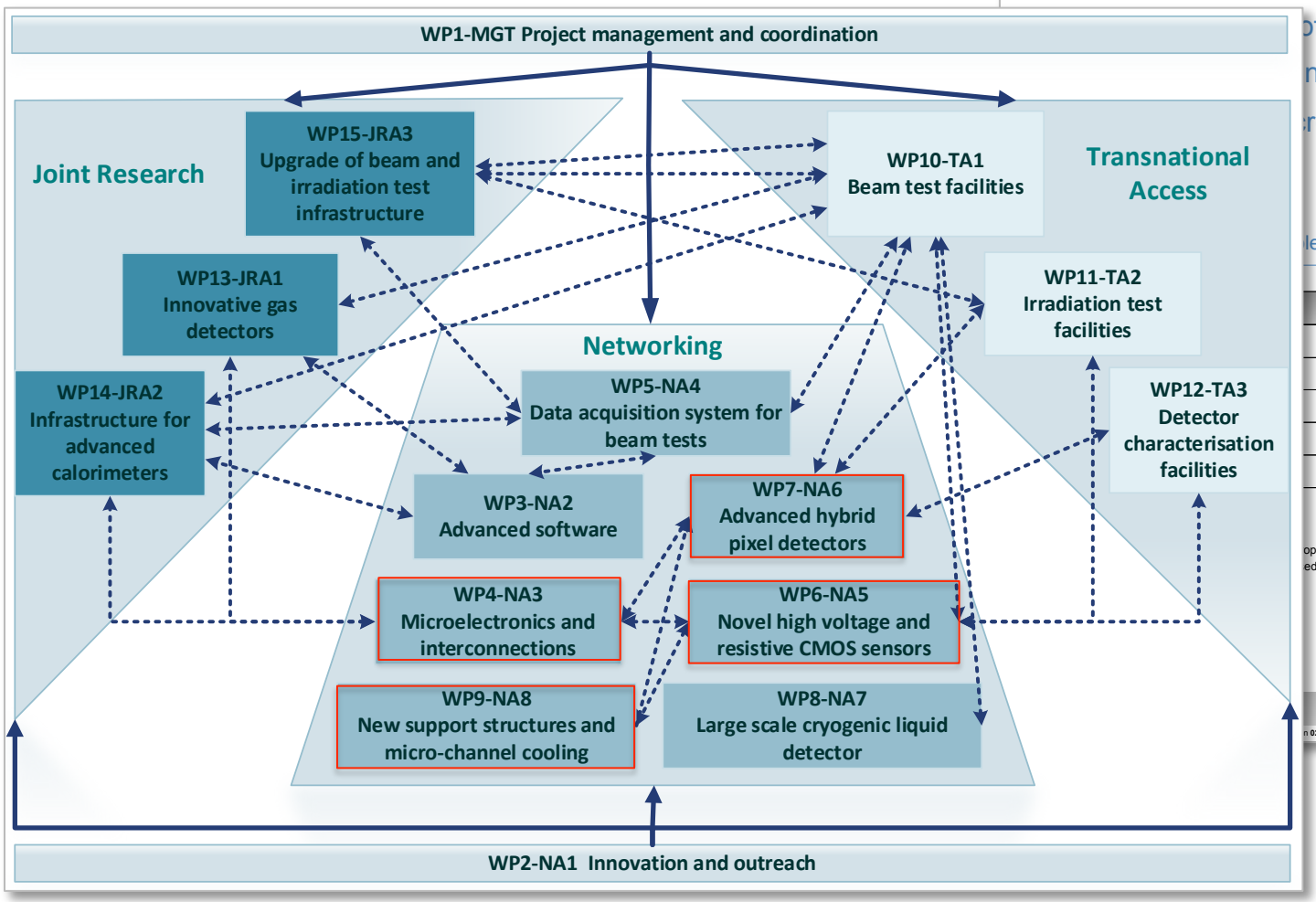
Milestones RD_FASE – Prev.2015

Descrizione	Data completamento
SENSORI PIXEL: verifica batch FBK n. 2 pixel planari su wafer DWB 6". Se positiva seguono test di moduli single ROC con pixel planari	31-07-2015
SENSORI PIXEL: qualifica della prima produzione di pixel 3D single side FBK	30-11-2015
MICROCOOLING-CMS: verifica uso CO2 evaporativo con micro-channel	31-10-2015
TRACKTRIGGER: set-up funzionante con 2 schede mezzanine con chip AM05 montate su scheda PULSAR in crate ATCA	01-10-2015
RPC: elettrodo HPL a bassa resistivita' e prototipo camera piccola dimensione	30-09-2015
RPC: prototipo camera piccola dimensione testato alla GIF++	31-12-2015
ECAL-CMS: prova di concetto di un calorimetro a readout ottico basato su fibre rad-hard per HL-LHC	31-12-2015
ECAL-CMS: studio dellaresistenza alle radiazioni di SiPM raffreddati come rivelatore candidato per readout ottico	31-12-2015
LAr-ATLAS: Moduli di potenza commerciali acquisiti e caratterizzati elettricamente	30-09-2015
LAr-ATLAS: Design della scheda ATCA terminato	31-10-2015
Tile-ATLAS: preparazione apparato sperimentale a Pisa	30-09-2015
Tile-ATLAS: definizione del protocollo di test delle schede di FE	31-12-2015
TRACKTRIGGER : inizio disegno del primo prototipo per AMchip2020, stima dimensione prima cella AM	31-12-2015

AIDA-2020

- *AIDA-2020proposal*
  - Submitted on 2 Sept. 2014
  - Approval status before end of the year





Silicon in AIDA2: Beneficiaries

WP4:

Electronics & Interconnections

AIDA 2 - WP Name - Task 3.2: 65 nm chips

Beneficiary short name*	Institute
CERN	CERN
INFN	PAVIA
INFN	TORINO
INFN	MILANO
IN2P3	CPPM
IN2P3	OMEGA/LAL/LPNHE
AGH	AGH-Krakow

AIDA 2 - WP Name - Task 3.3: SiGe chips

Beneficiary short name*	Institute
IN2P3	OMEGA
IN2P3	CPPM
CEA	SACLAY
AGH	AGH-Krakow
UHEIDELBERG	University of Heidelberg

AIDA 2 - WP Name - Task 3.4: Interconnection and TSV

Beneficiary short name*	Institute
INFN	PAVIA
INFN	GENOVA
INFN	PERUGIA
IN2P3	CPPM
IN2P3	LAL
UBONN	University of Bonn
UU	University of Uppsala
UGLAS	University of Glasgow
MPG	MPI Munich

WP6:

Advanced Hybrid Pixel Detectors

AIDA 2 - WP Name - Task 5.2: TCAD SIMULATION

Beneficiary short name*	Institute
INFN	Perugia
INFN	Trento
CERN	LCD

AIDA 2 - WP Name - Task 5.3: Process optimization

Beneficiary short name*	Institute
CSIC	CNM
FBK	

AIDA 2 - WP Name - Task 5.4: Detector validation (3D and planar sensors)

Beneficiary short name*	Institute
CERN	LCD
MPG	MPP
Manchester	
INFN	Milano
INFN	Firenze

WP7:

HV/HR-CMOS

ATLAS – Beneficiary

CMS – Beneficiary

AIDA 2 - HV-CMOS - Task 6.2: Simulation

Beneficiary short name*	Institute
CPPM	Marseille
Bonn	
STFC	RAL

AIDA 2 - HV-CMOS - Task 6.3: Sensor development

Beneficiary short name*	Institute
Bonn	
KIT	Karlsruhe
CEA	Saclay
STFC	RAL
Glasgow	
Liverpool	
CPPM	Marseille

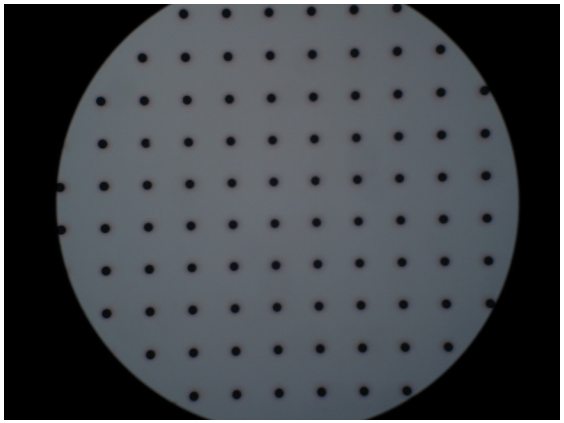
AIDA 2 - HV-CMOS - Task 6.4: Hybridisation

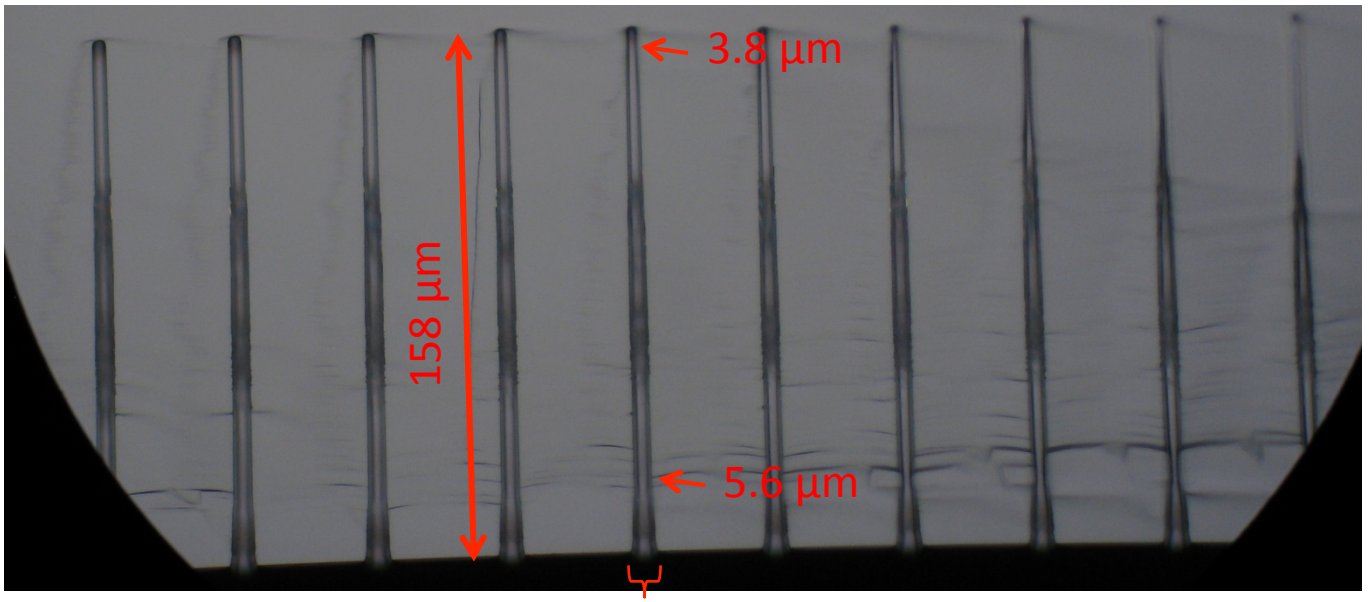
Beneficiary short name*	Institute
IFAE	Barcelona
Liverpool	
INFN	Genova

SPARE SLIDES

DRIE for Ohmic Columns

Ref.: M. Boscardin and S. Ronchin, FBK



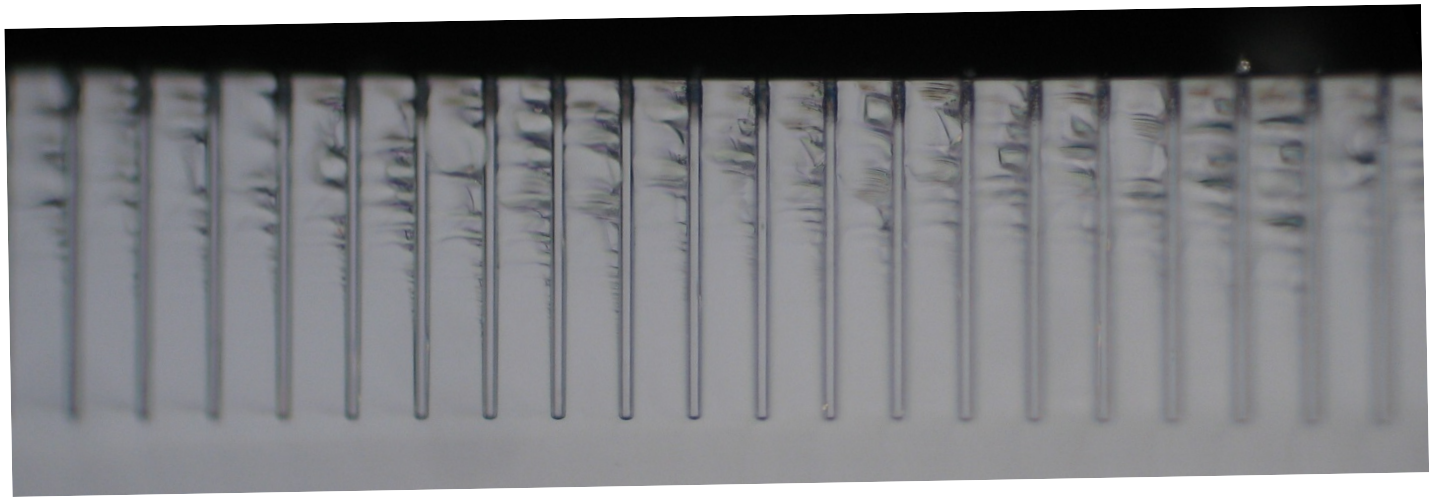


$7.6^{(*)}$ µm

(*) – the 2.6 µm larger than nominal (5 µm) can be corrected by the DRIE recipe

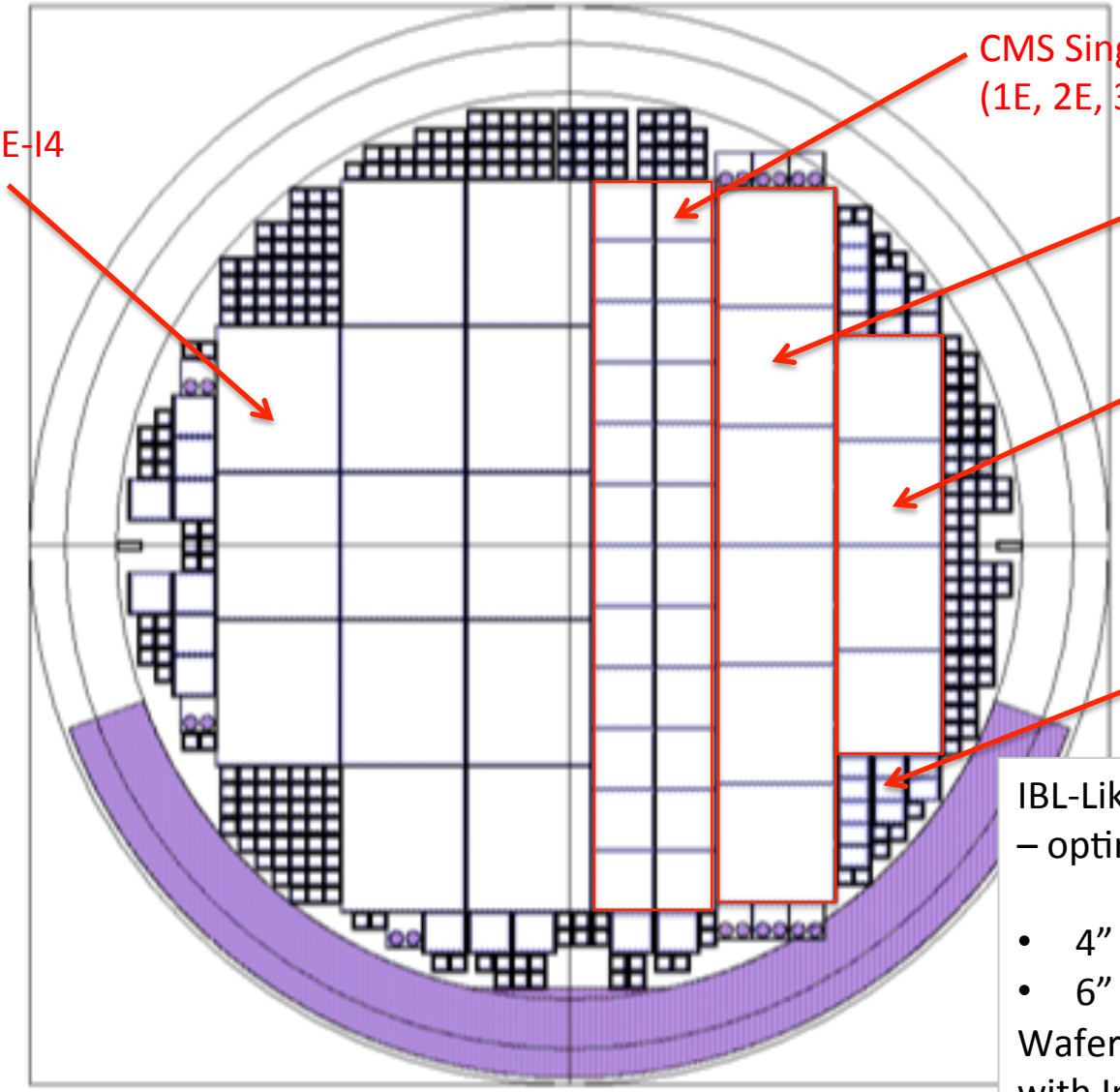
DRIE for Junction Columns

	ID#	Nominal diameter (um)	Depth (um)	Surface diameter (um)	Diameter at tip (um)
LEFT	5.1	5	99	3.5	3.2
	5.5	5	99.5	5.5	2.9
CENTER	5.5	5	100	5.5	3.5
	5.6	5	98	4.3	2.6
	5.8	5	98	5.5	2.6
	5.9	5	98	3.9	2.9
RIGHT	5.10	5	95	3.3	2.7
	5.11	5	95	3.3	2.7



Ref.: M. Boscardin and S. Ronchin, FBK

First batch on 6” wafers at FBK



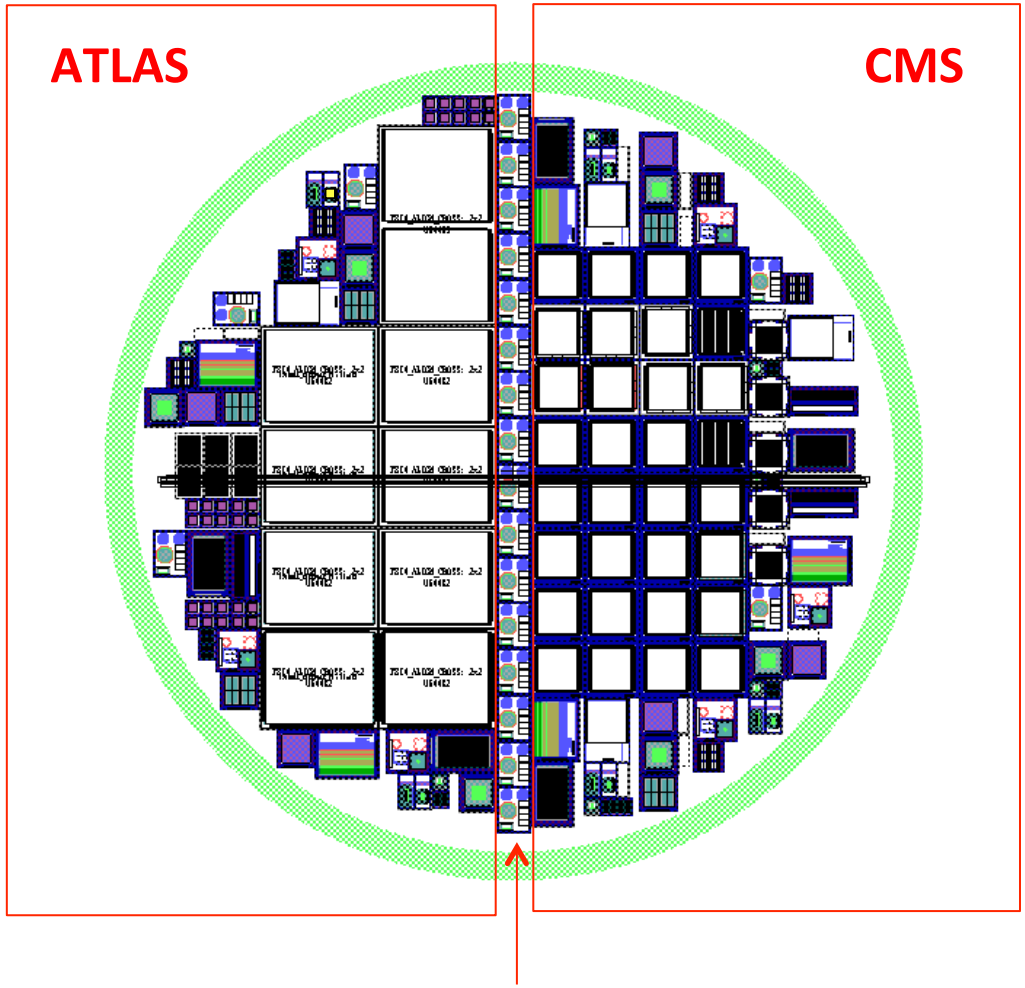
IBL-Like process – 275 µm thick wafers – optimized slim edge – increased V_{bd}.

- 4” wafers (IBL): 8 FE-I4 tiles
- 6” wafers (future): ~ 30 FE-I4 tiles

Wafers available after summer, BB with Indium at Selex – **20 k€ assigned to MI in May ’14 by CSN1**

Ref.: G.F. Dalla Betta – IFD2014, Trento, February 2014

Planar test batch



- p-type SiSi DWB wafers from ICEMOS
- 100-mm and 130-mm HR active sensor thickness
- p-spray & p-stop isolation
- Layout ready, masks ordered
- To start now, to be completed in 6-7 weeks

Test structures for Si-Si qualification