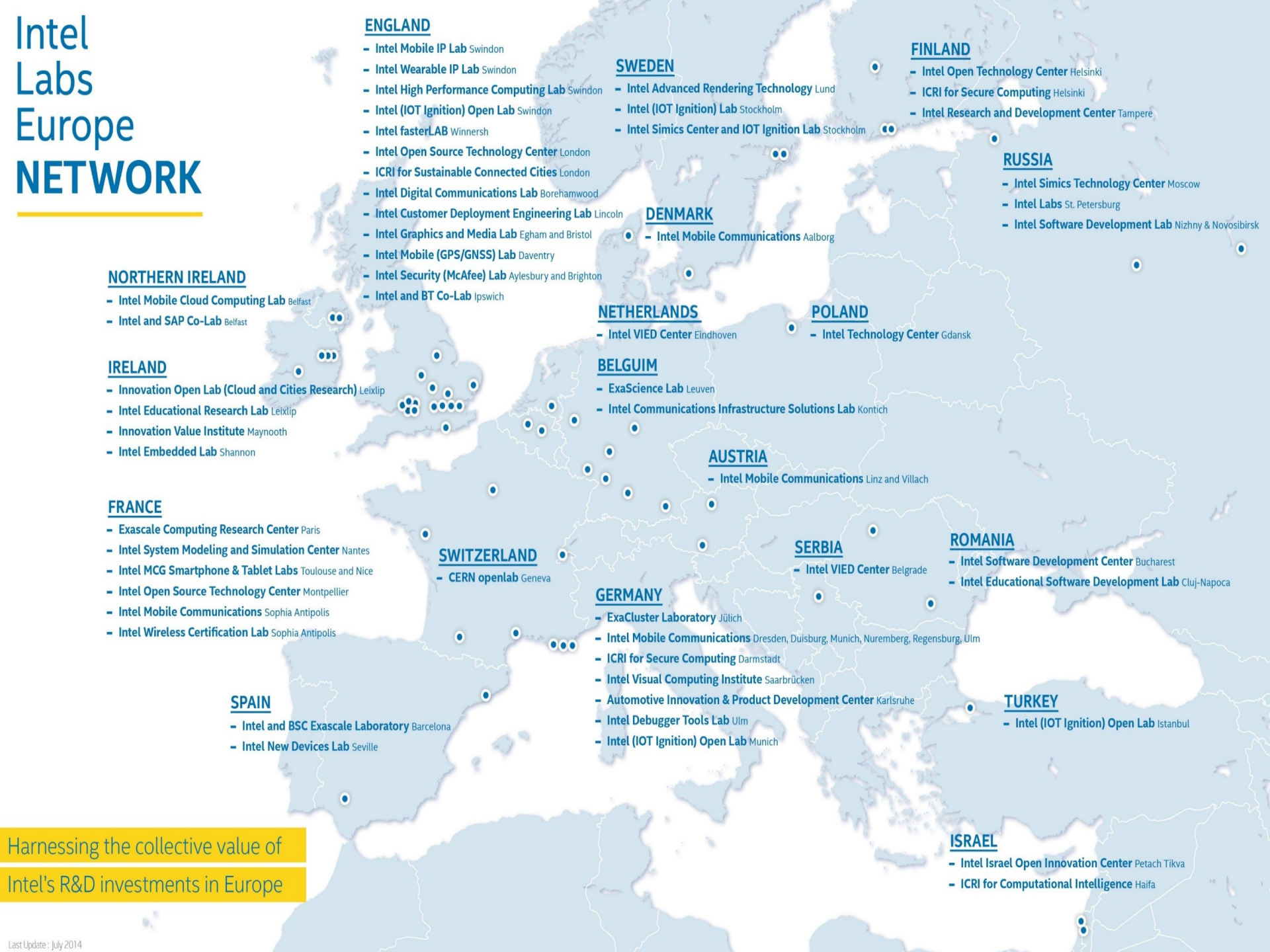

# Intel –
# A Technology Partner for HPC R&D in Europe

Karl Solchenbach

Ferrara, September 23, 2014

DCG
Data Center Group

# Intel Labs Europe NETWORK



## ENGLAND
- Intel Mobile IP Lab Swindon
- Intel Wearable IP Lab Swindon
- Intel High Performance Computing Lab Swindon
- Intel (IOT Ignition) Open Lab Swindon
- Intel fasterLAB Winnersh
- Intel Open Source Technology Center London
- ICRI for Sustainable Connected Cities London
- Intel Digital Communications Lab Borehamwood
- Intel Customer Deployment Engineering Lab Lincoln
- Intel Graphics and Media Lab Egham and Bristol
- Intel Mobile (GPS/GNSS) Lab Daventry
- Intel Security (McAfee) Lab Aylesbury and Brighton
- Intel and BT Co-Lab Ipswich

## SWEDEN
- Intel Advanced Rendering Technology Lund
- Intel (IOT Ignition) Lab Stockholm
- Intel Simics Center and IOT Ignition Lab Stockholm

## FINLAND
- Intel Open Technology Center Helsinki
- ICRI for Secure Computing Helsinki
- Intel Research and Development Center Tampere

## RUSSIA
- Intel Simics Technology Center Moscow
- Intel Labs St. Petersburg
- Intel Software Development Lab Nizhny & Novosibirsk

## DENMARK
- Intel Mobile Communications Aalborg

## NORTHERN IRELAND
- Intel Mobile Cloud Computing Lab Belfast
- Intel and SAP Co-Lab Belfast

## IRELAND
- Innovation Open Lab (Cloud and Cities Research) Leixlip
- Intel Educational Research Lab Leixlip
- Innovation Value Institute Maynooth
- Intel Embedded Lab Shannon

## NETHERLANDS
- Intel VIED Center Eindhoven

## POLAND
- Intel Technology Center Gdansk

## BELGUIM
- ExaScience Lab Leuven
- Intel Communications Infrastructure Solutions Lab Kontich

## AUSTRIA
- Intel Mobile Communications Linz and Villach

## FRANCE
- Exascale Computing Research Center Paris
- Intel System Modeling and Simulation Center Nantes
- Intel MCG Smartphone & Tablet Labs Toulouse and Nice
- Intel Open Source Technology Center Montpellier
- Intel Mobile Communications Sophia Antipolis
- Intel Wireless Certification Lab Sophia Antipolis

## SWITZERLAND
- CERN openlab Geneva

## SERBIA
- Intel VIED Center Belgrade

## ROMANIA
- Intel Software Development Center Bucharest
- Intel Educational Software Development Lab Cluj-Napoca

## GERMANY
- ExaCluster Laboratory Jülich
- Intel Mobile Communications Dresden, Duisburg, Munich, Nuremberg, Regensburg, Ulm
- ICRI for Secure Computing Darmstadt
- Intel Visual Computing Institute Saarbrücken
- Automotive Innovation & Product Development Center Karlsruhe
- Intel Debugger Tools Lab Ulm
- Intel (IOT Ignition) Open Lab Munich

## SPAIN
- Intel and BSC Exascale Laboratory Barcelona
- Intel New Devices Lab Seville

## TURKEY
- Intel (IOT Ignition) Open Lab Istanbul

## ISRAEL
- Intel Israel Open Innovation Center Petach Tikva
- ICRI for Computational Intelligence Haifa

Harnessing the collective value of Intel's R&D investments in Europe

Last Update : July 2014

# Intel HPC R&D activities in Europe

## Software & Solutions Group

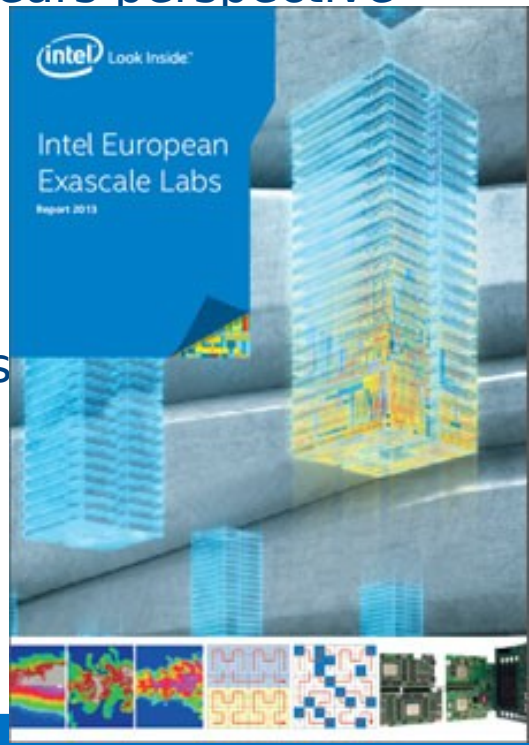
- Optimize existing codes on existing Intel HW & SW
- Support OEMs in benchmarks

## Intel Parallel Competence Centers (IPCC)

- Optimize existing community codes for Xeon Phi
- Contracts to universities / research labs with 1-2 years perspective

## Intel European Exascale Labs

- Focus on “future” applications
- Partner with leading HPC apps developers
- Feedback to Intel architects
- 5-7 years perspective, part of „pathfinding“ proces
  *(Research  Pathfinding  Development)*
- Engage in H2020 (ETP4HPC, FET-HPC, CoE, …)




ExaCluster Lab, Jülich
JÜLICH FORSCHUNGSZENTRUM
intel
PARTEC CLUSTER COMPETENCE CENTER
Leuven
LEUVEN
UNIVERSITEIT GENT
Universiteit Antwerpen
Universiteit Hasselt
intel
imec
Research Lab, Paris
GENCI
intel
cea
UNIVERSITE DE VERSAILLES SAINT-QUENTIN-EN-YVELINES
Intel and BSC Exascale Lab, Barcelona
BSC Barcelona Supercomputing Center
Centro Nacional de Supercomputación
intel
New: Intel-CERN Lab on Throughput Computing
CERN
intel
Liverpool
Manchester
KINGDOM
Birmingham
Cardiff
London
Amsterdam
NETH.
Rotterdam
Hamburg
Bremen
Berlin
Poznań
Oder
Elbe
Essen
Leipzig
Cologne
Brussels
Lille
Bonn
GERMANY
English Channel
Guernsey (U.K.)
Jersey (U.K.)
Frankfurt
Prague
CZECH REPUBLIC
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LUX.
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SLOVENIA
Milan
Venice
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Genoa
CROATIA
SAN MARINO
Toulouse
MONACO
Bilbao
Andorra la Vella
Marseille
Ligurian Sea
Florence
ANDORRA
Zaragoza
Corsica
ITALY
Adriatic Sea
Rome
VATICAN CITY
Barcelona
Naples
Balearic

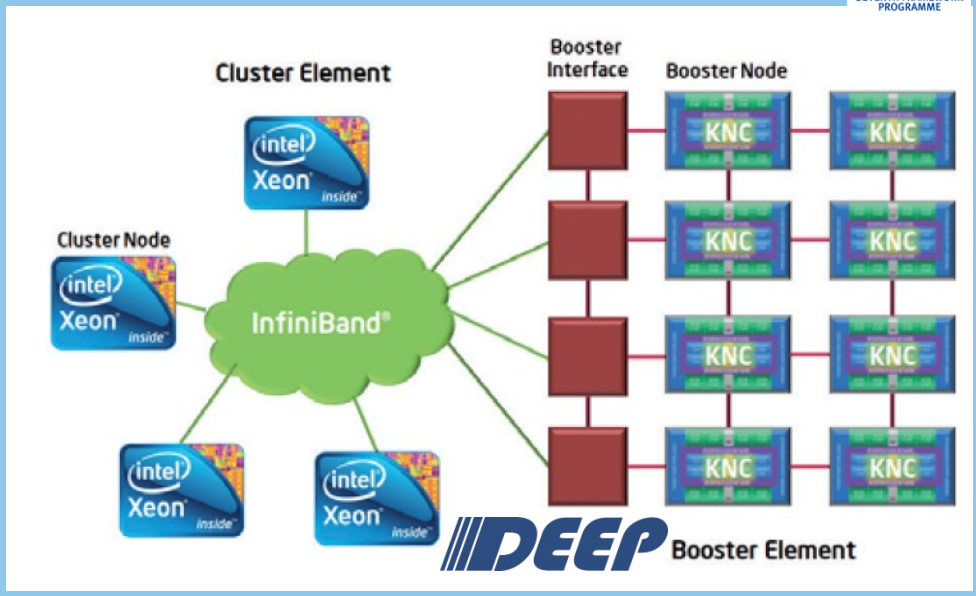
# Germany: Juelich ExaCluster Laboratory

SW Scalability and Resilience

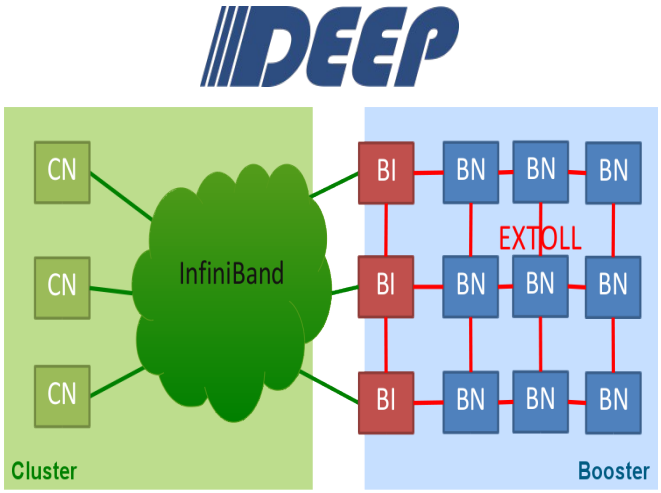
Exascale Cluster Architecture

Exascale Simulation and Tools

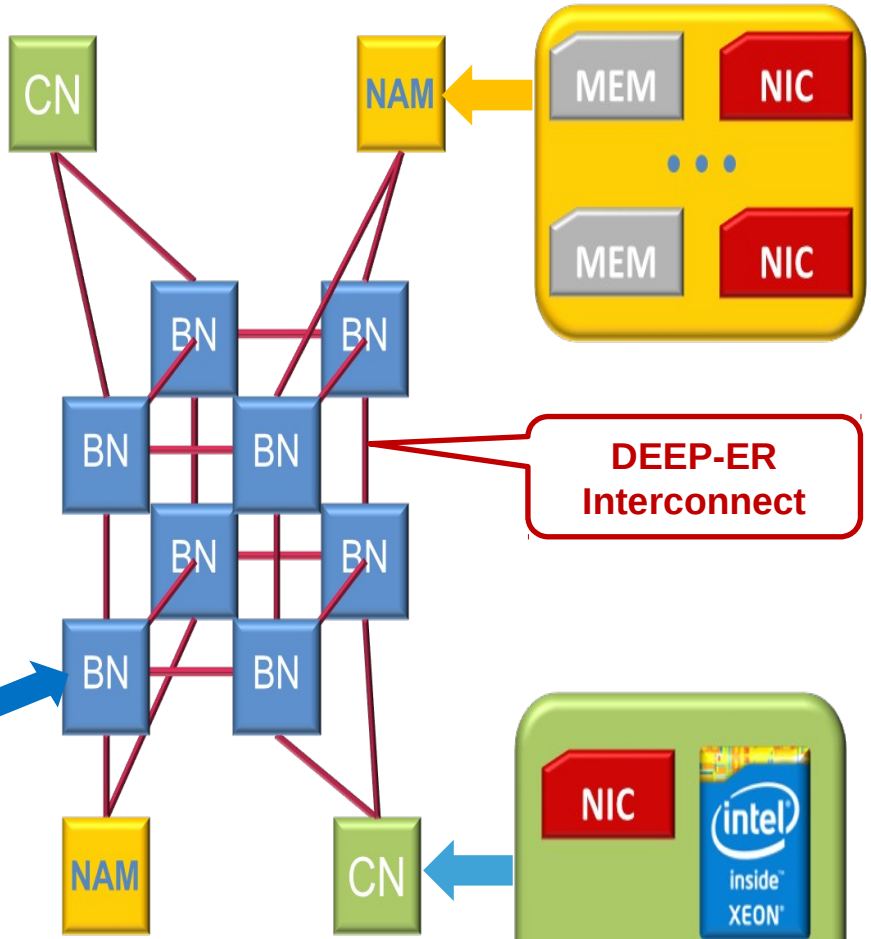
## The DEEP Architecture



# Architecture Evolution



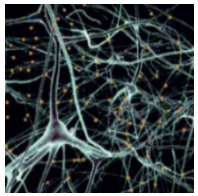


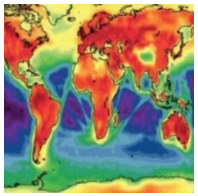


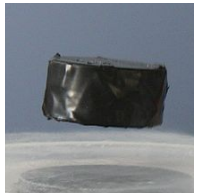
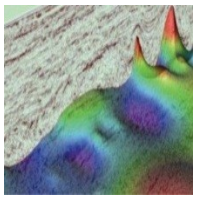
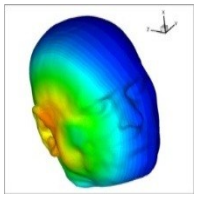

**Legend**:

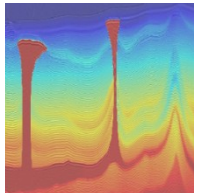
| | |
|---|---|
| CN: | Cluster Node |
| BN: | Booster Node |
| BI: | Booster Interface |
| KNL: | Intel® Xeon PhiTM |
| NAM: | Network Attached Memory |
| NVM: | Non Volatile Memory |

# Application-Driven Approach





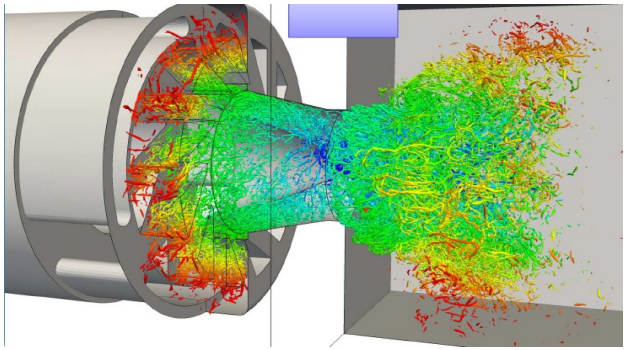

**DEEP & DEEP-ER applications:**

- Brain simulation (EPFL)
- Space weather simulation (KULeuven)
- Climate simulation (CYI)
- Computational fluid engineering (CERFACS)
- High temperature superconductivity (CINECA)
- Seismic imaging (CGGVS)
- Human exposure to electromagnetic fields (INRIA)
- Geoscience (BADW-LRZ)
- Radio astronomy (Astron)
- Oil exploration (BSC)
- Lattice QCD (UREG)

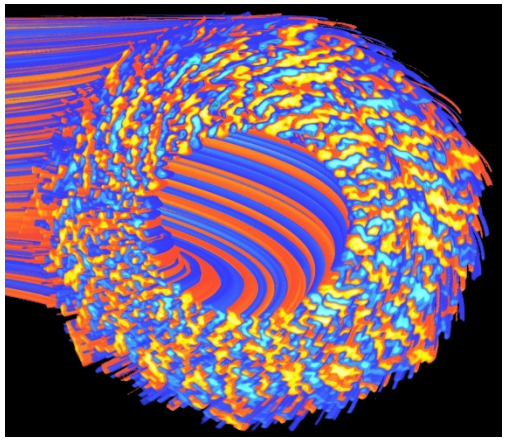
**Objectives:**

- Co-design & evaluation of DEEP architecture & programmability
- Analysis of the I/O and resiliency requirements of HPC codes

# Paris Exascale Lab – Adressing SW Challenges



YALES2



Gysela5

## Scaling

- How do codes scale from peta- to exa-scale?
- With MPI + X?

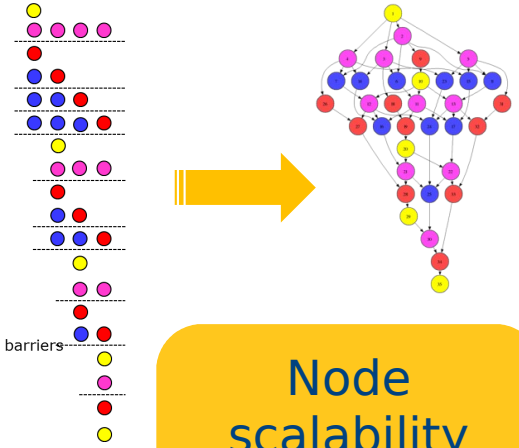
## New memory architecture

- cache – DRAM – disk  cache – high BW local memory – NVM

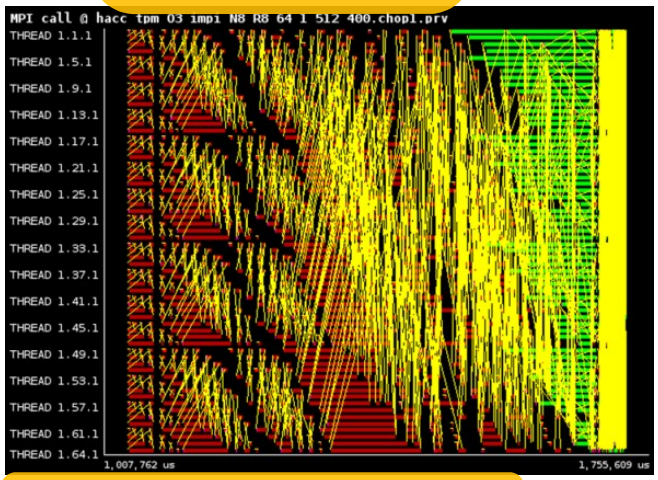
## Energy

- How will applications run in a power-bound regime?
- Does it make sense to overlap of calculation and comms?

# Barcelona (BSC) Exascale Lab

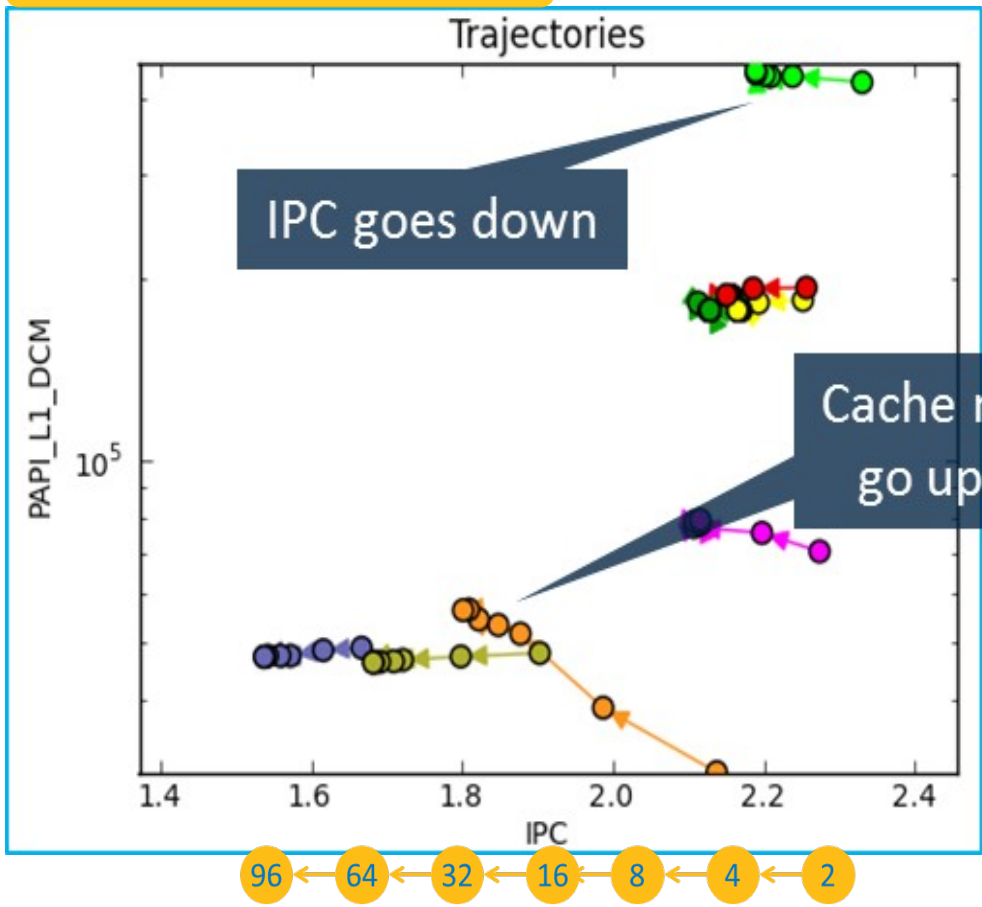



Node scalability improvements

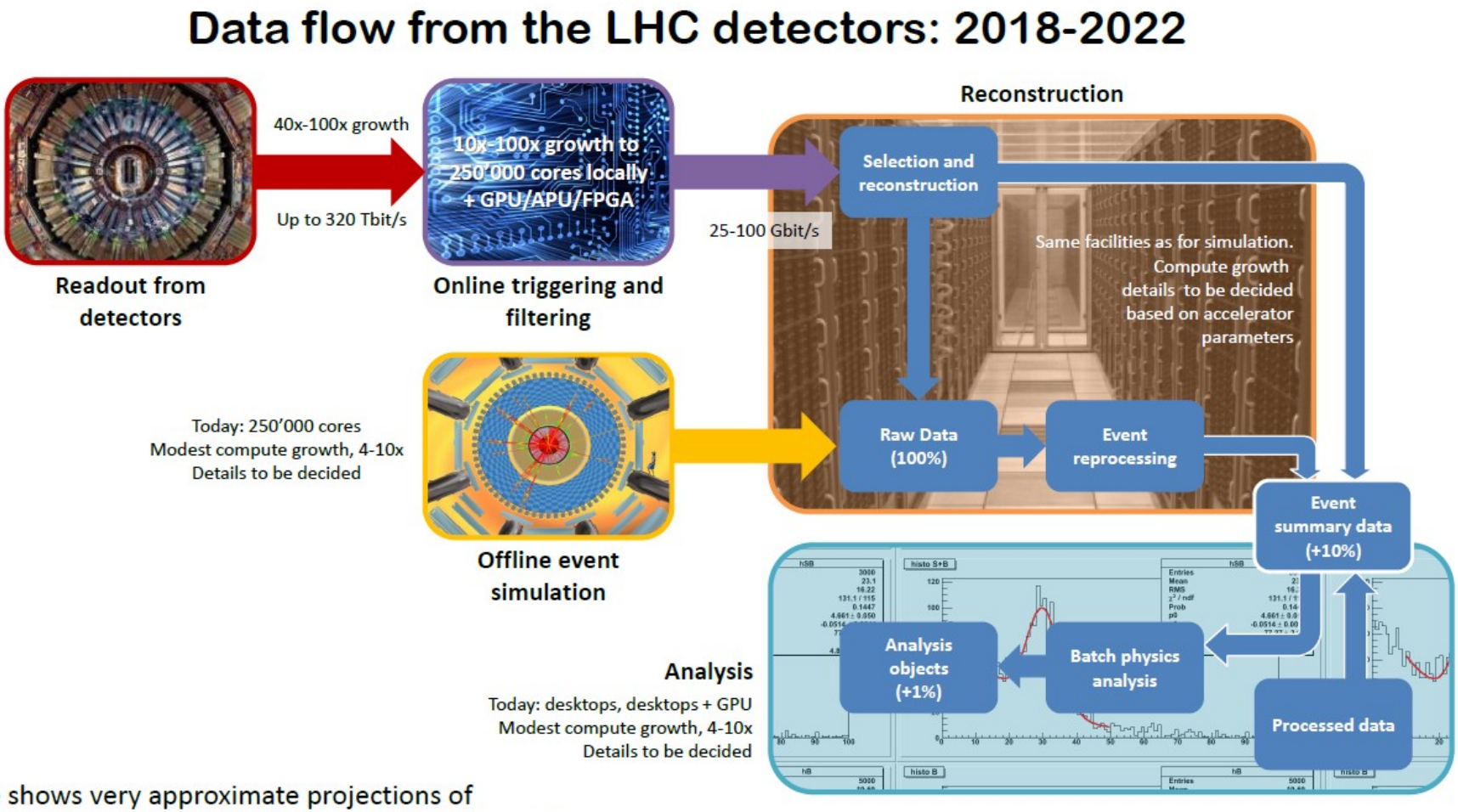



Workload analysis

Code phase analysis



# LHC Data Flow




This slide shows very approximate projections of the LHC data flow around 2018 (after Long Shutdown 2)

# CoE: Intel‘s potential contribution and role

## Can we establish a „co-design“ process?

- Can the community agree on a codes / mini-apps / kernels / libraries ...
- Analyze requirements and present to architects
- Intel to provide fast simulator to the CoE community?

## How to collaborate?

- Big issue: confidentiality vsIP  rules of H2020/CoE?
  - Intel needs to understand IP rules early
- Keep links to different vendors separate
- Vendors part of the consortium (i.e. signing the CA)?