TOFPET perfomances: latest results

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INFN & LIP

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1. Context
   - EndoTOFPET-US FP7
   - Requirements and specifications
2. Design of the TOFPET chip
   - Chip and channel Architecture
   - Front-end
   - Time-to-Digital Converter
   - Chip integration
3. TOFPET characterization
   - Test setup
   - Electrical Characterization Results
   - Tests with MPPCs
   - System-ready hardware
4. Outlook

Outline

EndoTOFPET-US FP7: Endoscopic PET and Ultrasound

Combined TOF-PET (200 ps time resolution), ultrasound imaging and endoscopic biopsy

PET components:
- dSiPM/crystal endoscopic probe
- aSiPM/crystal external plate

ENDO TOFPET US
Endoscopic TOFPET & Ultrasound

Target

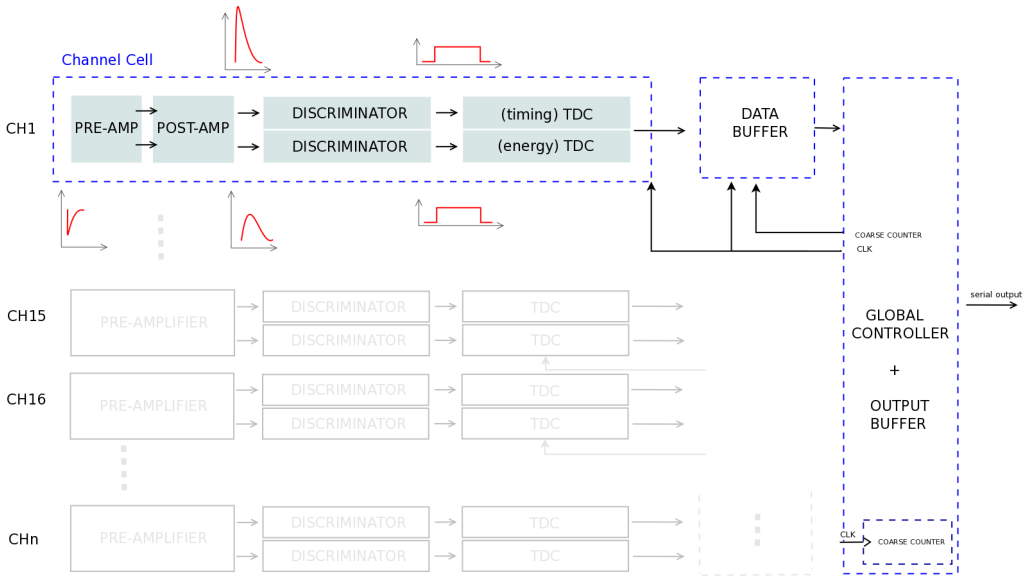
- **Design of a low power SiPM readout ASIC for Time of Flight applications**
- integrates signal conditioning and discrimination circuitry and high-performance TDCs for each of 64 independent channels
- targets 25 ps r.m.s. intrinsic resolution and features fully digital output
- TOFPET ASIC developed in the framework of the **FP7 project EndoTOFPET-US**
  - PET time-of-flight detector plate (4000 channels)
  - MPPC (16-channel arrays, 3x3 mm^2) and LYSO crystals
  - Coincidence time resolution (CTR) 200 ps (FWHM)

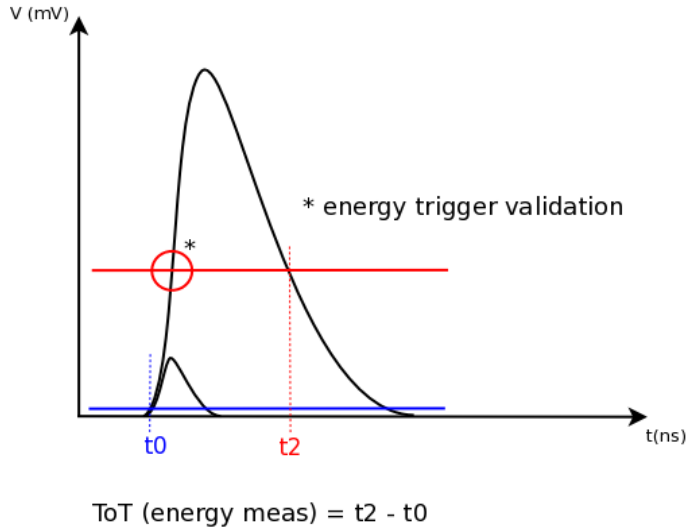
Features of an ASIC for SiPM readout in PET applications

Parameter	Value
Number of channels	64
Clock frequency	$80 - 160$ MHz
Dynamic range of input charge	**300 pC**
SNR ($Q_{in} = 100$ fC)	$>$ 20-25 dB
Amplifier noise (in total jitter)	$<$ 25 ps (FWHM)
TDC time binning	**50 ps**
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. channel hit rate	100 kHz
Max. output data rate	320 Mb/s (640 w/ DDR)
Channel masking	programmable
SiPM fine gain adjustment	**500 mV (5 bits)**
SiPM	up to 320pF term. cap., 2MHz DCR
Calibration BIST	internal gen. pulse, 6-bit prog. amplitude
Power	**$<$ 10 mW per channel**

Outline

Overview of the channel architecture

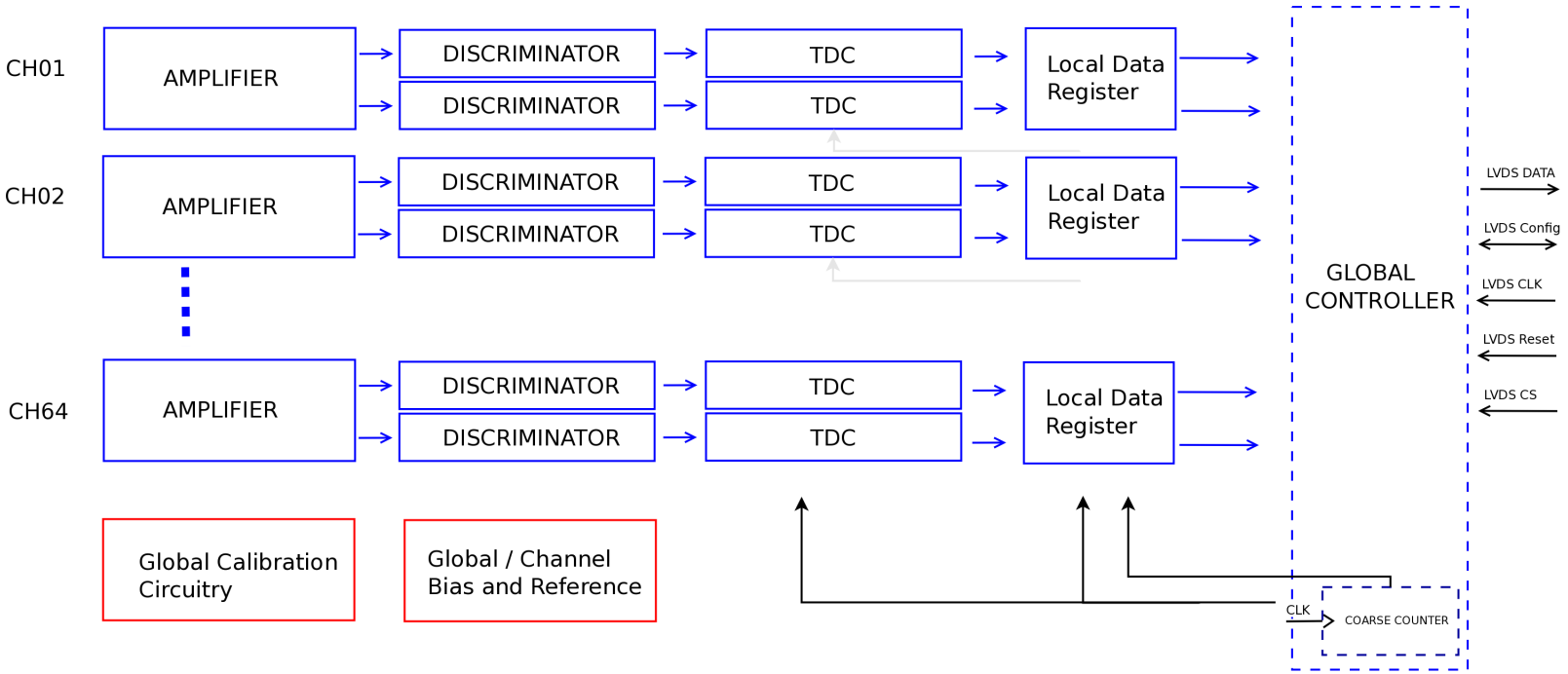




- Time and charge measurements with independent TDCs
- Trigger level **0.5 p.e.** with SNR = 25 dB
- Target intrinsic resolution 25 ps r.m.s.
- Charge measured with Time-over-threshold
- Low-power 8-11 mW p/channel
- **Single-Ended Input**

Overview of the chip architecture

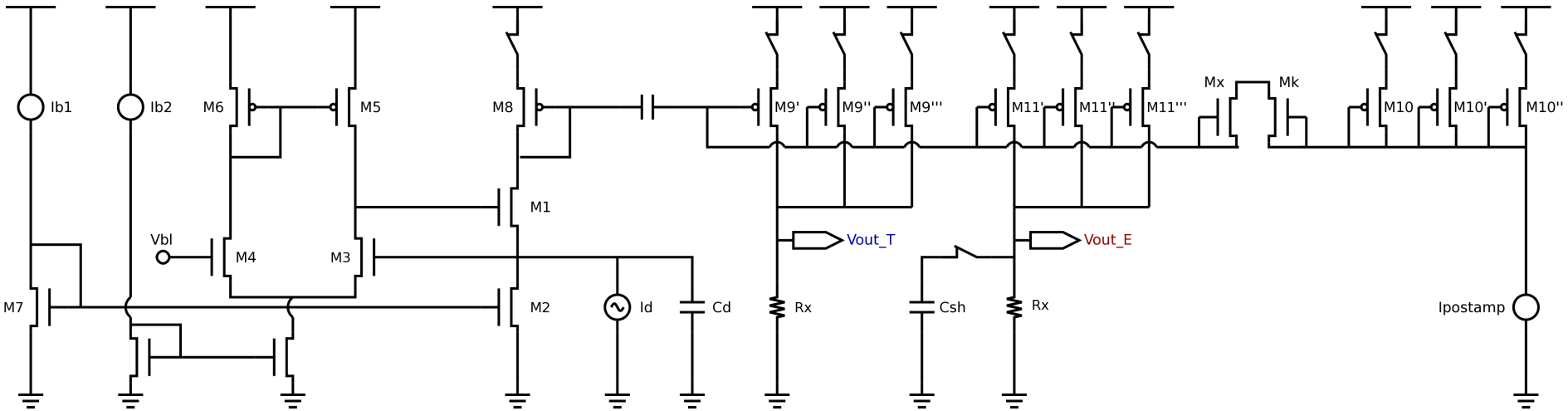
The TOFPET ASIC consists of a 64-channel analogue block, calibration circuitry, Golden-references and Bias generators and a global controller.



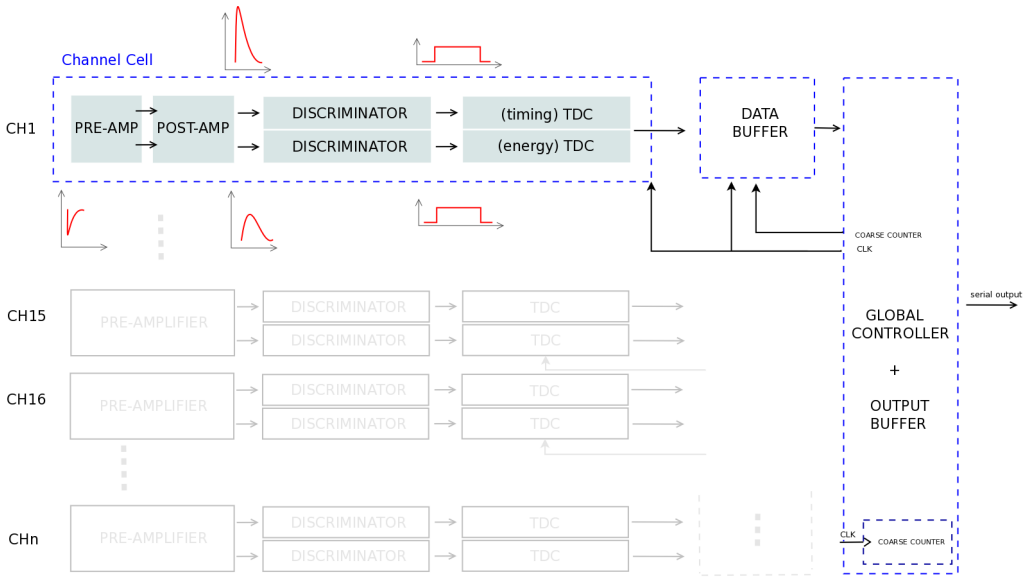
- LVDS 10 MHz SPI configuration link and dark count measure
- LVDS up to 640 Mbps data output interface; 8B/10B encoding
- On-chip DACs and reference generators

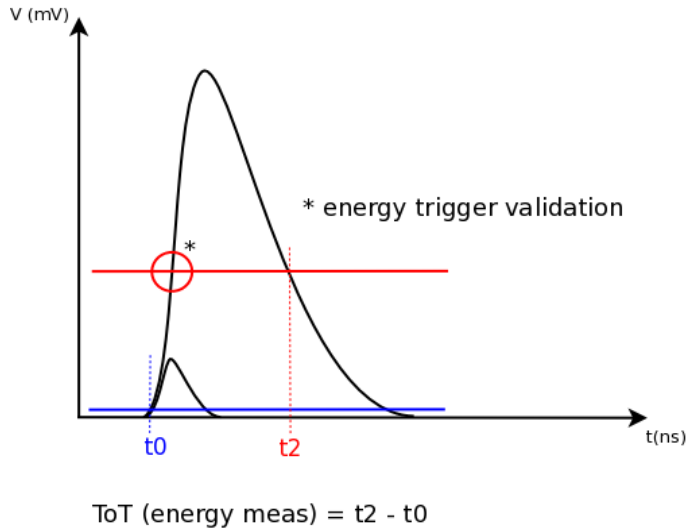
Front-end for SiPM readout

- Low-Zin pre-amplifier, 2 independent TIA branches for Timing and Energy triggers
- coarse gain adjustment, optional shaping function for Vout_E
- Selectable delay line for dark count filtering
- Representation for cathode readout, extra circuit for anode type SiPM



Inputs for TDC



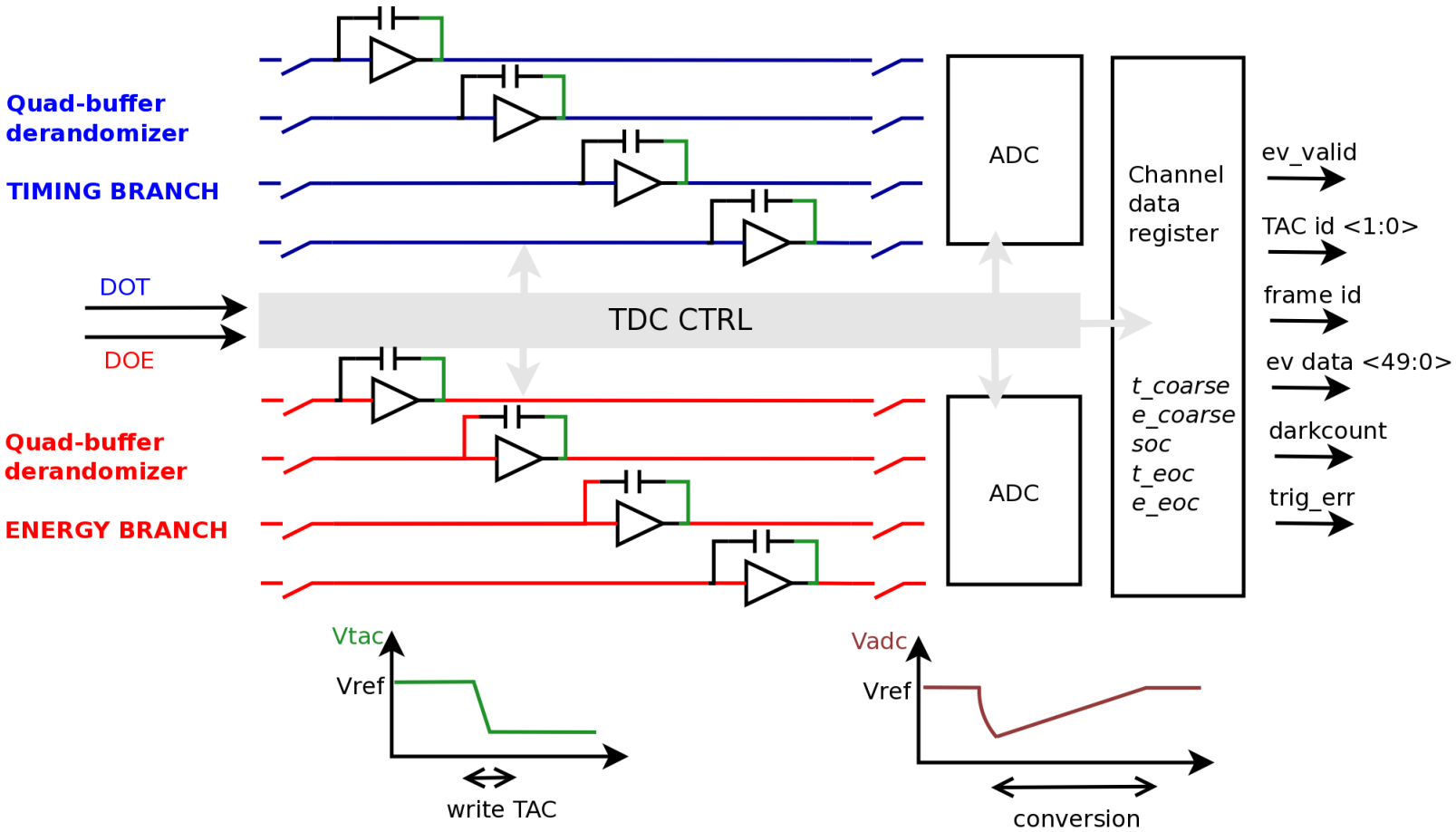


- t0: 50 ps time stamp from rising edge of DOT
- t2 : 50 ps time stamp from falling edge of DOE

Time-to-Digital Converter

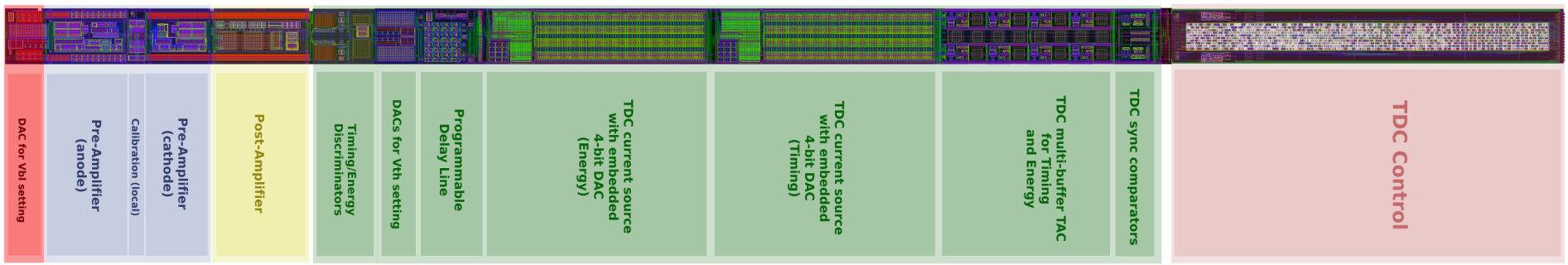
Analogue TDC with 25ps/50ps time binning - based on Analogue Interpolators

- TDC Control: switching, hit validation, buffer allocation, data reg.
- Time stamp: 10-bit master clock count + Fine time measurement

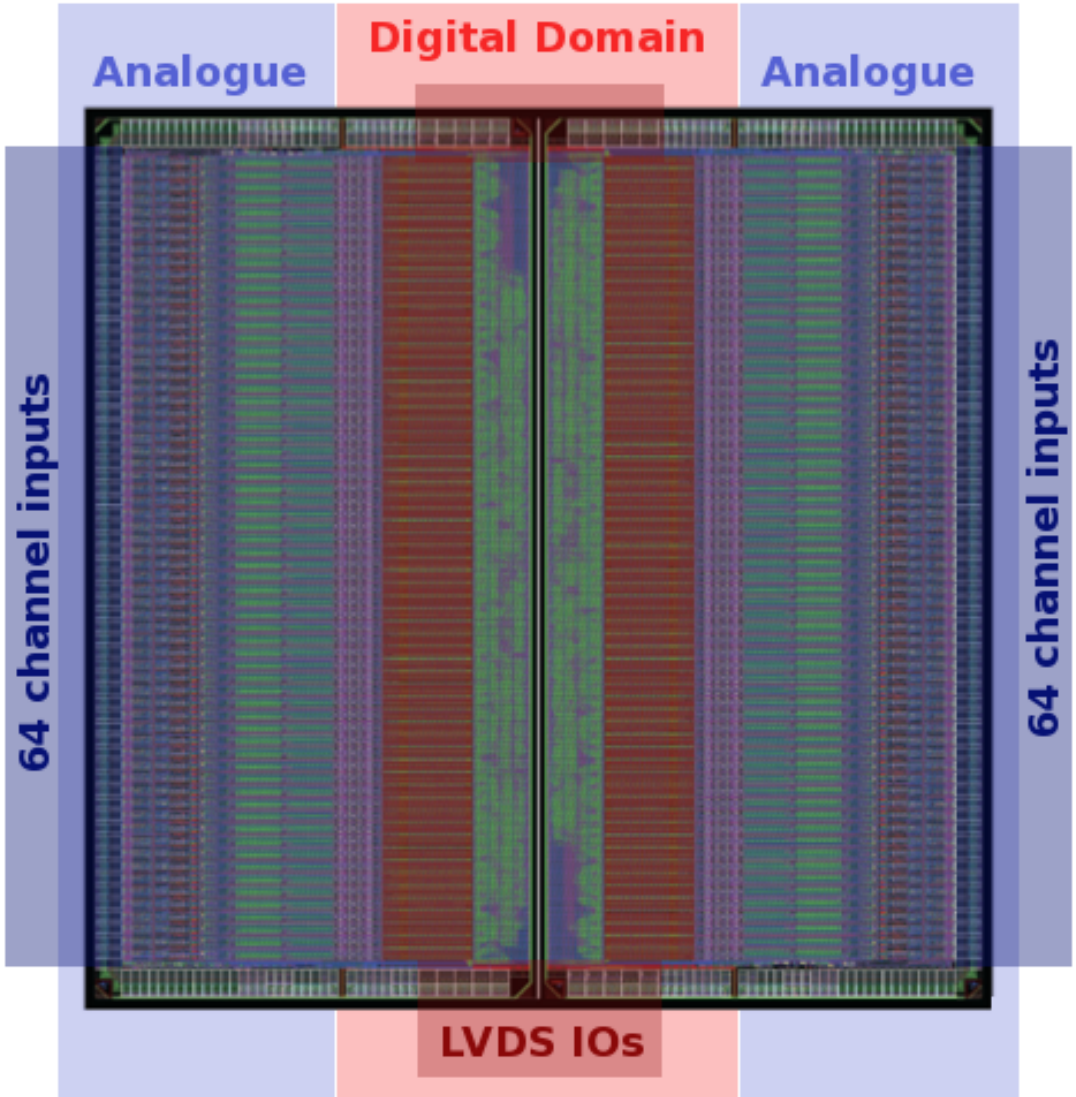


Channel Layout

- 64 channels, form factor 0.1 x 2.5 mm
- Each channel comprises:
  - front end 2-polarities
  - local calibration circuitry
  - discriminators for timing, energy
  - DACs for input DC setting, thresholds
  - delay line for DCR filtering
  - TDC-analogue: current sources, TACs, wilkinson ADC and latched comparator
  - TDC-digital: sequence control, buffer assignment, 50-bit register, interface with back-end

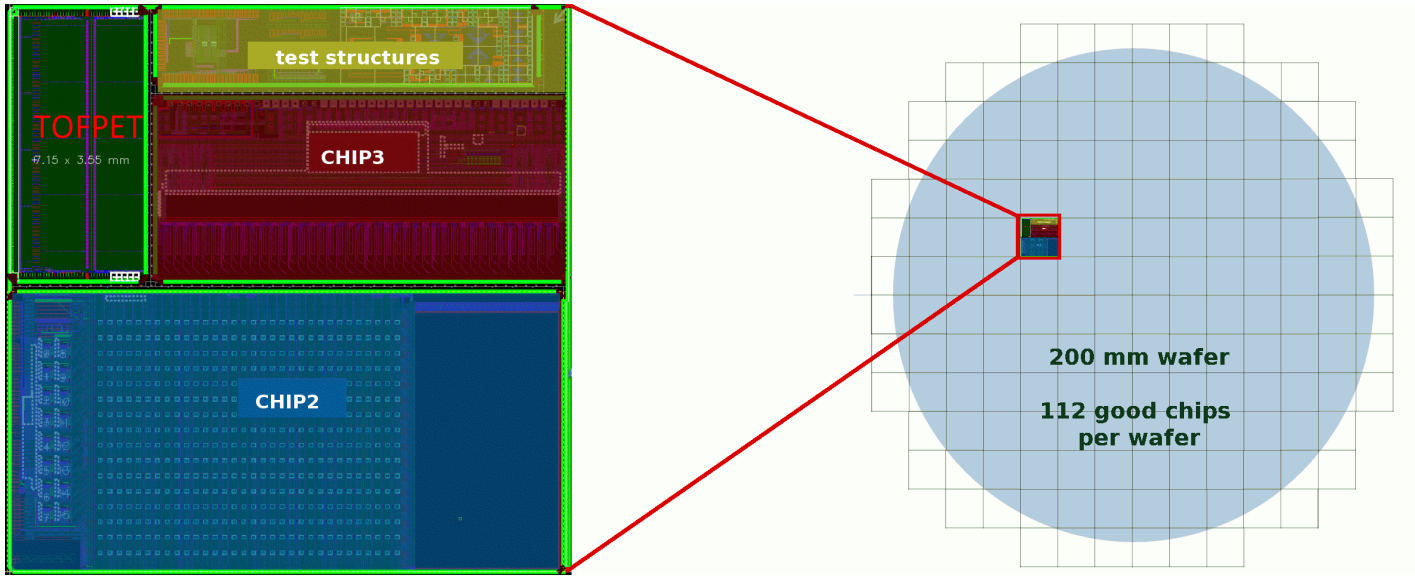


128-channel System-in-a-Package



Outline

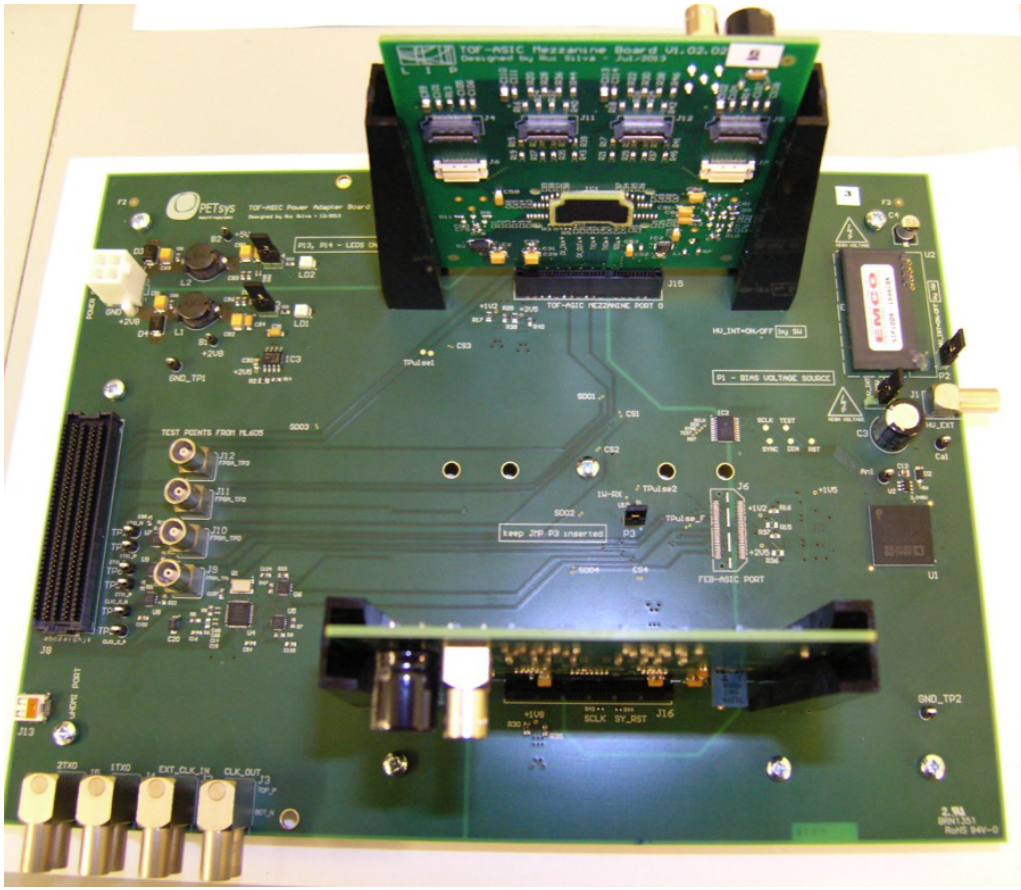
Chip production

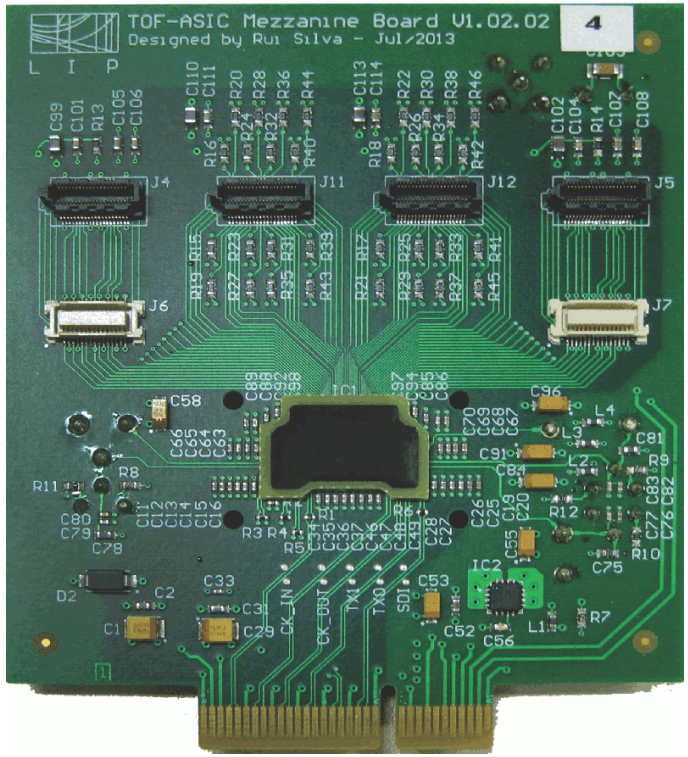


- 25 mm^2 IBM 0.13μm CMOS/RF
- submitted June 2012 within a CERN dedicated run
- 112 chips per wafer
- available as naked dice
- available as 128-channel SiP BGA-packaged

TOFPET ASIC test setup

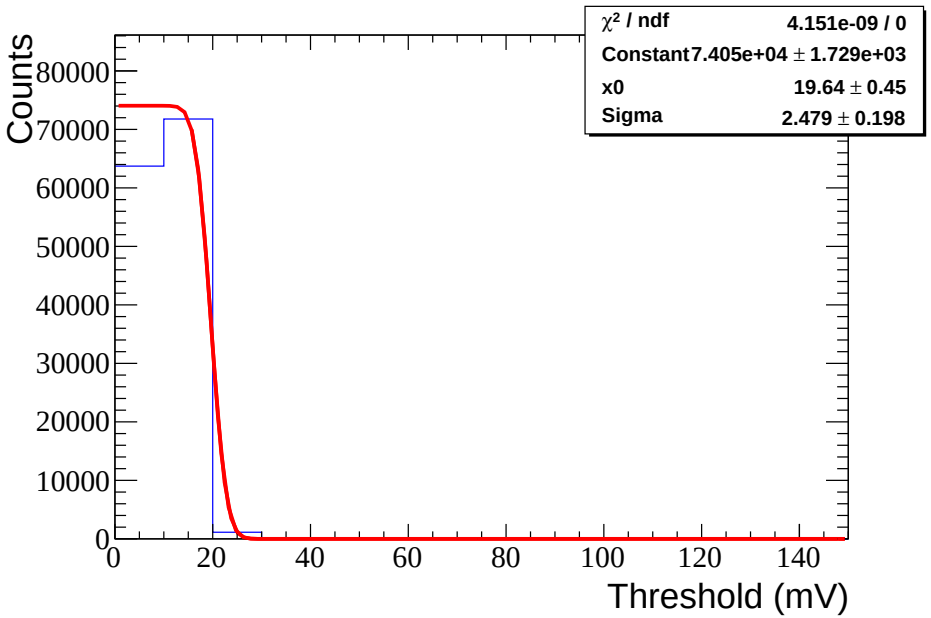
- Two mezzanines and power adapter board
- Mezzanines with crystal matrices are face-to-face

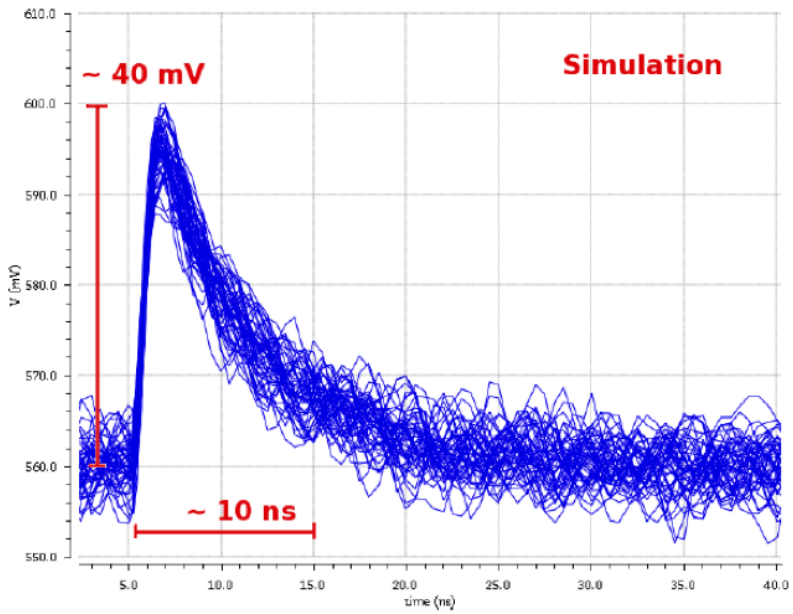




Front-end noise estimation

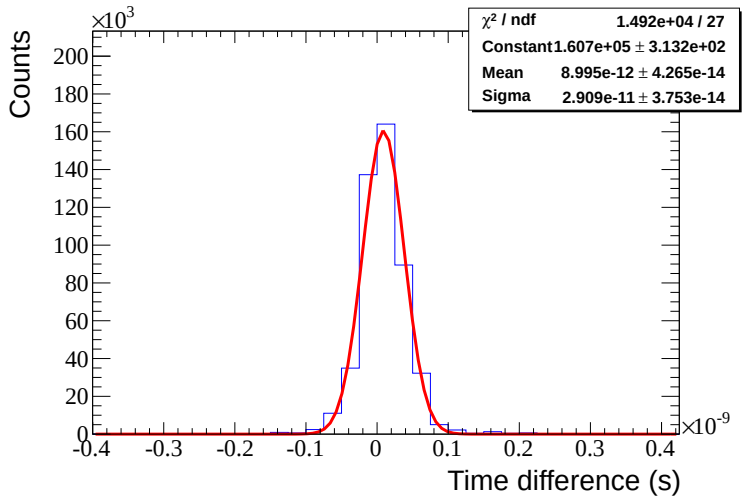
- number of events as function of threshold (both thresholds set to the same value)
- fit to a cumulative probability distribution function
- **2.5 mV r.m.s.** (agrees to simulation results)





TDC Quantization Error

- **Step 1**: TDC calibrated with a test pulse sweep across 50 ns (500 ps step, 10000 pulses p/ step)
- **Step 2**: Correct for TDC non-linearity
- **Step 3**: Trigger simultaneously two channels and measure time difference (removes common mode test pulse jitter)

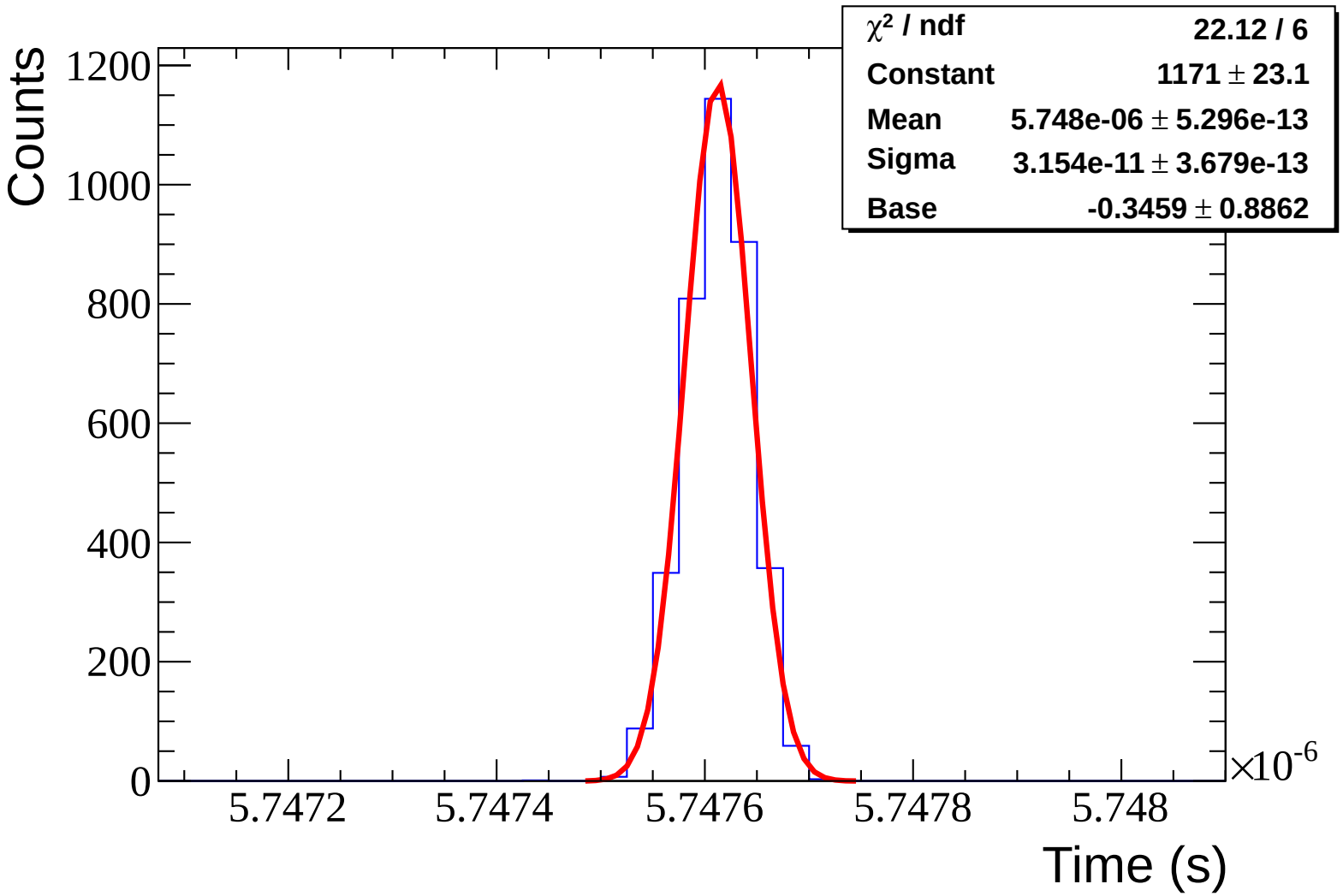


- Distribution with 29 ps r.m.s.,
  corresponds to a **per channel error of 21 ps r.m.s.**

Multi-Photon Time Resolution

- Laser: no optical attenuator ($N_{ph} > 1000$)

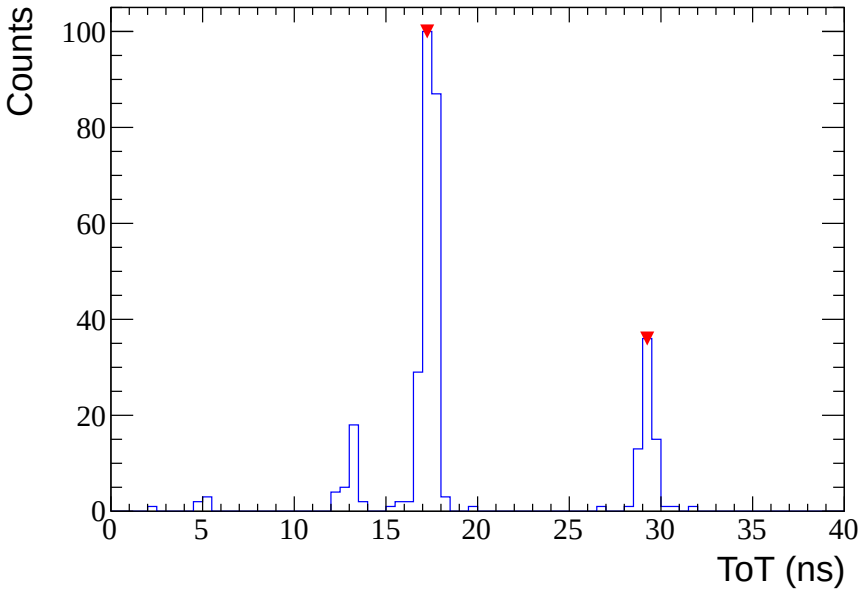
↪ 32 ps r.m.s., includes jitter from the laser and the test pulse

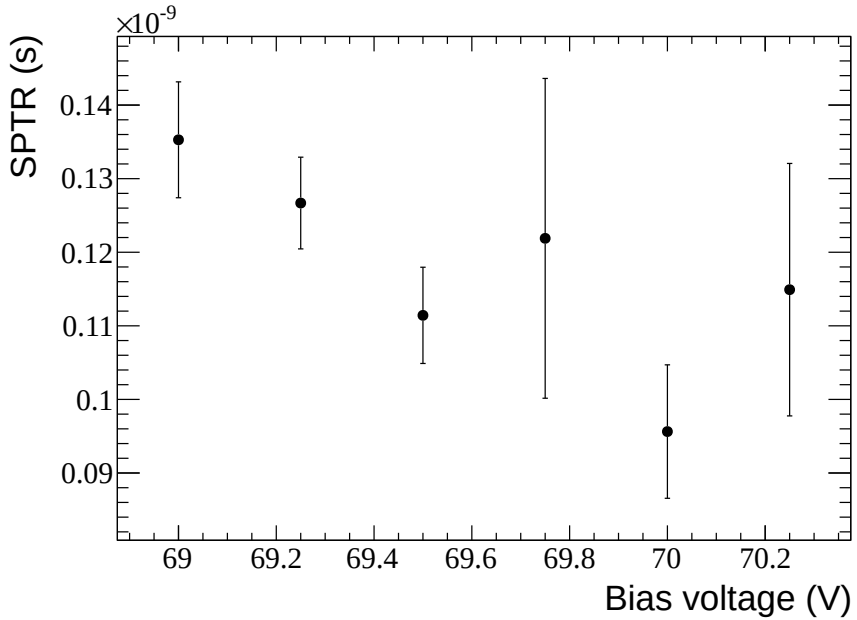


Single-Photon Time Resolution

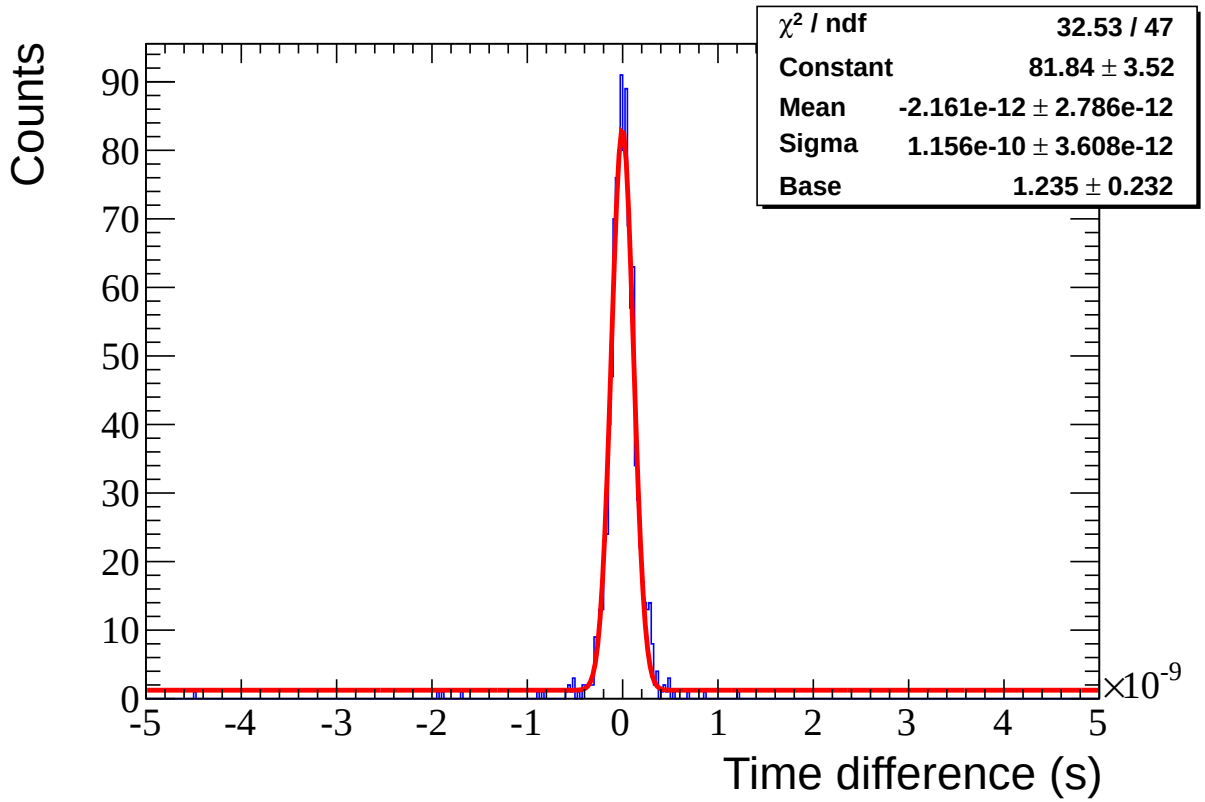
- Laser: w/ optical attenuator ($N_{ph} = 1$)
- both thresholds set to 0.5 p.e. level
- laser triggered at 80 kHz rate, known time in respect to the start-of-frame
- ToT distribution of events within 1 ns of the expected laser pulse time show the 1 photon and 2 photon peaks

↪ 110 ps r.m.s., after optimization of the HV





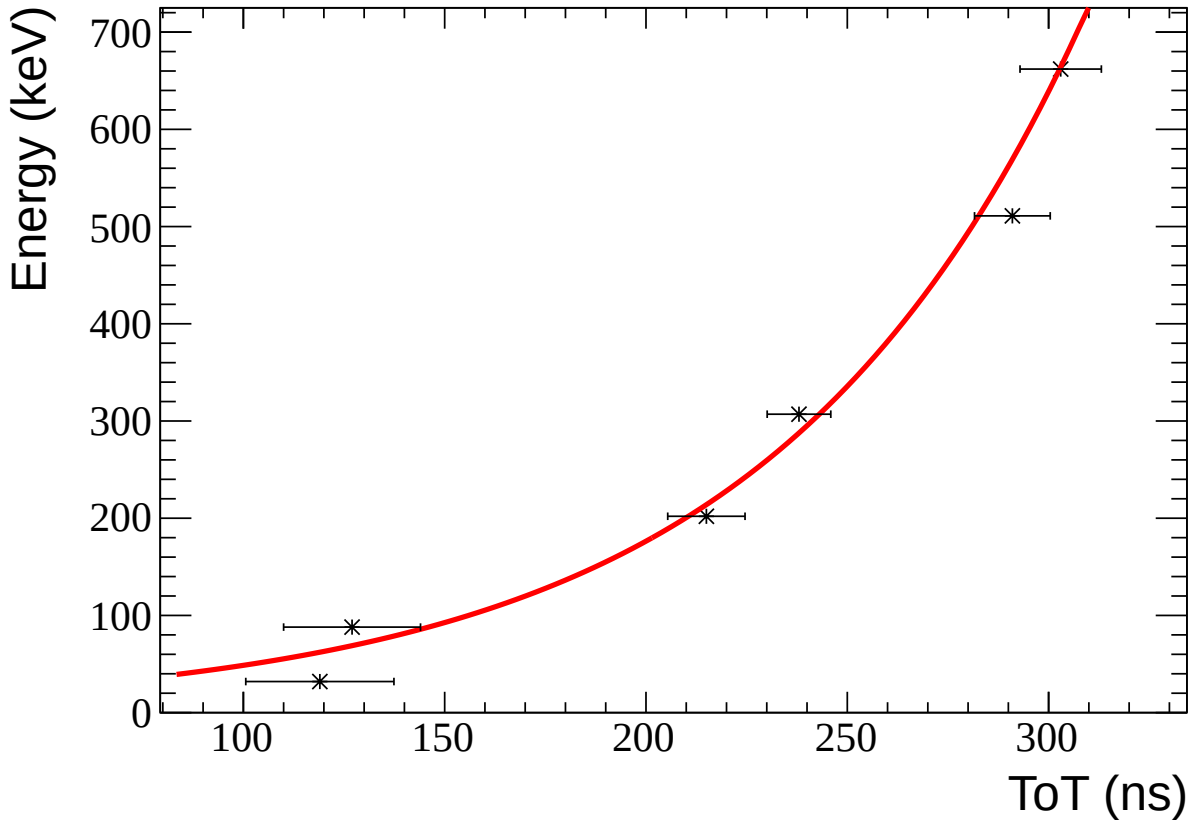
Coincidence Time Resolution - **preliminary**



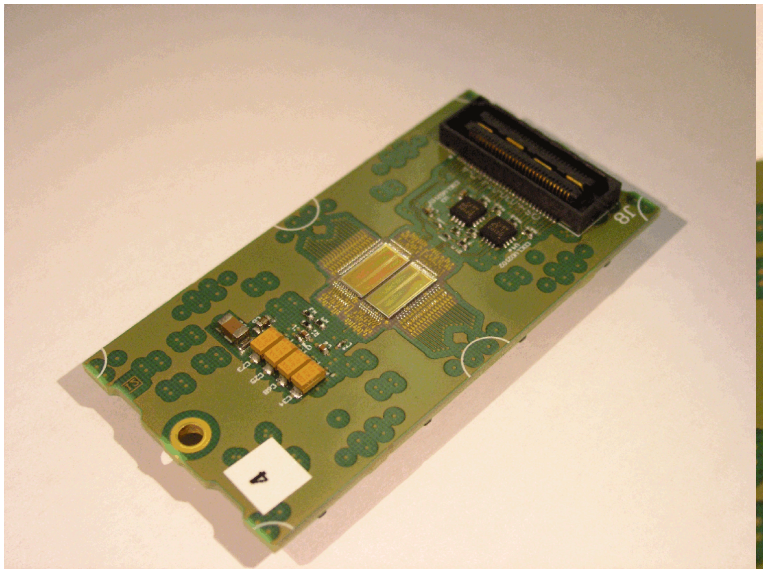
- MPPC discrete TSV 4x4 arrays (3 x 3 mm^2 pixels)
- Single Crystal on each array (3 x 3 x 15 mm^3)
- **CTR = 270 ps FWHM**
- Result does not depend on the threshold setting other channels

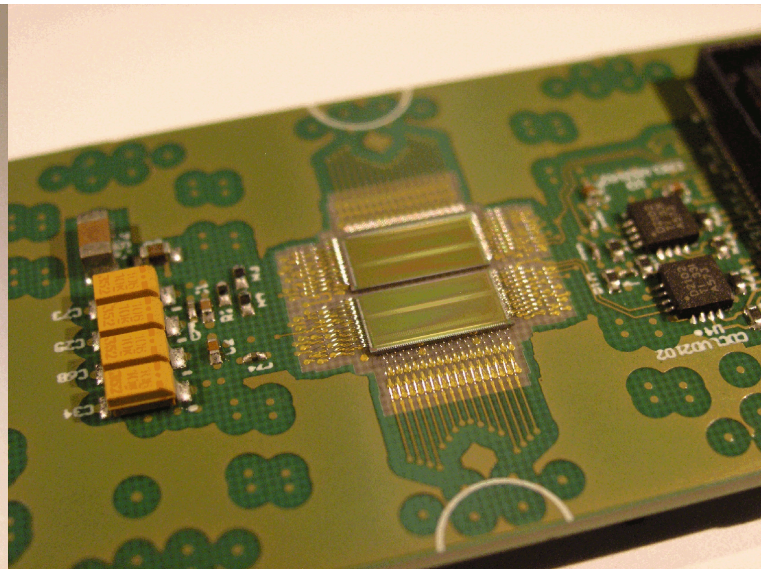
Energy Calibration - **preliminary**

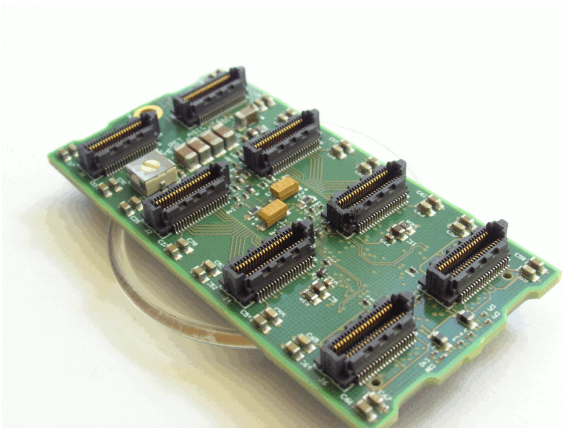
- ToT vs. Qin characteristic is non-linear
- Data aquired with ^{22}Na, ^{176}Lu, ^{137}Cs
- Fit to an exponential function to correct energy spectrum
- **Preliminary** energy resolution 17%

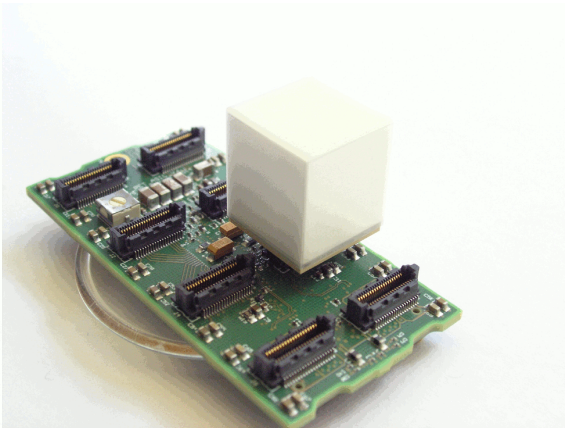


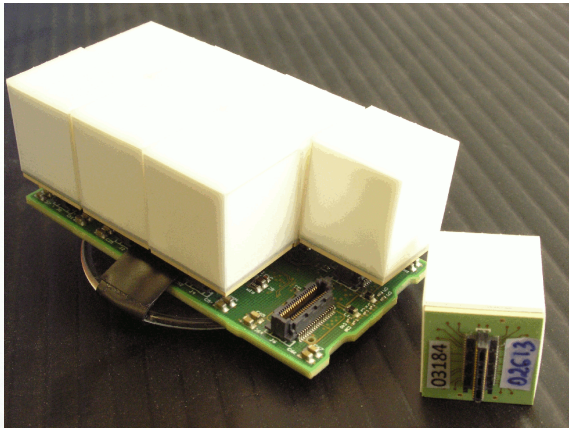
New hardware development: FEB/A for 2 ASICs



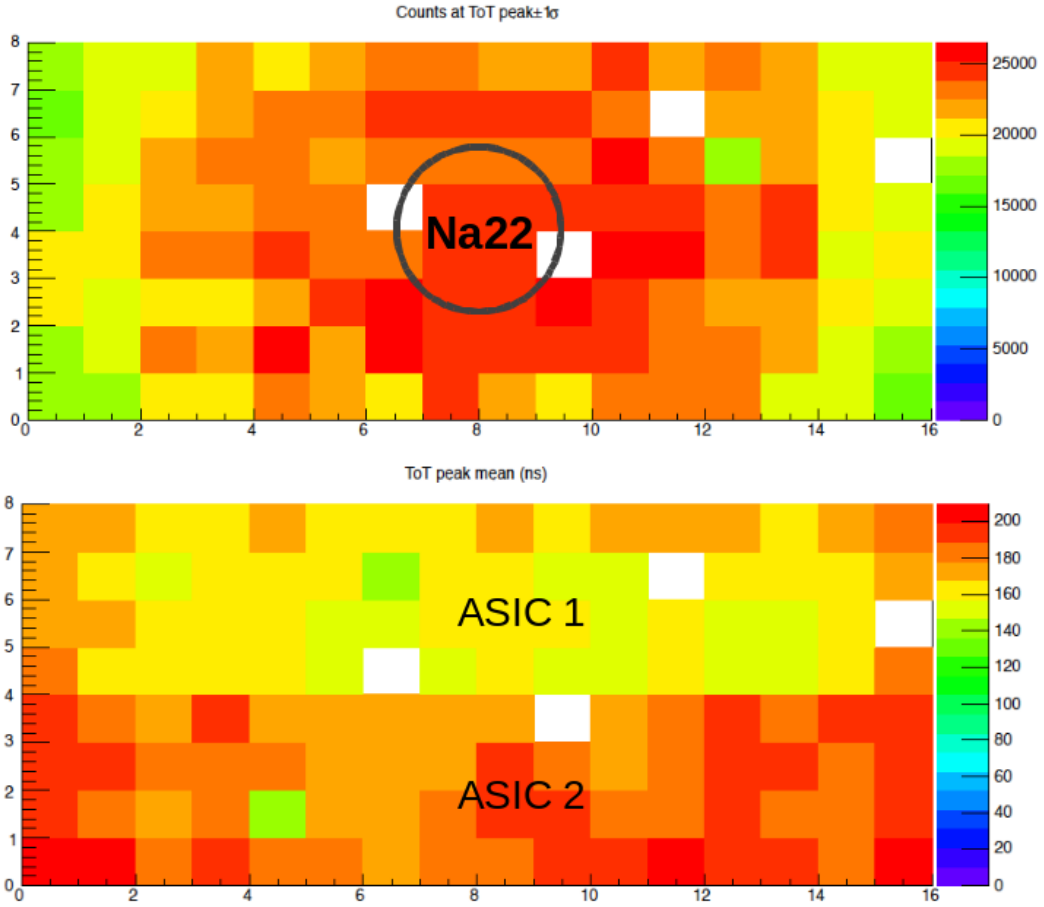








First tests with FEB/A - occupation map



Flood histogram:

- 128 channels
- number of counts in the photopeak

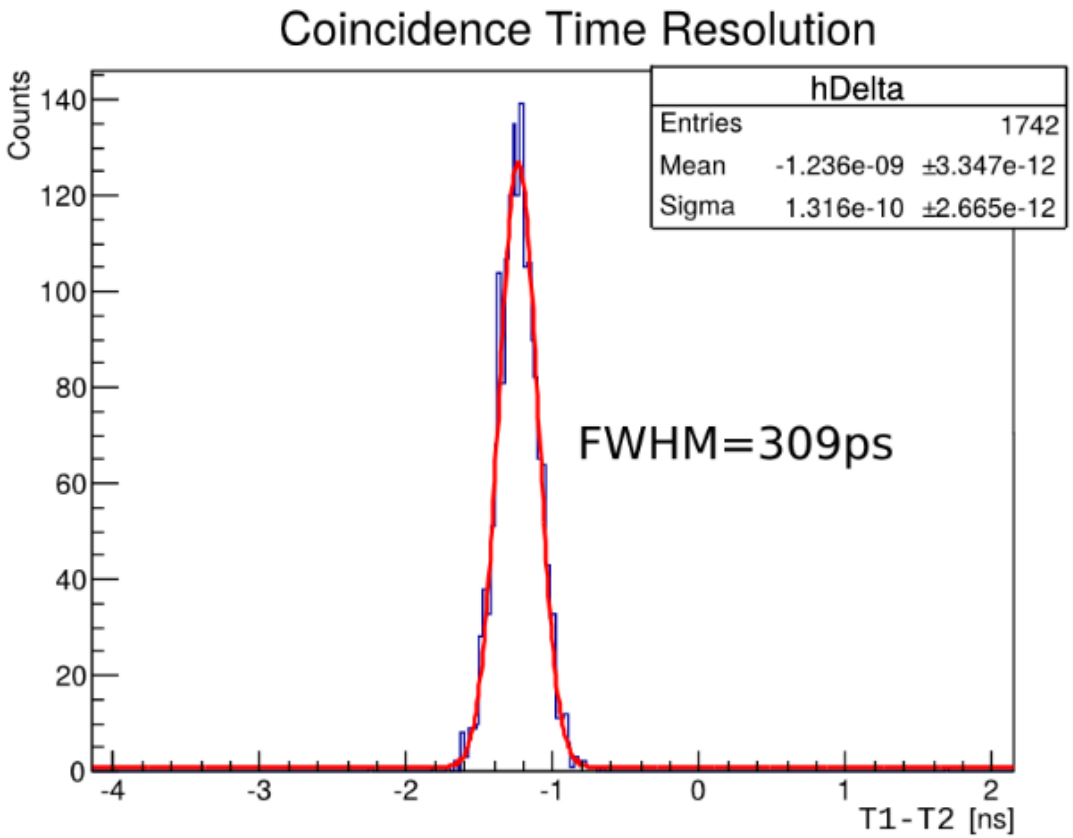
Source placed 37 mm above crystals

Photopeak position ToT (ns)

White spots: automatic calibration failed in 4 channels

First tests with FEB/A - CTR

- MPPC discrete TSV 4x4 arrays (3 x 3 mm^2 pixels)
- Crystal 4x4 matrix on each array (3.5 x 3.5 x 15 mm^3)
- Crystal-SiPM matching 73 %

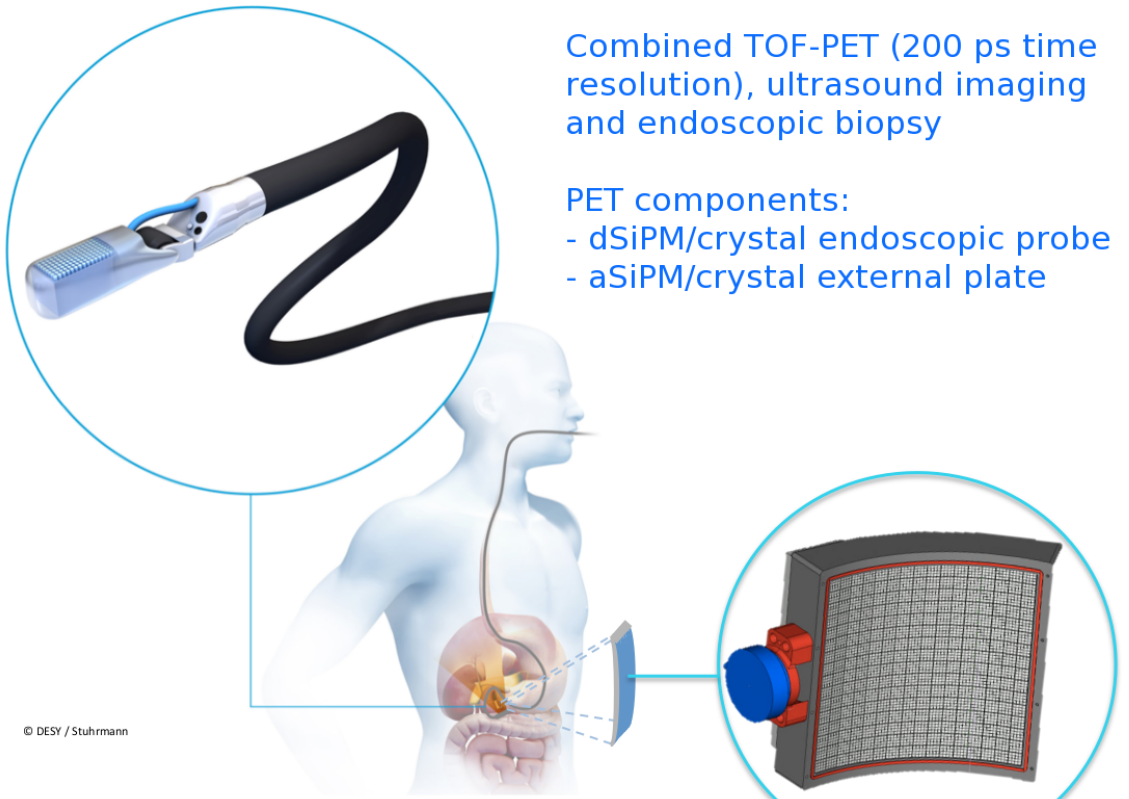


Outline

Status and Outlook

- ASIC distributed to several groups for Medical Imaging and HEP
- Integration of EndoTOFPET-US external plate - FEB/A characterization ongoing
- TOFPET offspring under way
  - **TOFPETv2** - design ongoing at PETsys
    - Targets time resolution better than 20 ps r.m.s.
    - high-rate applications
    - Linear ToT
    - improved energy resolution

EndoTOFPET-US FP7: Endoscopic PET and Ultrasound



Thank you!

Test setup for SPTR and MPTR tests

- Tests with Bare Die
  - MPPC: TSV arrays (3x3 mm^2)
  - (for CTR only): 15 mm^2 long LYSO
  - nominal: 160 MHz, DVDD=1v5
- PicoQuant Laser
  - MPTR: LI=1.5, no optical attenuator ($N_{ph} >> 1000$)
  - SPTR: LI=7.5, WITH optical attenuator ($N_{ph} = 1$)
- Nominal test conditions:
  - T = 18-20 C
  - TP rate = 80 KHz
  - V_{thE} approx 500mV above $V_{th,noise}$
  - V_{thT} approx 10mV[1] above $V_{th,noise}$

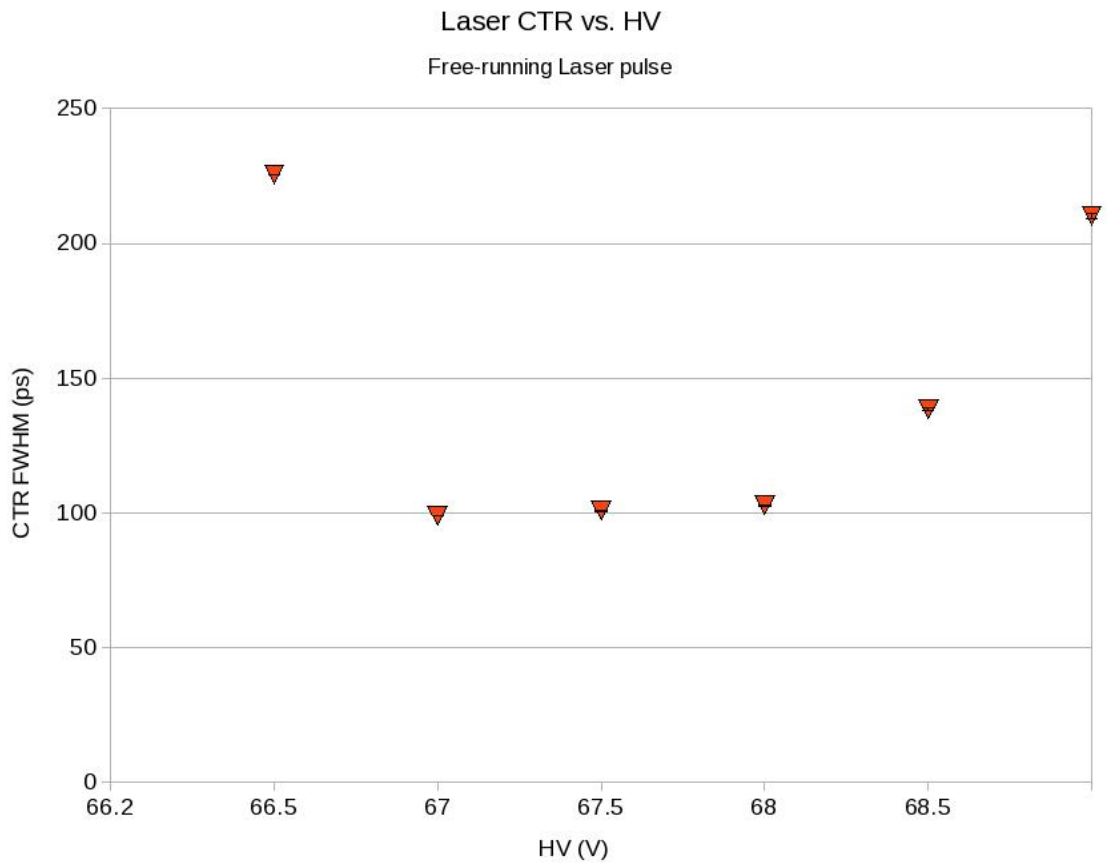
[1] for CRT with LYSO, nominal V_{thT} setting is to 100 mV above noise (corresponds to a threshold of 2-3 equivalent photoelectron charge)

Laser CTR

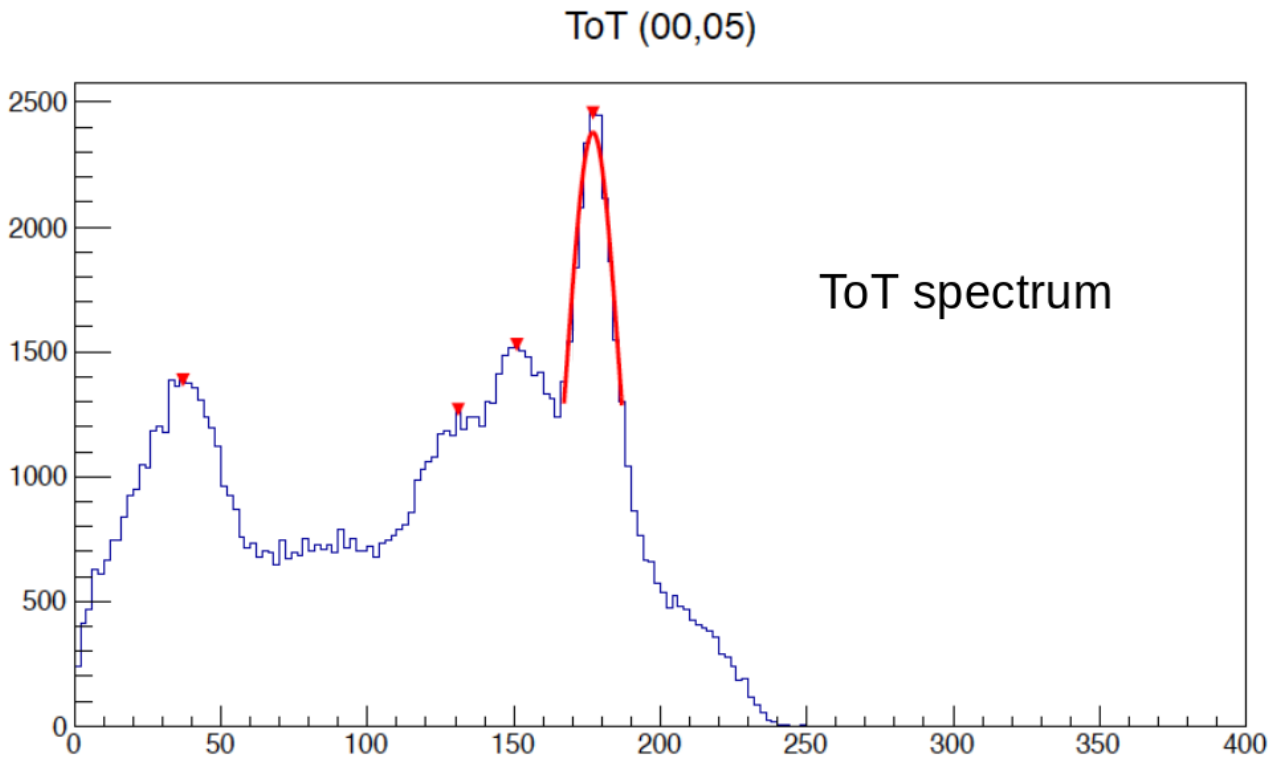
- free-running laser

↪ $CTR_{laser} = 100\ ps\ FWHM$

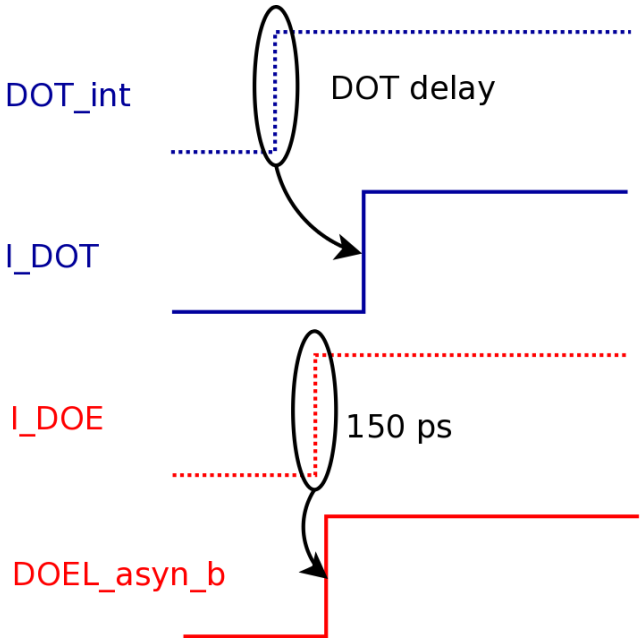
- $mptr_{sigma} = CTR_{laser}/(2.35 \times \sqrt{2}) = 30$ ps r.m.s.

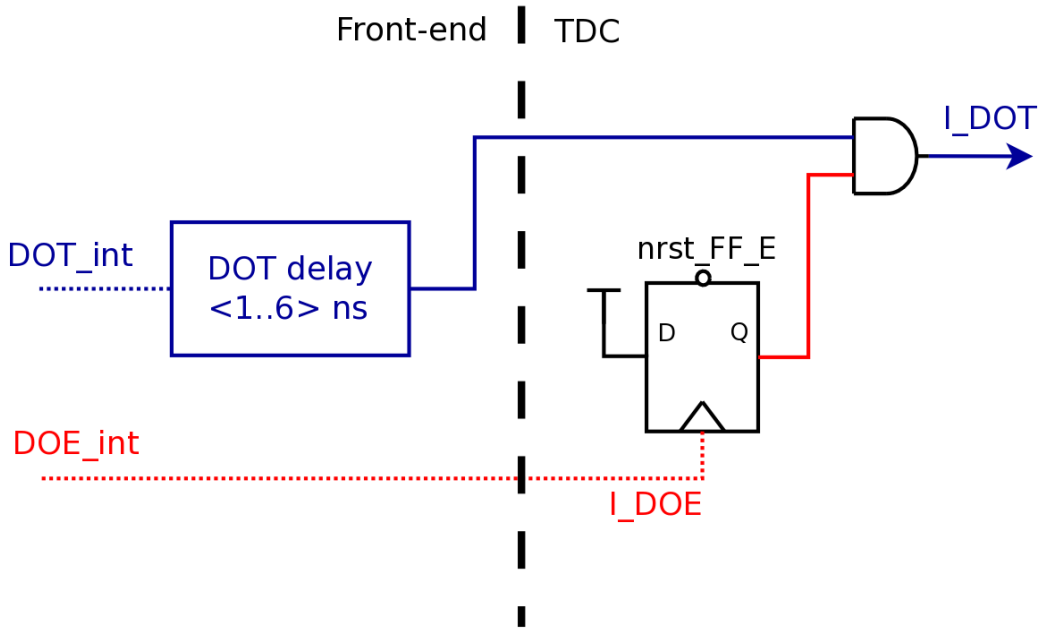


First tests with FEB/A - ToT



Operation with SiPMs - Rejection of dark pulses



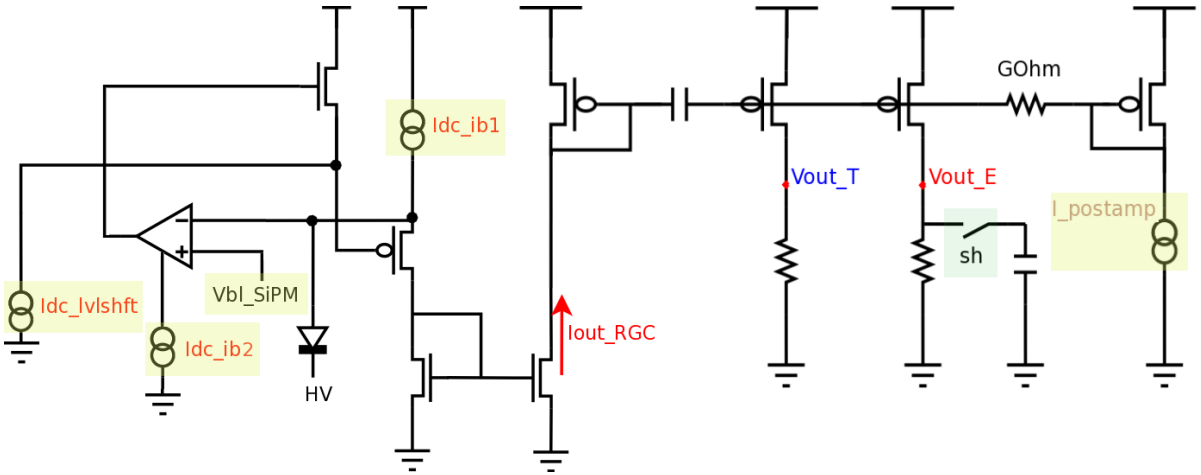


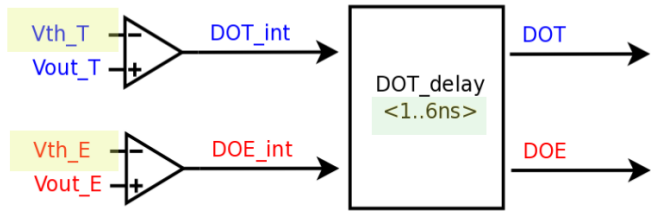
Filtering of spurious pulses: TDC is not triggered

- Quiet operation mode: limited TDC CTRL switching, TAC re-assignment,...
- Critically dependent on the quality of the power supply (main contributor for the delay line jitter)
- Synchronous validation schemes are implemented as backup.

Concept of the front-end

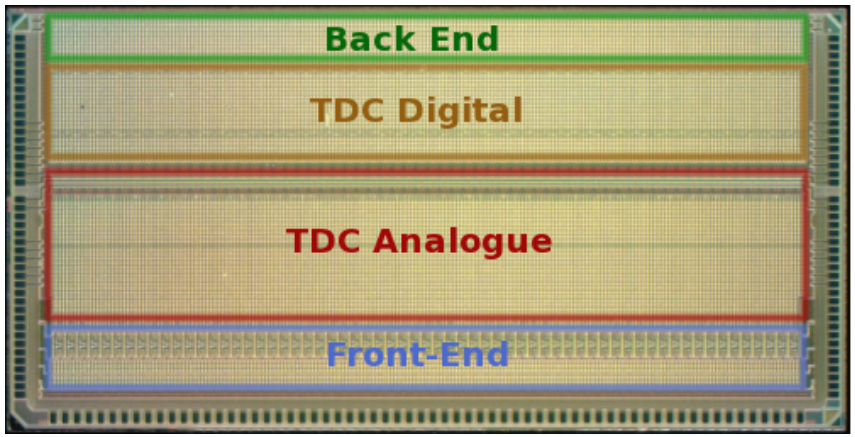
- Low-Zin pre-amplifier, 2 independent TIA branches for Timing and Energy triggers
- Fine adjustment of the HV bias (6-bit over 500mV range) of the SiPM
- Selectable shaping function for Vout_E
- Selectable delay line for dark count filtering
- Usable for p-type or n-type (hole, electron collection) devices

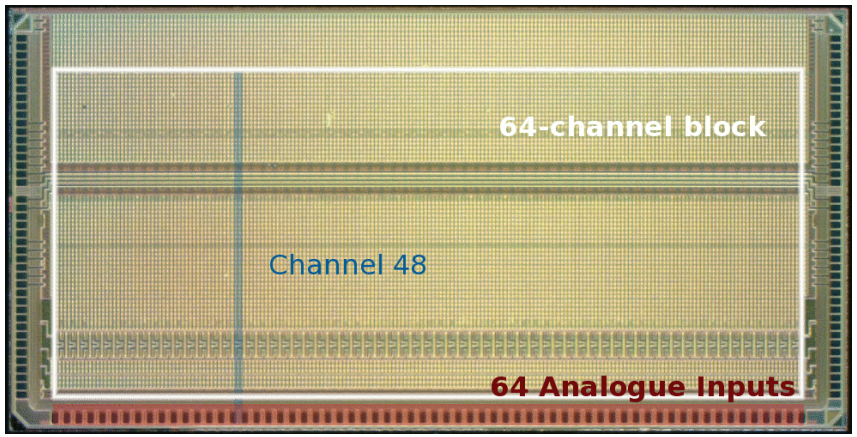




Configurable with on-chip 6-bit DACs

Floorplan of the 64-channel IC





- 64 channels side-by-side, 102 μm pitch
- calibration circuits, reference and bias generators