Profiler test electronics: development of the evaluation board

Matteo Cecchetti, Giuseppe Battistoni,
Mauro Citterio, Alessandro Andreani,
Adalberto Sciubba

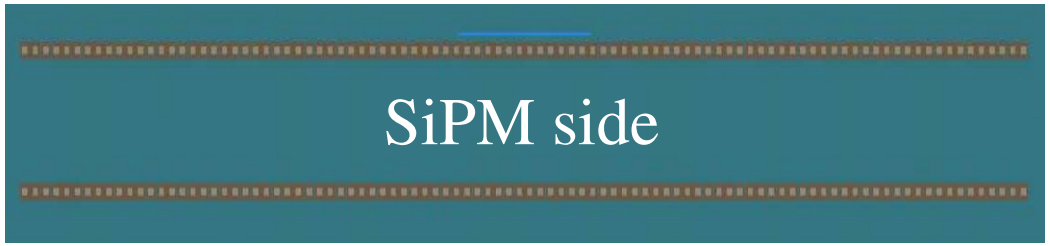
INSIDE Meeting – 15th September 2014, Torino

INFN
Istituto Nazionale
di Fisica Nucleare
SEZIONE DI MILANO

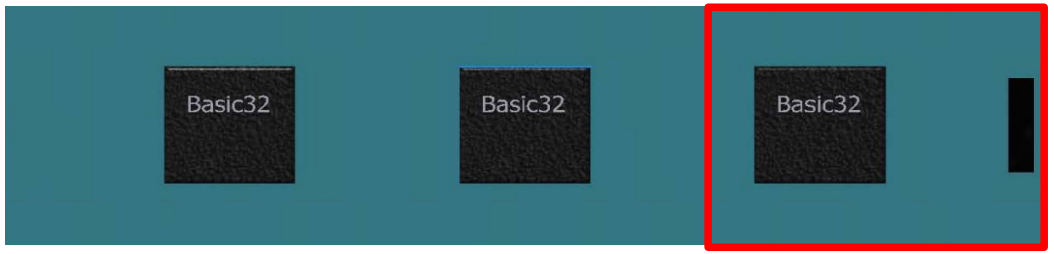
- The evaluation board has been fully designed; it represents a subset of the final board
- **The production of 5 boards is ongoing**
- The board testing will begin during next weeks

Final Board

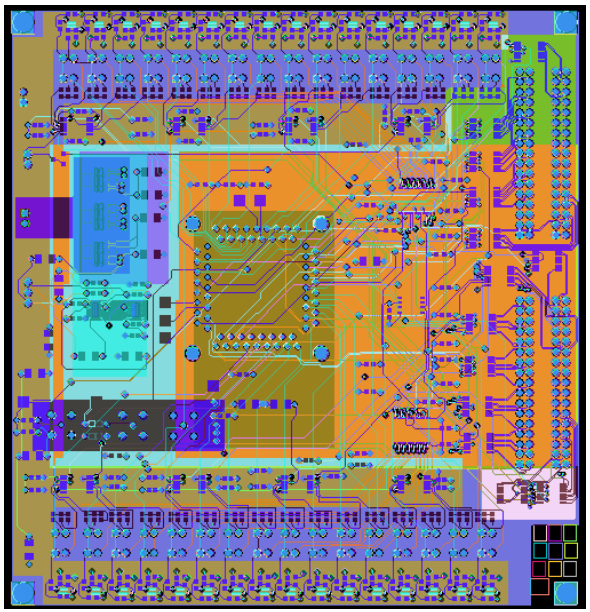
TOP view



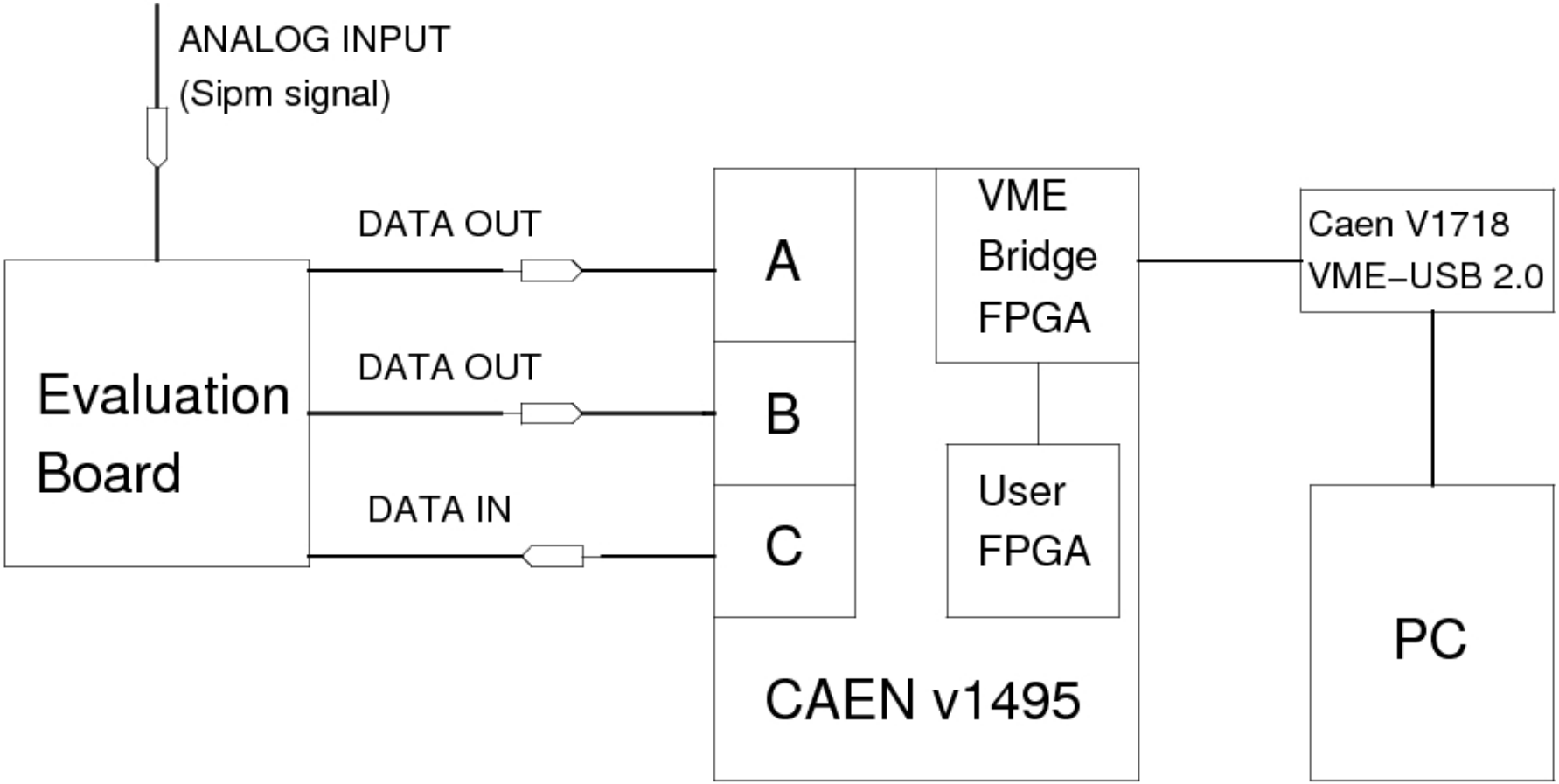
BOTTOM view



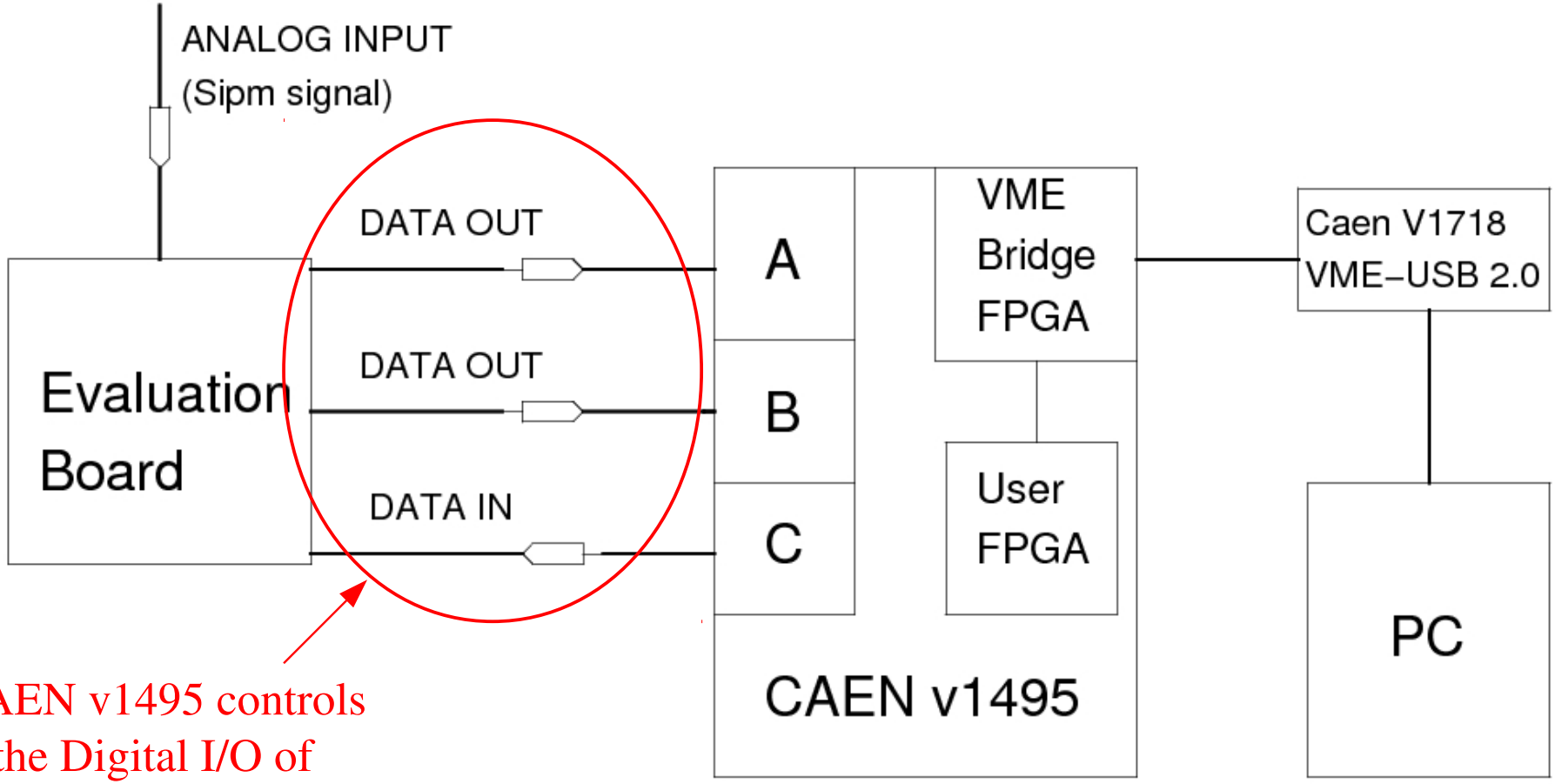
Evaluation Board



How the evaluation board will be used

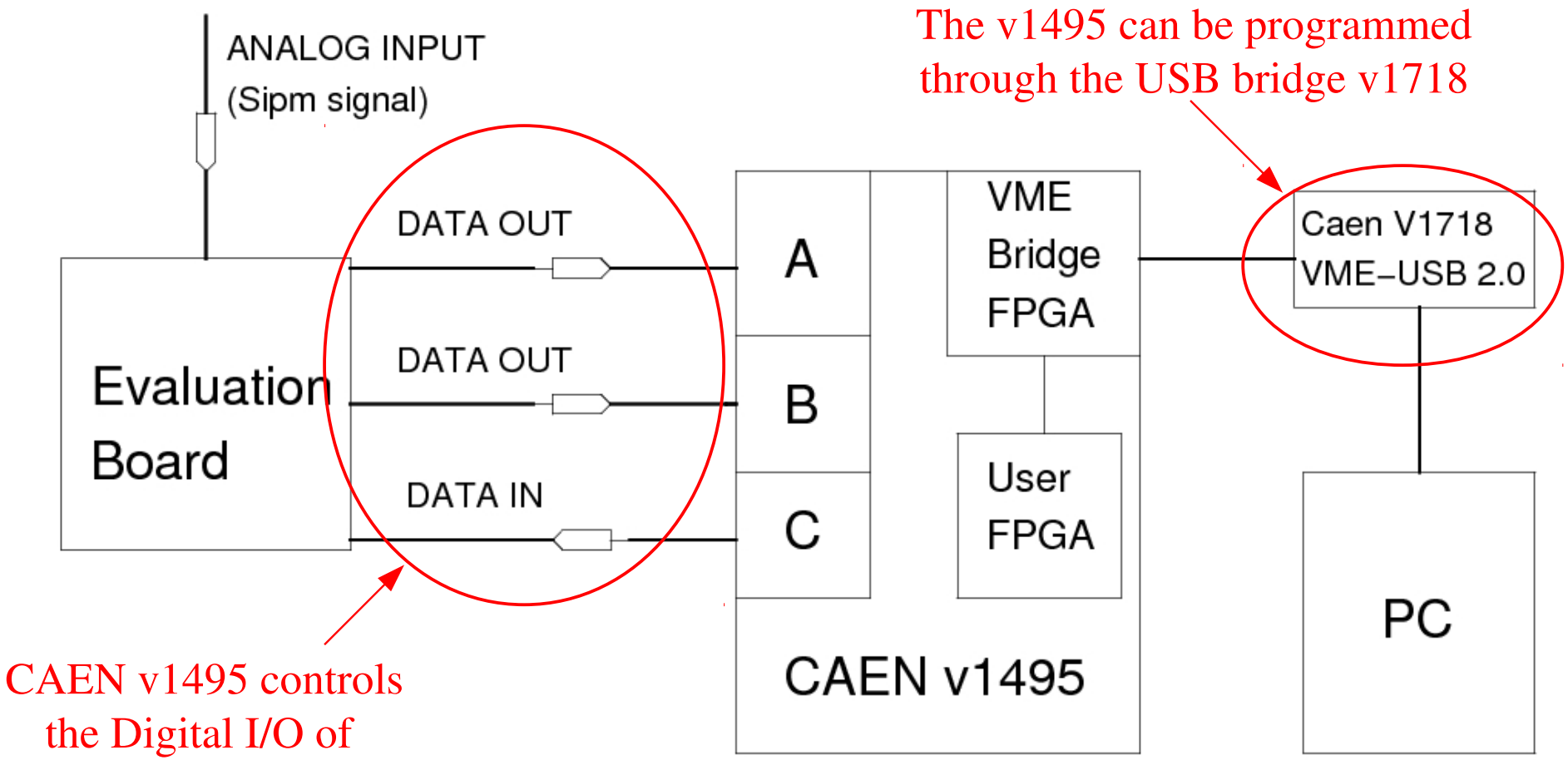


How the evaluation board will be used

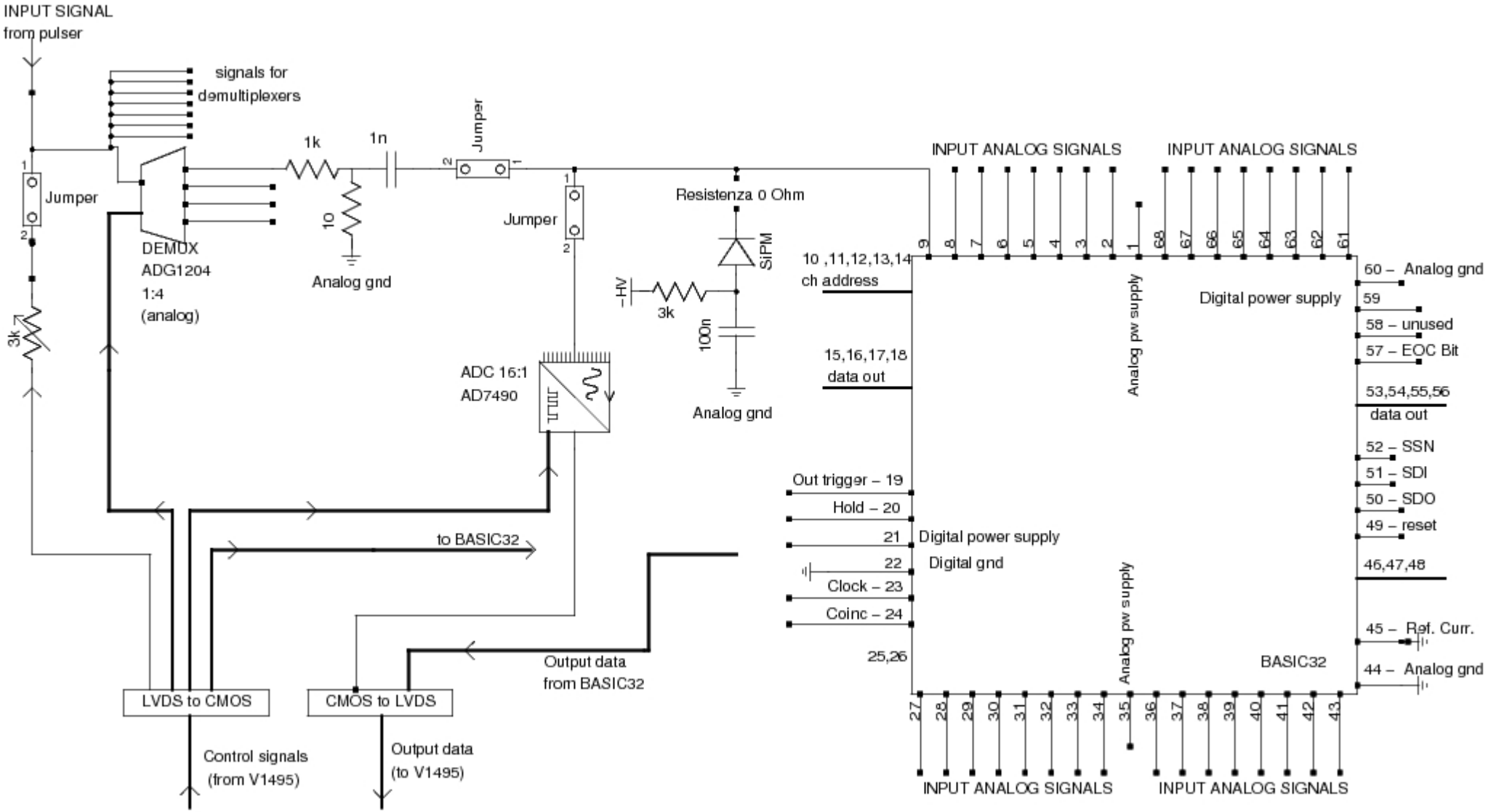


CAEN v1495 controls the Digital I/O of the evaluation board

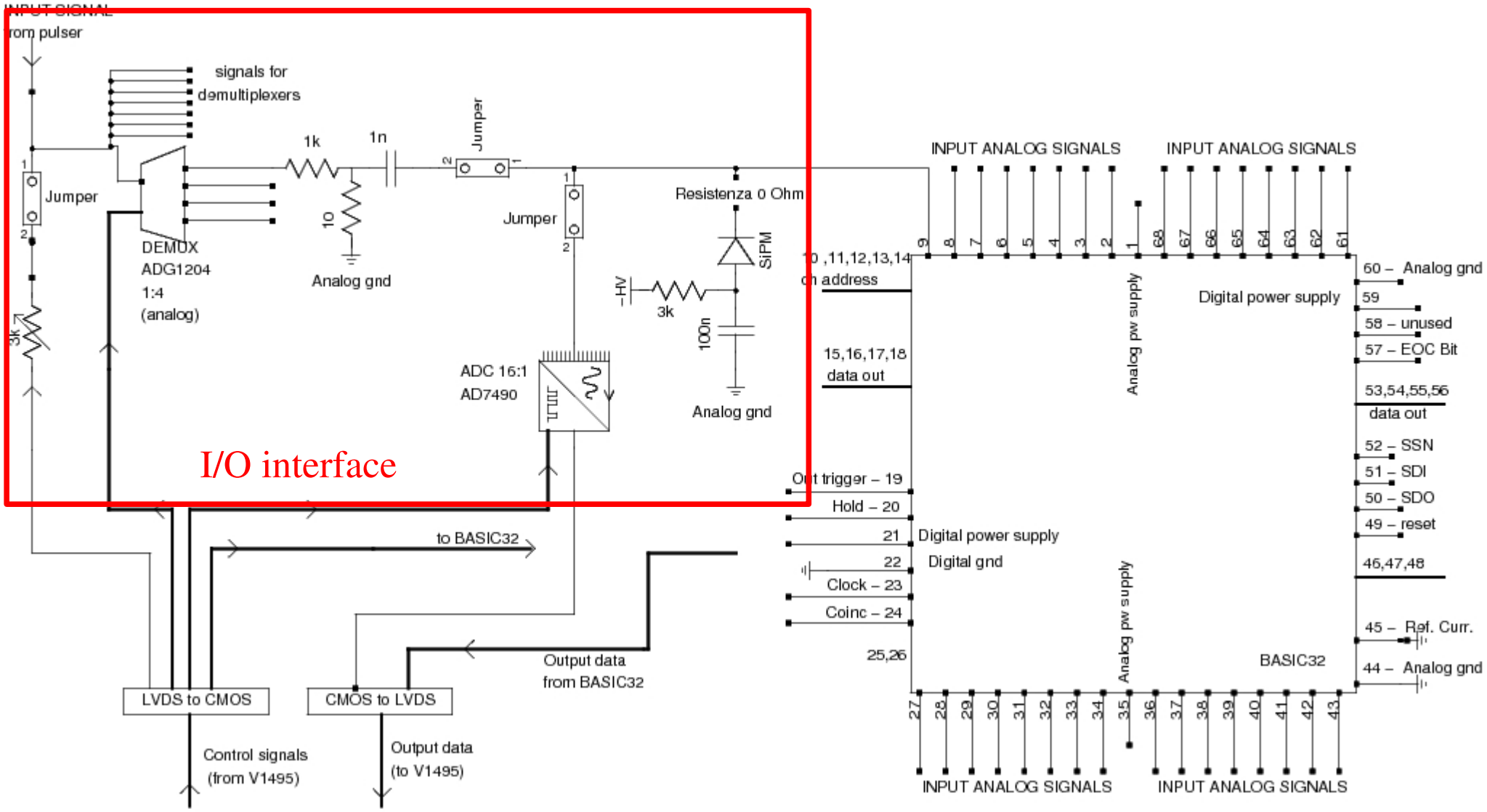
How the evaluation board will be used



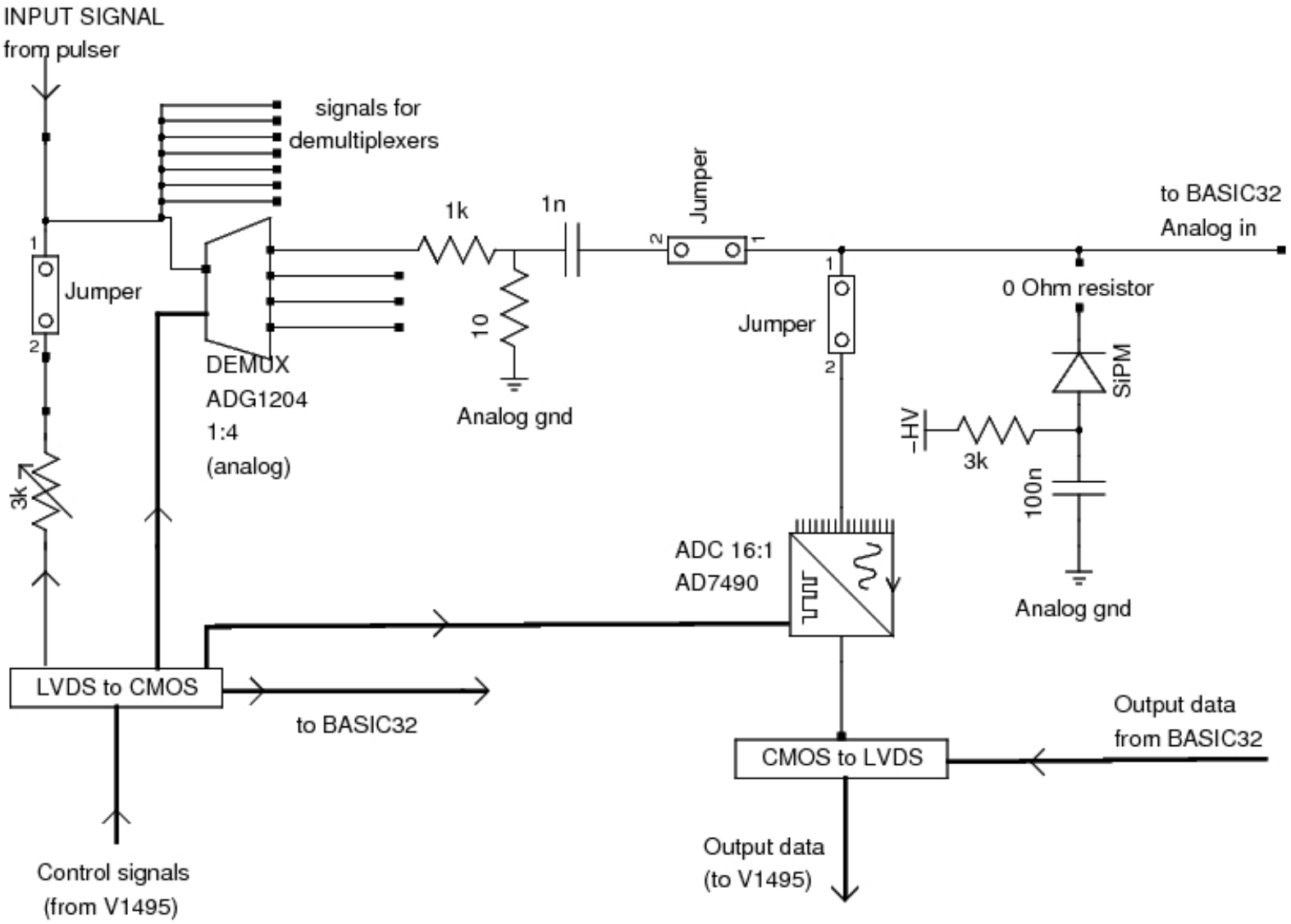
Main features of the board



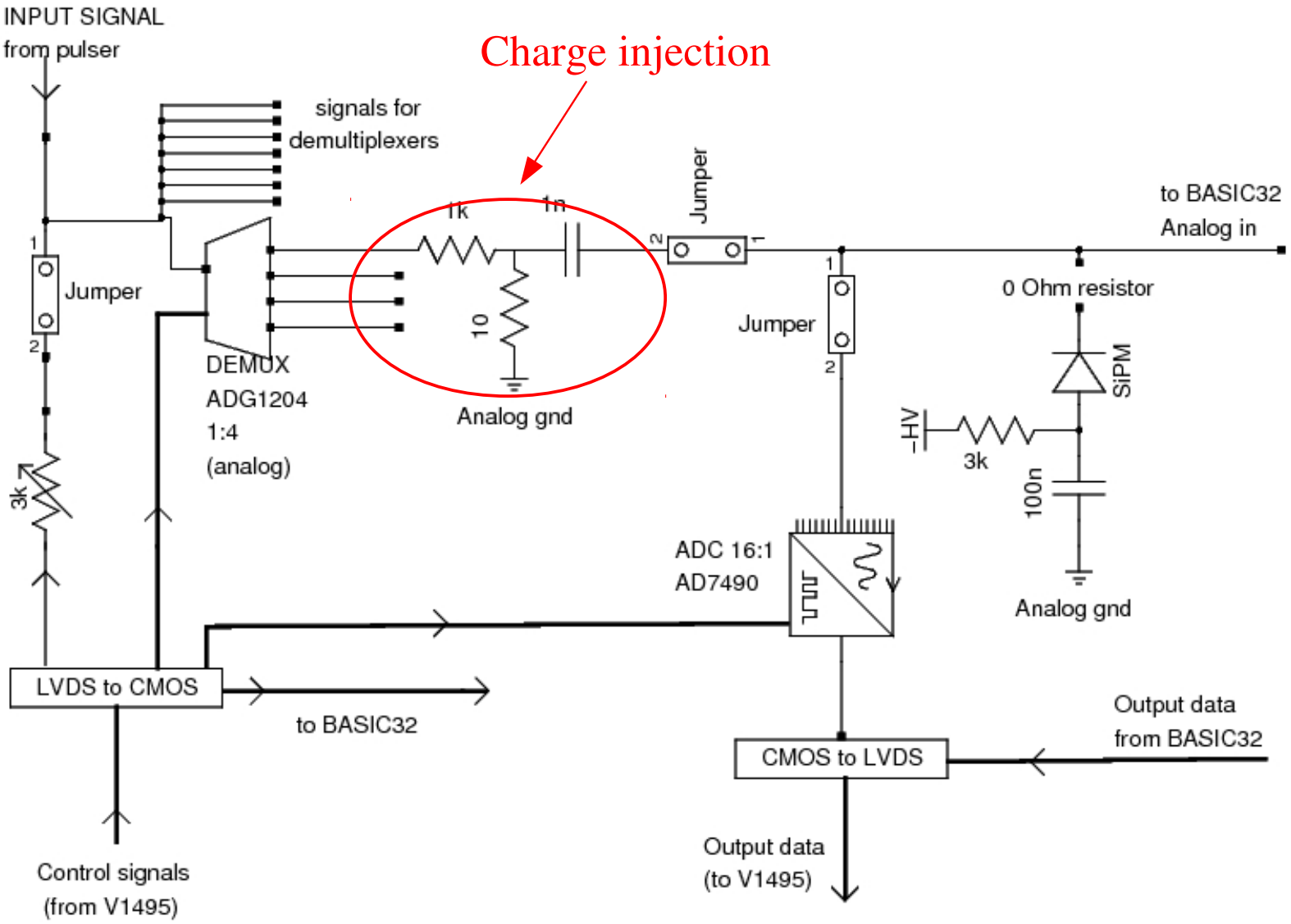
Main features of the board



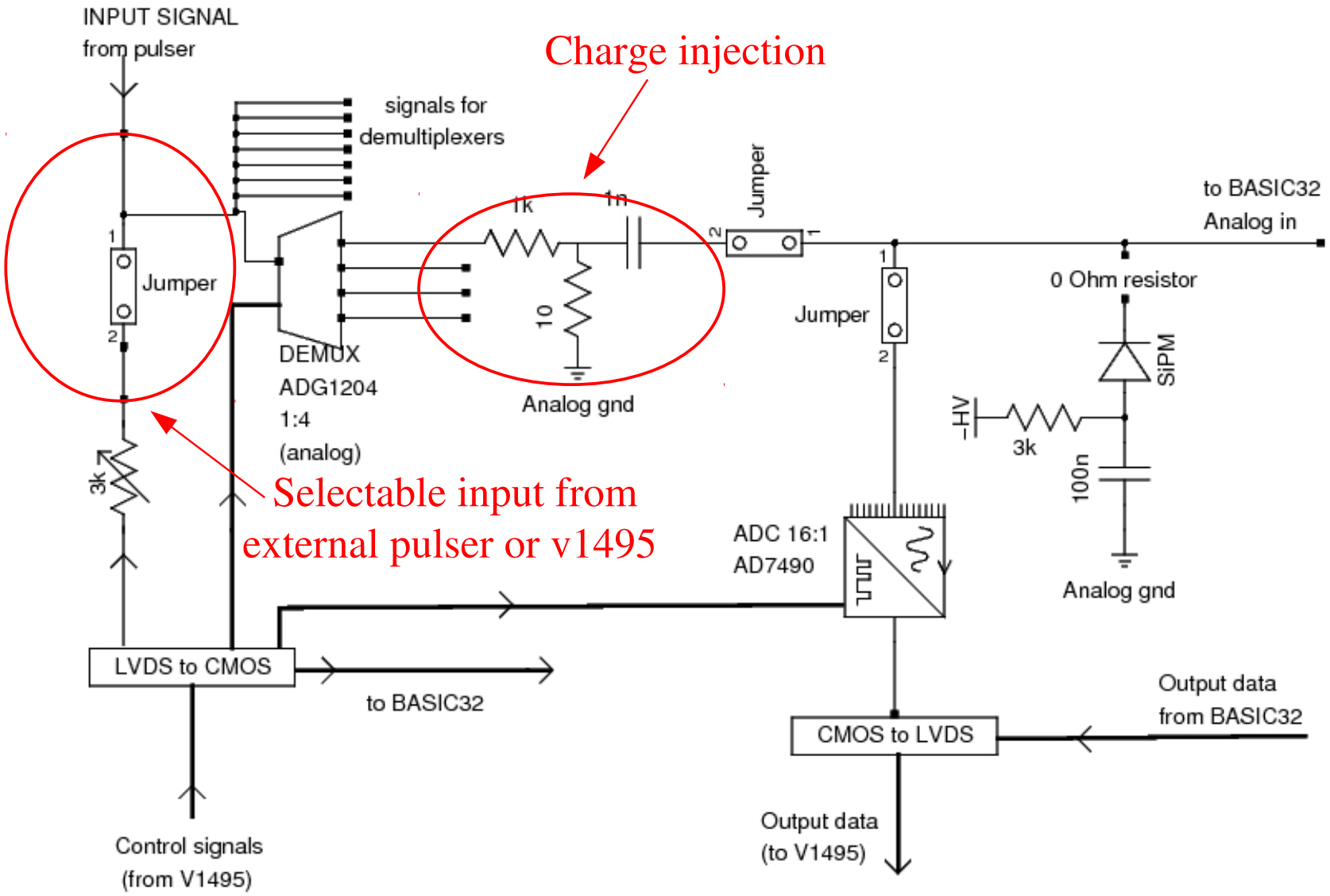
Details of the I/O interface



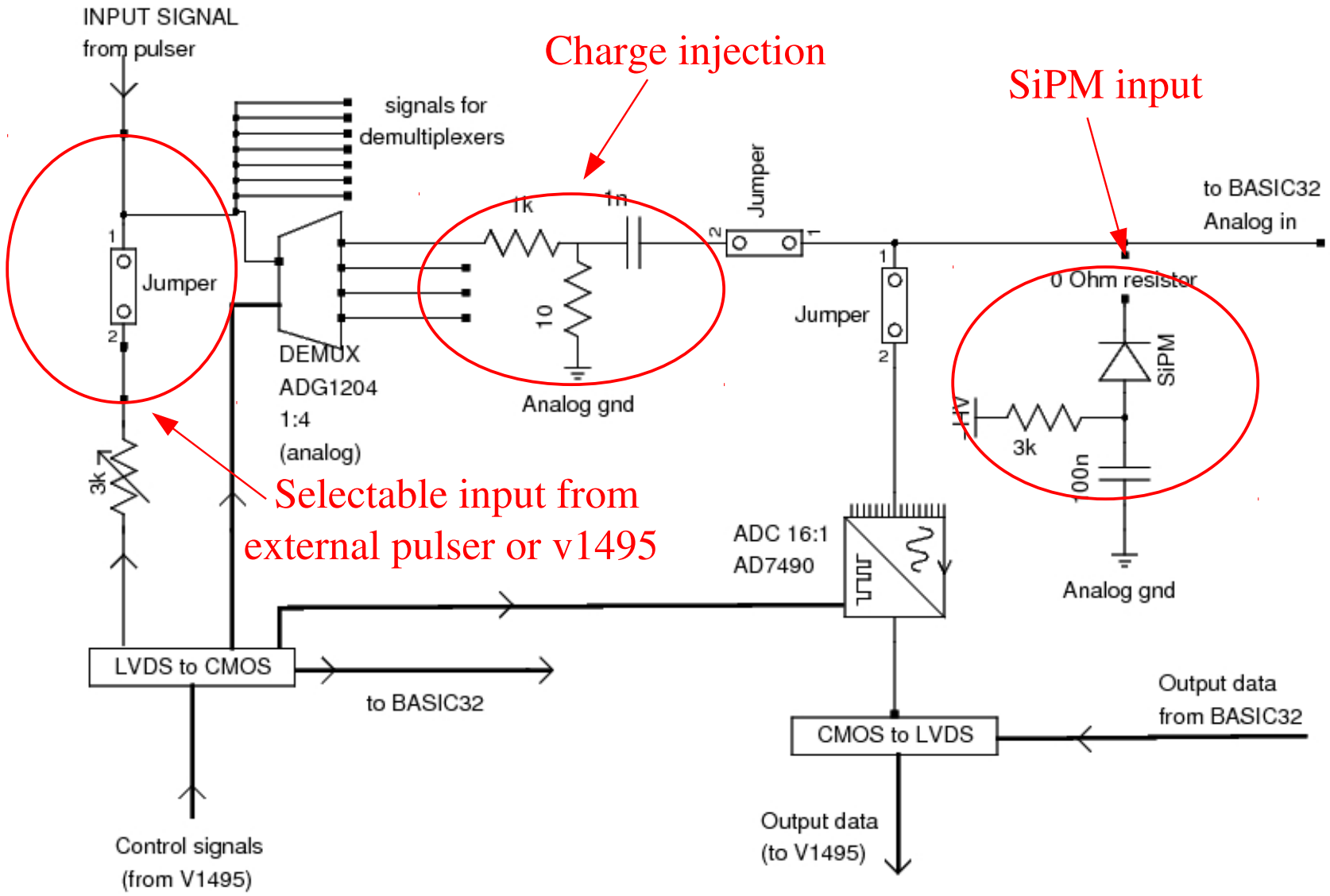
Details of the I/O interface



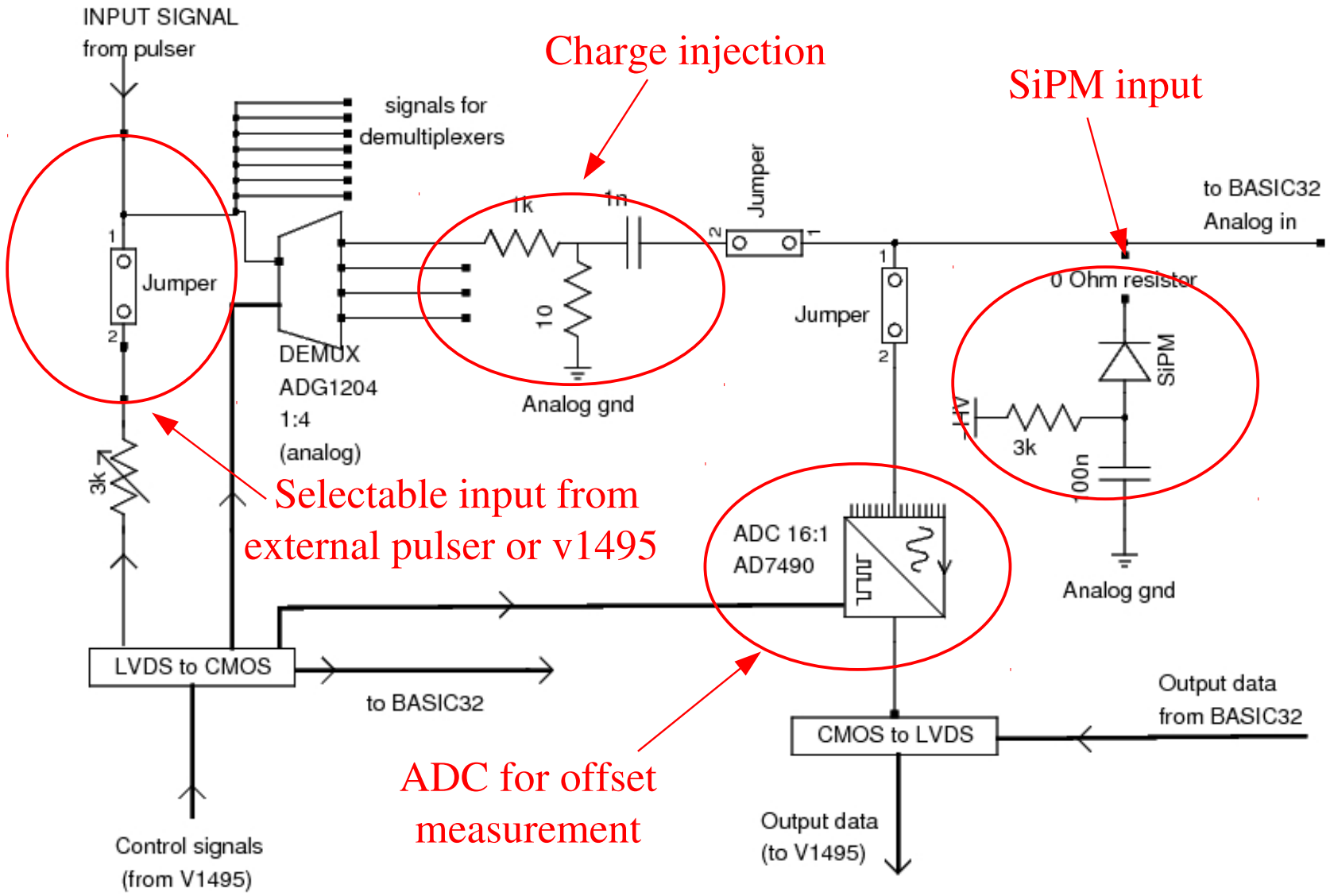
Details of the I/O interface



Details of the I/O interface

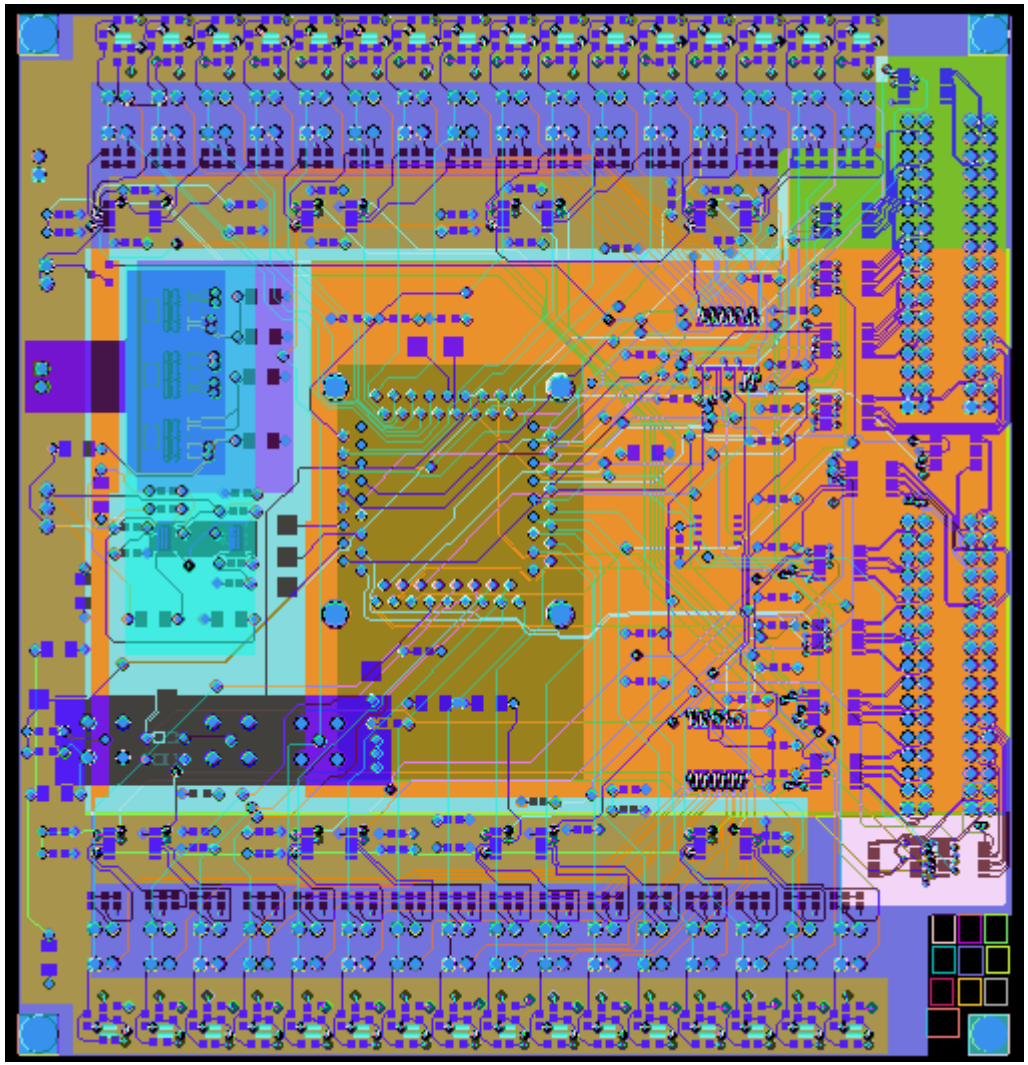


Details of the I/O interface



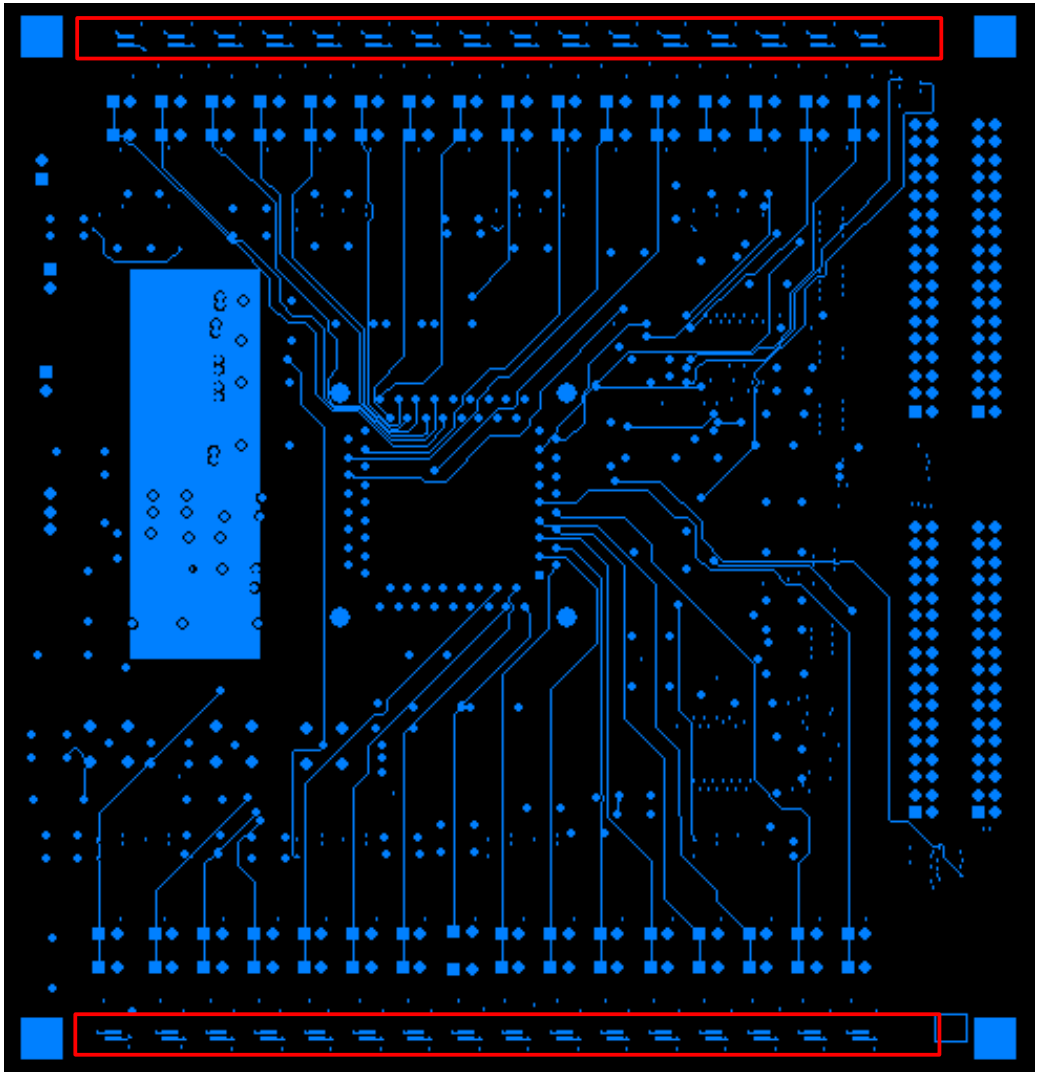
Main features of the layout

- 10 layers with separated Analog and Digital GND
- The SiPMs are mounted on TOP layer and the other components on BOTTOM layer



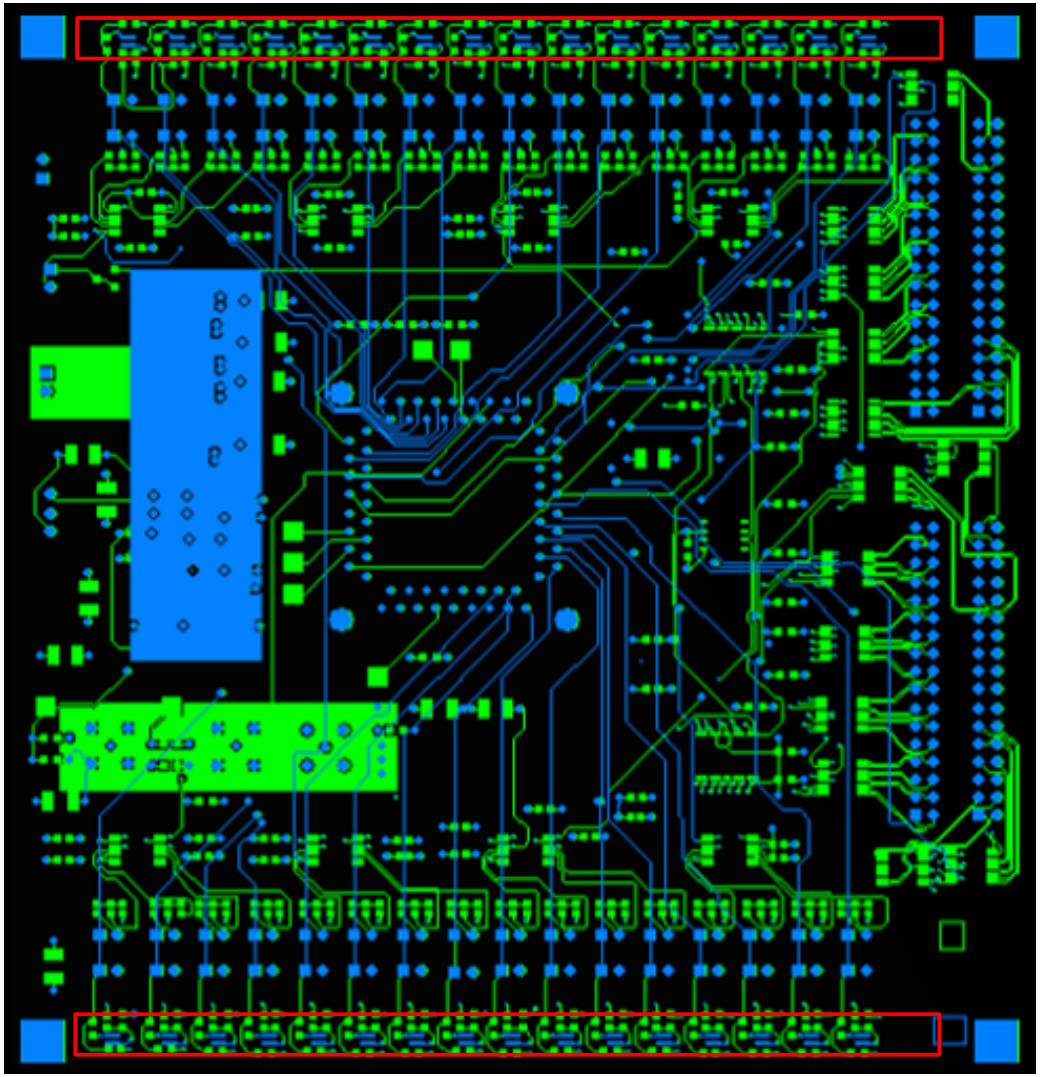
Main features of the layout

- 10 layers with separated Analog and Digital GND
- The SiPMs are mounted on TOP layer and the other components on BOTTOM layer



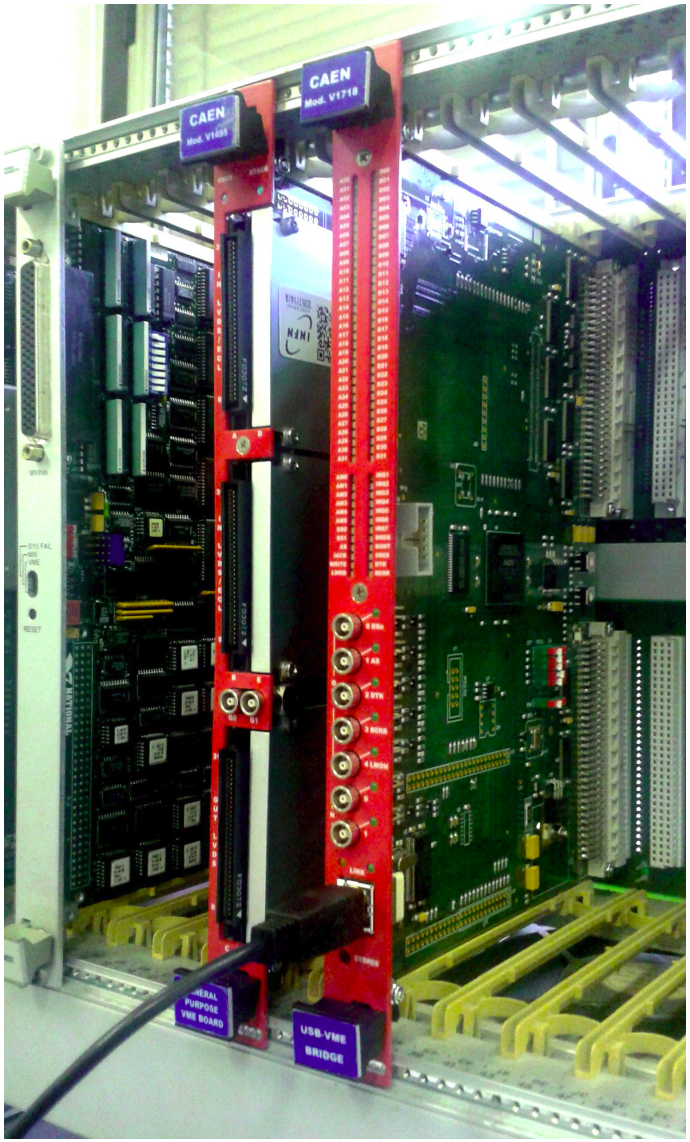
Main features of the layout

- 10 layers with separated Analog and Digital GND
- The SiPMs are mounted on TOP layer and the other components on BOTTOM layer



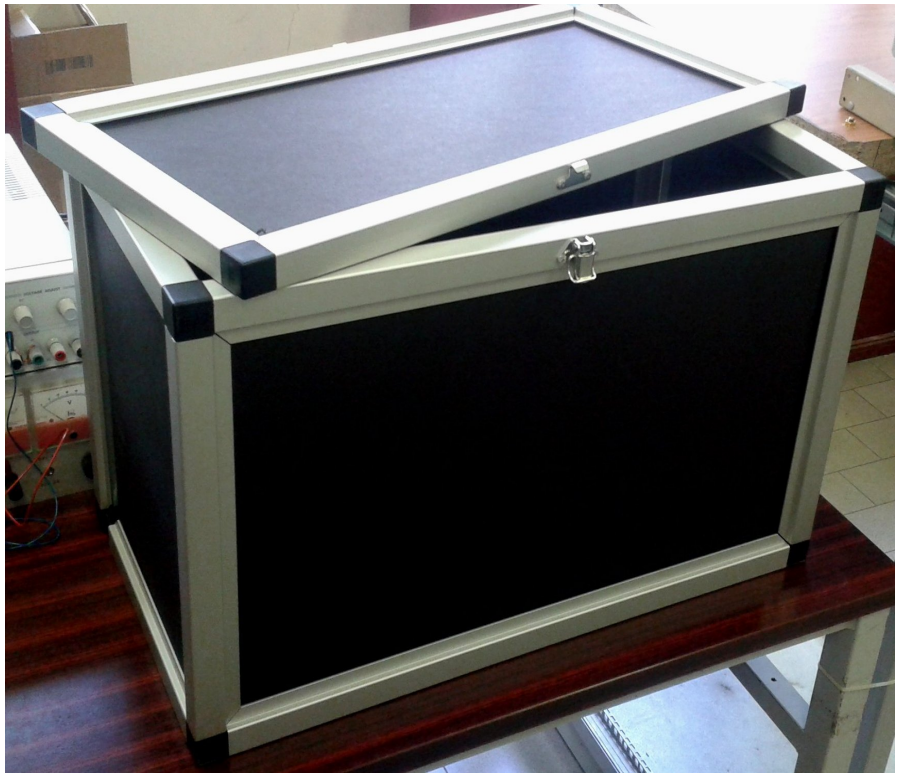
Next steps

- I/O board test using the CAEN board (v1495)
- SiPM input test within the Light Tight Enclosure (Newport LTE-12)



Next steps

- I/O board test using the CAEN board (v1495)
- SiPM input test within the Light Tight Enclosure (Newport LTE-12)



Thanks for your attention!