Indium bonding @Selex

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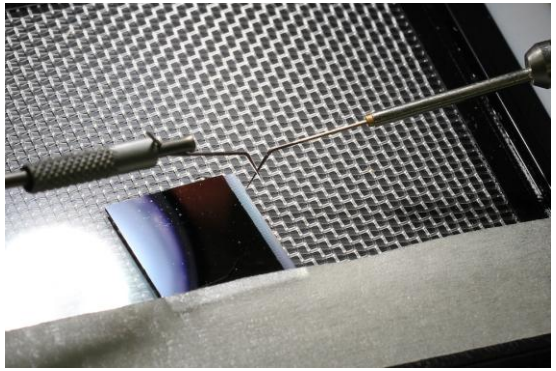
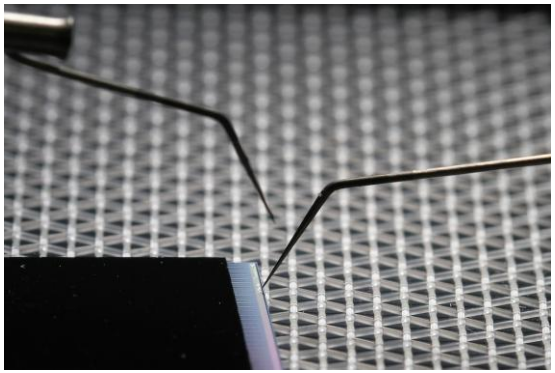
Same technology used for about half the Atlas Pixel Detector modules but:

- Larger (~19x20 mm^2 instead of 7x11 mm^2) and thinner (100 μm) chips (Atlas FE-I3 thinned down to about 180 μm)
- One order of magnitude more bumps (26880 instead of 2880) due to a larger chip area and a smaller pixel size (50x250 μm^2 instead of 50x400 μm^2)



Tests performed at Genova by G. Darbo, C. Gemme & A. Rovani



From the bumping point of view, the higher density requirement of 8000 contacts/cm^2, or 26880 bumps per readout IC, is achievable, provided the minimum pitch of 50 μm.

The critical parameters for the bonding process are the larger size of the read out chip, together with the requirement of a much thinner chip.

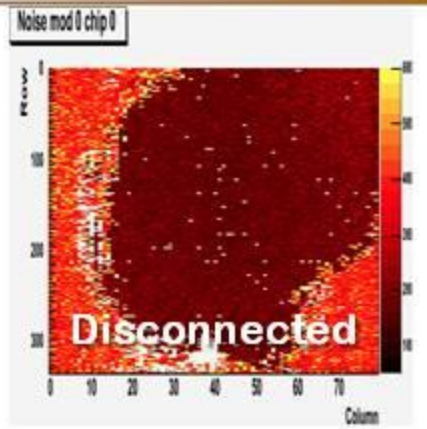
Possible origin of problems for the hybridization step are:
•handling of such a thin and large chip
•planarity with respect to the sensor during flip-chip
•deformations coming from internal stress of the chip and/or working temperature during the bonding step

The indium bump bonding technique is an appealing candidate for coping with these problems because it requires just one Under-Bump Metallization (UBM) step and a low (90 ˚C) maximum working temperature. Therefore a research and development collaboration has been arranged between INFN and Selex to develop this process up to the point to produce assemblies with FE-I4 chips thinned down to 100 μm.

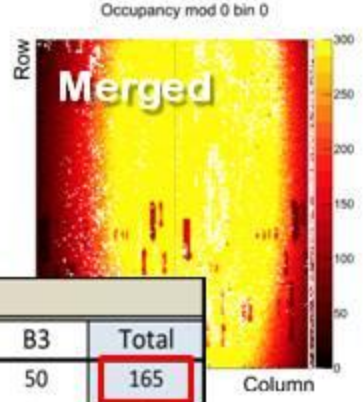
Bump-bonding Yield

Ref: Pixel Col. - 2012 JINST 7 P11010

Bare modules	Indium		PbSn		Total	
	Modules	Fraction	Modules	Fraction	Modules	Fraction
Assembled	1468		1157		2625	
Rejected	172	11.7%	35	3.0%	207	7.9%
Accepted (total)	1296	88.3%	1122	97.0%	2418	92.1%
Accepted as delivered	1101	75.0%	1035	89.5%	2136	81.4%
Accepted after reworking	195	13.3%	87	7.5%	282	10.7%



- *IZM yield on BB passing from small chip (0.5cm^2) to large chip (4cm^2) dropped significantly*
  - Yield (16xFE-I3) ~90%
  - Yield (1xFE-I4 – 2xFE-I4) ~ 50-60% averaged on the current IBL module production (>250 modules assembled)



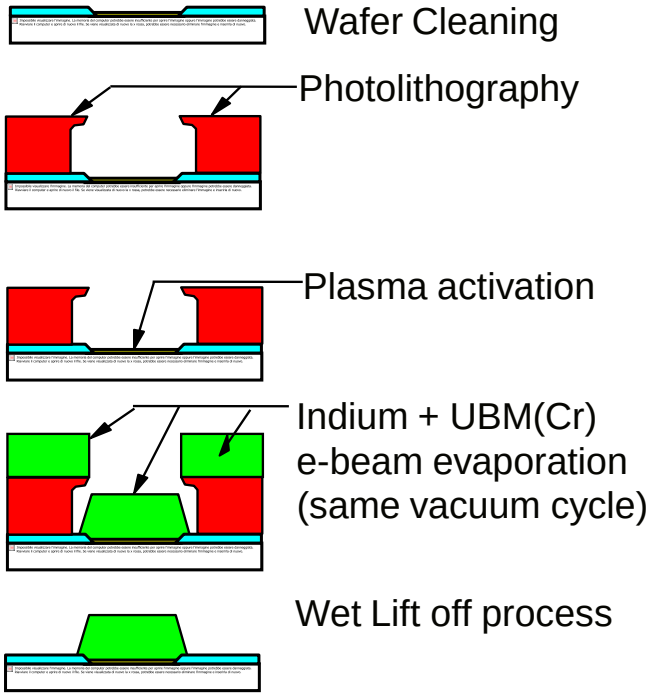
	SC						DC					
	B1	B2	B4	B5	B3	Total	B1	B2	B4	B5	B3	Total
Total Built	18	16	14	15	37	100	26	48	11	30	50	165
Total Bad w/o BB	5	3	0	3	9	20	7	4	2	8	3	24
Failure Rate w/o BB	**0,28**	**0,19**	**0,00**	**0,20**	**0,24**	**0,20**	**0,27**	**0,08**	**0,18**	**0,27**	**0,06**	**0,15**
Failure Rate with BB	**0,83**	**0,56**	**0,00**	**0,33**	**0,49**	**0,47**	**0,73**	**0,65**	**0,18**	**0,27**	**0,18**	**0,42**
gelpack	0	0	0	0	1	1	0	1	2	0	1	4
handling	0	0	0	0	0	0	1	2	0	5	0	8
IV sensor BARE/after BARE	3	1	0	3	8	15	2	0	0	1 / 0	1 / 0	4
Open/short LV/ no data	0	2	0	0	0	2	1	0	0	2	1	4
Broken regulators	2	0	0	0	0	2	3	1	0	0	0	4
Bump Bonding (open/shorts)	10	6	0	2	9	27	12	27	0	0	6	45

Note: B1/B2 modules not completely tested for BB

Ref: Claudia Gemme – June 2013 Pixel Week

The indium bump-bonding technique is a two-step process: the bumps deposition on both the silicon sensor and the IC wafers and the flip-chip assembly.

In the first process the indium bumps evaporated through a polyimide mask are about 9 μm tall with a defect rate, measured by optical inspection, on the order of 10^{-5}.
The UBM process is very simple: after plasma activation, about 10 nm of chromium are deposited just before indium is evaporated in the same vacuum cycle, with the temperature never exceeding 50 ˚C.

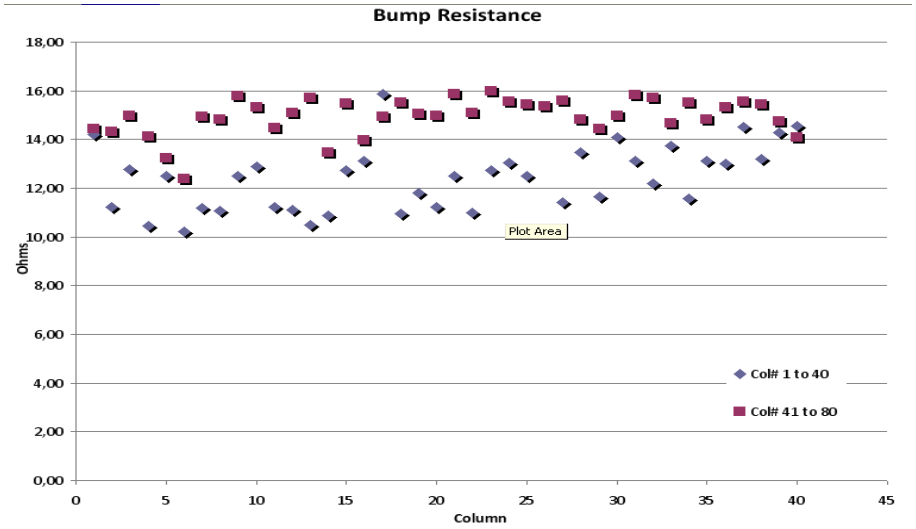


A cycle with controlled temperature and pressure allows the bumps to establish the electrical and mechanical connections.
The resulting bump has an height of about 12 μm and a diameter of about 20 μm.

Resistance measurement and X-ray images of the assembly, are a powerful method to optimize the planarity between the facing dies during flip-chip: a lower resistance comes from a larger bump that shows a higher pressure applied in that area of the assembly, very likely coming from a bad planarity between the dies.

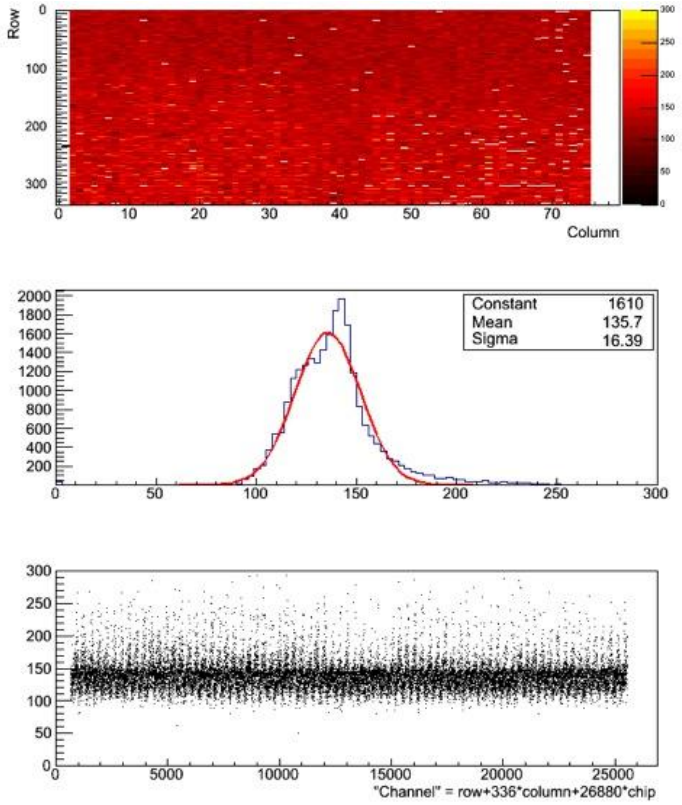
Selected Bonding parameters:

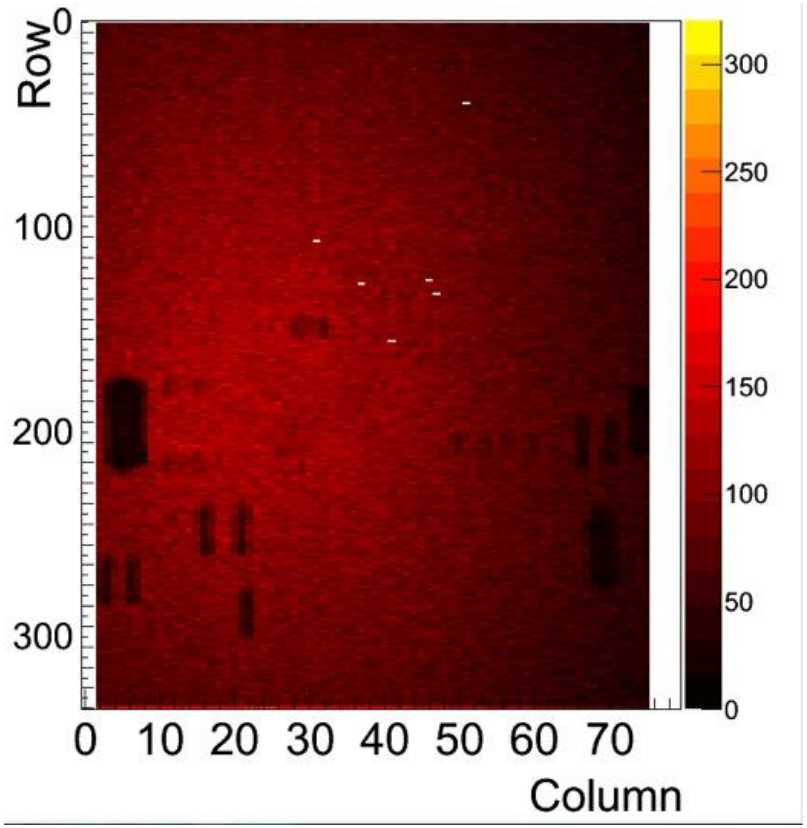
- **Force: 160N (on 26880 bumps)**
- **Substrate temperature: 90 ° C**
- **Chip temperature: 90 ° C**
- **Time: 42 s.**



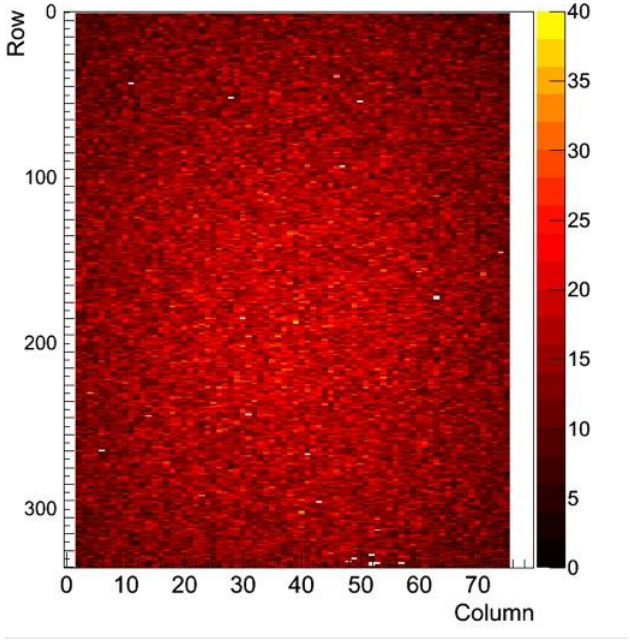
The flip-chip process parameters have been optimized and best results have been obtained with 160N force applied for 42 s at 90 ˚C. With such parameters, the electrical resistance value is uniform all over the assembly and has a value of 13±3 Ω per bump; this is compatible with the 10 Ω per bump obtained for the ATLAS pixel production, where lower pressure was applied (25N over 2880 bumps).

Module assembled on a module flex with 3D sensor and non thinned FE-I4a: results show no problem or damage caused by the indium bonding process. The shadows seen in the source scan are coming from SMD components, which are loaded on the flex circuit glued above the module and attenuating the Am^{241} gamma rays.



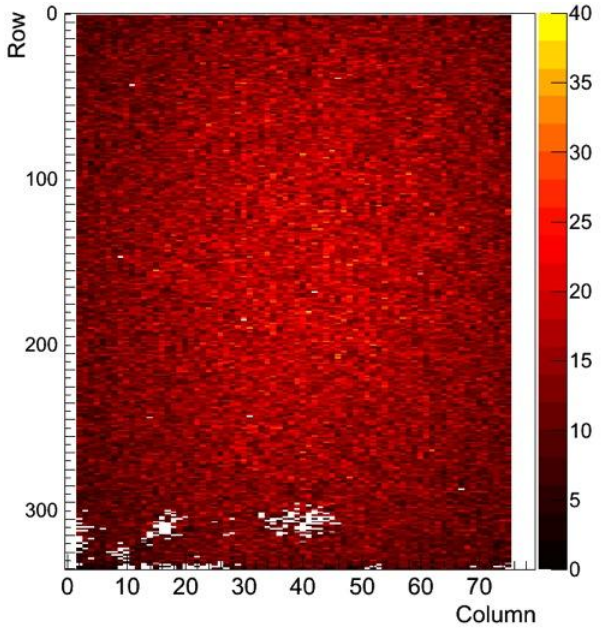


Good results are coming also from modules assembled with a planar sensor and a FE-I4a thinned to 200 μm. This is already an important step from the level reached for the ATLAS pixel production: the read out chips have about the same thickness but now have a much larger area that is a critical parameter for the indium bonding process.



100 μm thinned FE-I4a:

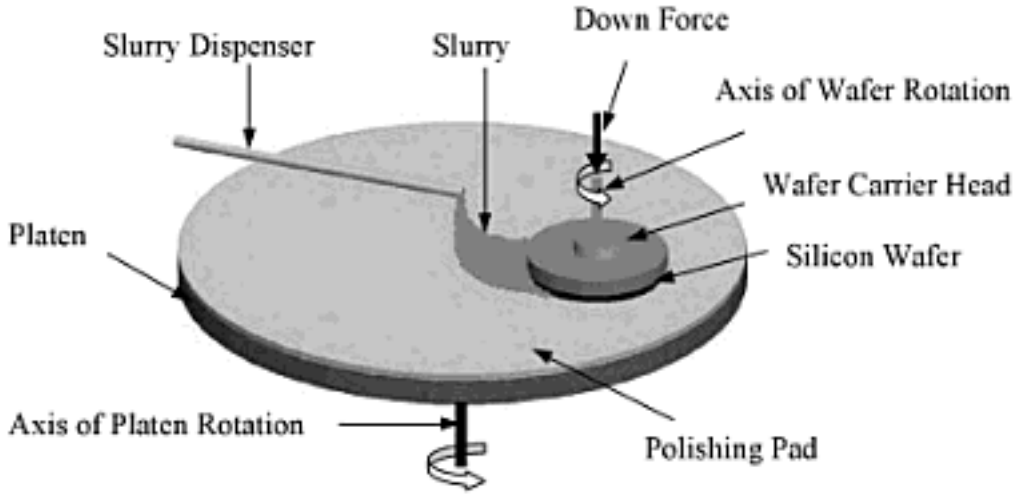
- No pixel masked
- < 20 pixels not responding



Problems are first seen going to 100 μm thinned FE-I4a.

Chemical Mechanical Process (CMP) with a maximum temperature of 35 ˚C

The wafer is mounted on a rotating carrier head and pushed against a rotating pad with a colloidal silica dispensed between the two. The colloidal silica (slurry) etches the silicon surface and polishes the wafer. The pressure between the wafer and the pad, and the rounds per minute (RPM) in which the carrier head and rotating platen spin, determine the removal rate and temperature control.

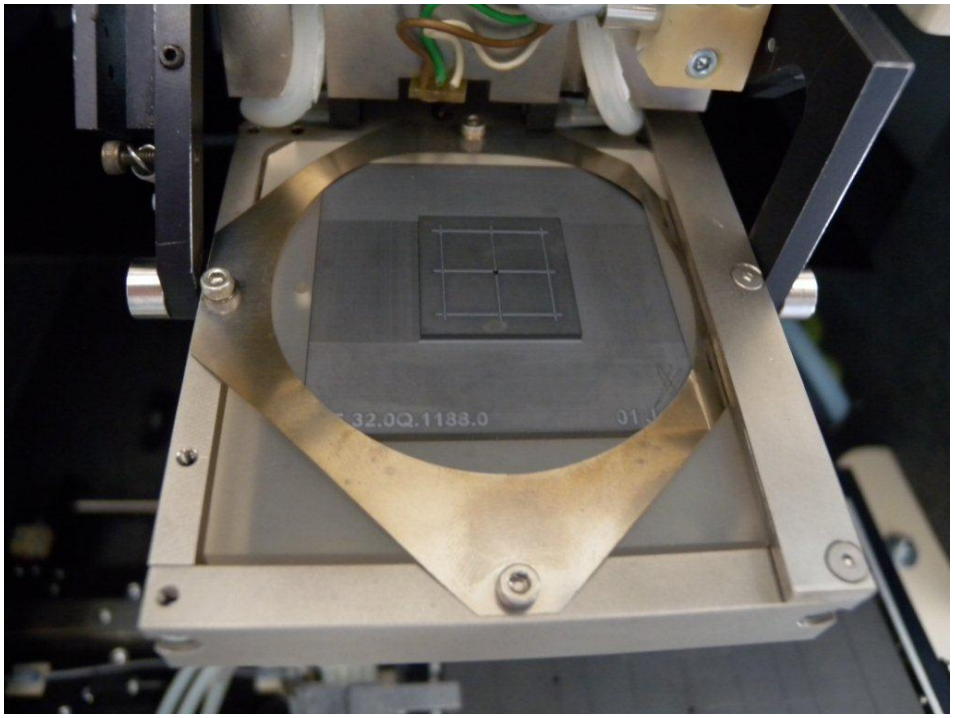


Dry polishing step, with the maximum working temperature not exceeding 90 ˚C

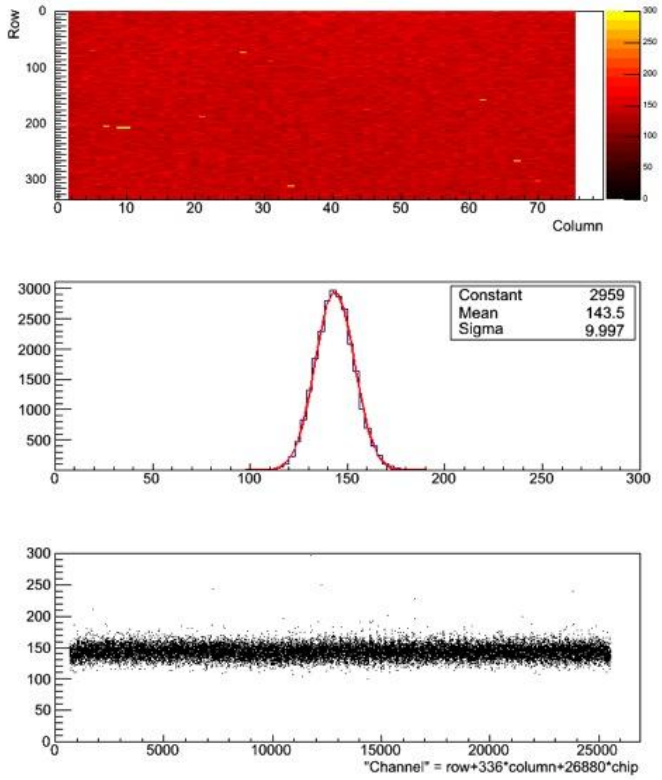
A proprietary process, a specially developed polishing wheel containing non-diamond grit, is rotating in direct contact with the wafer and uses no chemical, slurry or water.

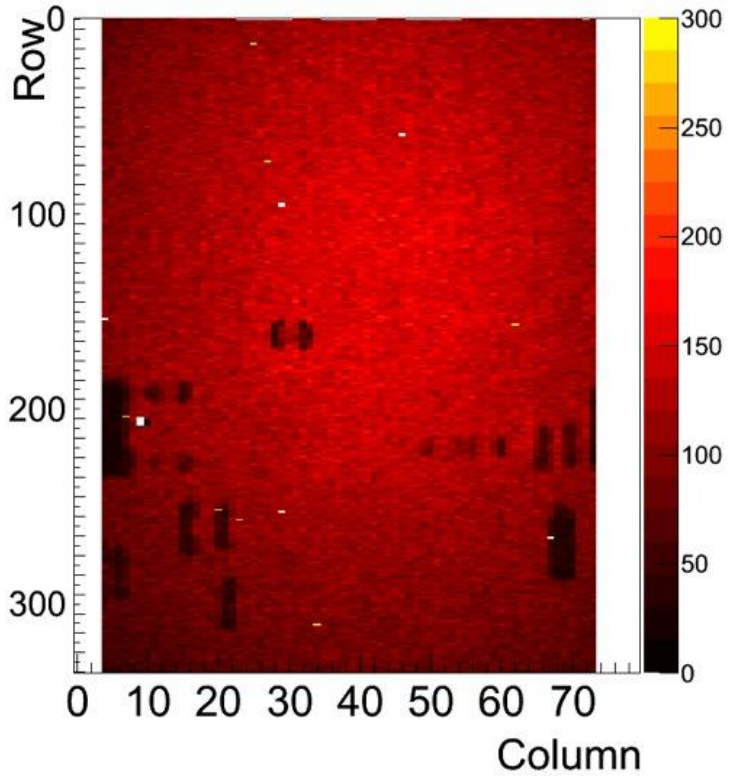
Furthermore, a modification has also been done in the bonding process: the pickup tool, by vacuum holding the thinned chip to a flat surface and applying a uniform pressure, is a natural support to flatten the deformed chip. Indium bonds at 90˚C are still very weak (indium melting temperature is 156˚C): after the flip-chip step (42 s at 90˚C), the 160N force is not immediately released but is now kept until the assembly temperature cools down to 50 ˚C.

Indium connections are then stronger and keep better in shape (flat) the bonded chip.



With these improvements results are very good for 100 μm thinned FE-I4a too, and similar to the non thinned or 200 μm thinned FE-I4a that do not require any stress relief process as shown by a planar sensor bonded to a 100 μm thick FE. Even if chips worked with the CMP process are better looking (showing a mirror like back side) than the chips worked with the polishing step, results on the modules do not show any significant difference.





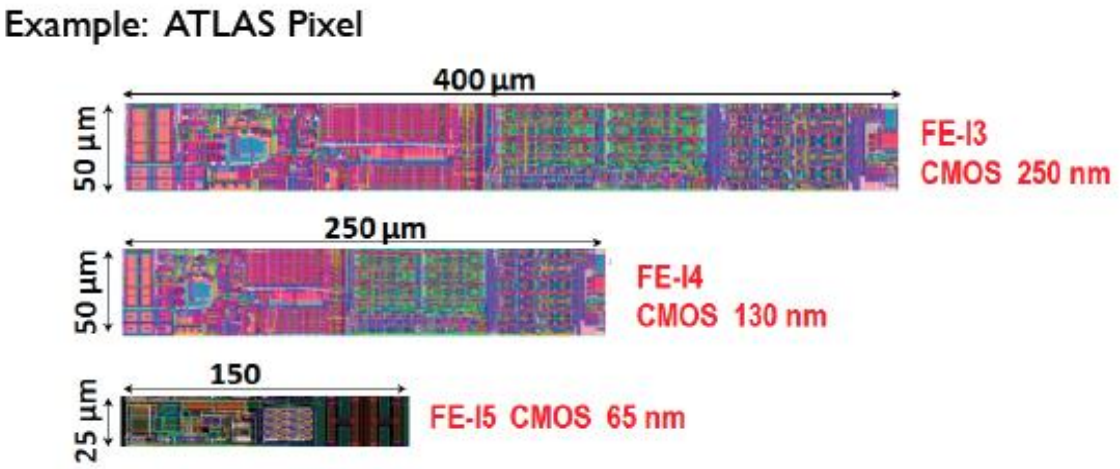
…a che punto siamo

Modules produced with 18.8 x 20.2mm^2 FE-I4 read-out chips thinned down to 100 µm have shown that the Selex indium bump bonding process can be used both with planar and 3D sensors, provided a stress relief process is applied after thinning and the flip-chip step is slightly modified allowing the working temperature to go below 50˚C before releasing the pressure.

Tests with thinner chips have not been done but there seems to be no apparent reasons that prevent working with even thinner chips.

Development of Indium bump bonding for the ATLAS Insertable B-Layer (IBL)

G Alimonti *et al* 2013 *JINST* **8** P01024 doi:10.1088/1748-0221/8/01/P01024



Cosa resta da fare?...

Certificare il bonding a 100 μm : produrre alcune decine di moduli con chip assottigliati a 100 μm sia con sensori planari che 3D.

In questa fase produrre anche moduli con 2 FE o 4FE.

R&D: verficare la lavorabilità di chip di dimensioni dei FE-I4, ma con bumpx4 (100000), con pitch minimo di 50 μm. Limiti di forza per la macchina (50Kg)?

Necessità di fare test di bonding e misure di resistenza con dummies.

Upgrade lavorazione wafer 6": prime stime di costo sui 35K Euro

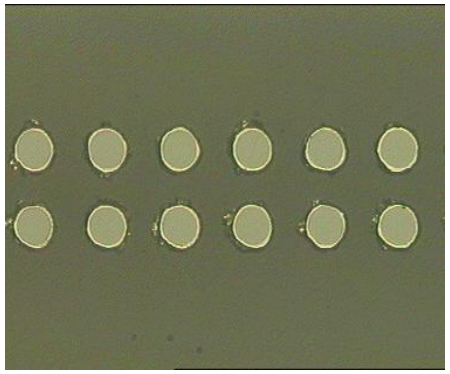
R&D: interesse a verificare la possibilità di spingersi sotto i 100 μm?

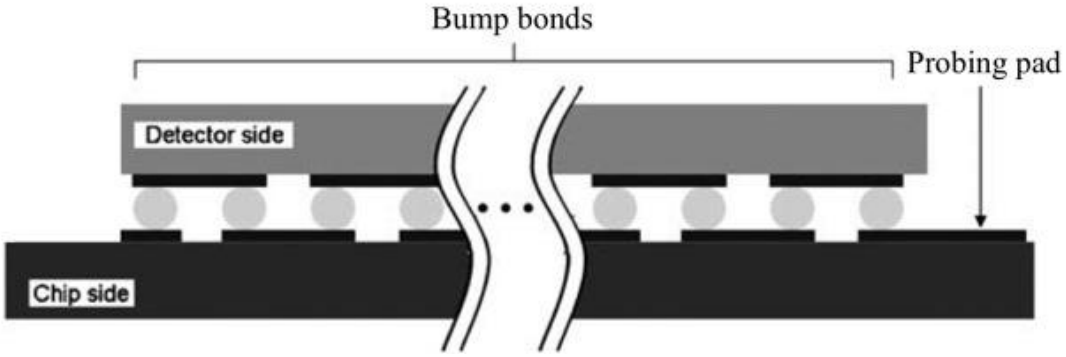
Proposta di un framework contract con Selex ove inquadrare le attività di R&D per i prossimi anni (2014-2017?)

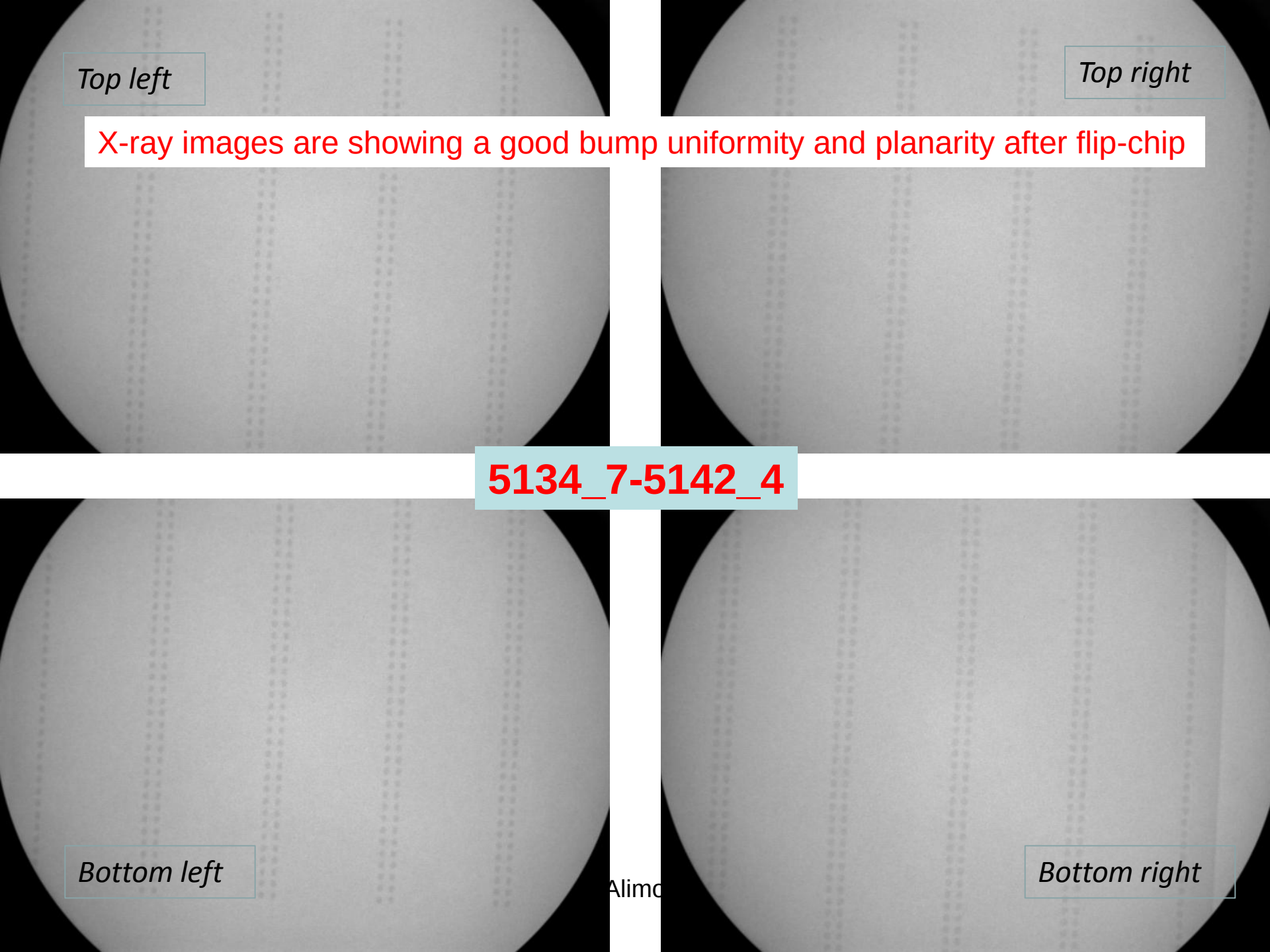
A cycle with controlled temperature and pressure allows the bumps to establish the electrical and mechanical connections. The resulting bump has an height of about 12 μm and a diameter of about 20 μm.

A custom pick-up tool for the bonding machine has been designed to match the larger size of the new modules.

The tuning of the process parameters has been performed using both glass substrates, having the same size of the dies, in order to better investigate the effects on bumps by simple inspection under optical microscope, and dummy chips. Glass substrates are also used to periodically check the flip-chip planarity and the alignment of the mating parts, monitoring the uniformity of the front-end corner bumps, which are the most sensitive to the machine settings.






Top left
Top right
X-ray images are showing a good bump uniformity and planarity after flip-chip
5134_7-5142_4
Bottom left
Bottom right