SLP2 integration at CAEN, AUX-AMBSLP, minLAMB-AMBSLP2 communications

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The basic components to test integration at CAEN are:

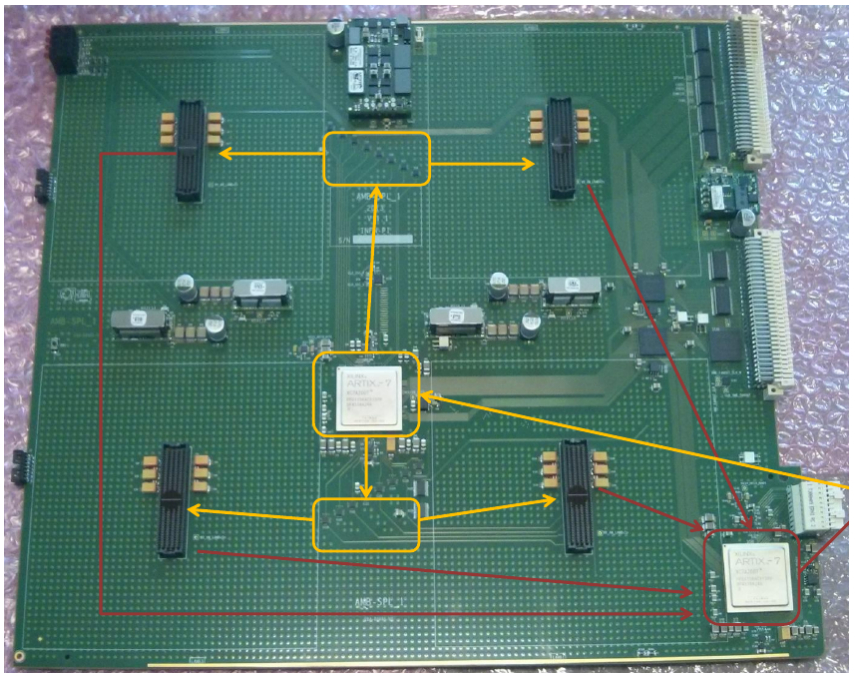
- VME 9U crate + Linux CPU with ATLAS TDAQ software
- AMBSLP2
- miniLAMB
- AUX board

A VME 9U crate is installed at CAEN in a dedicated room for FTK

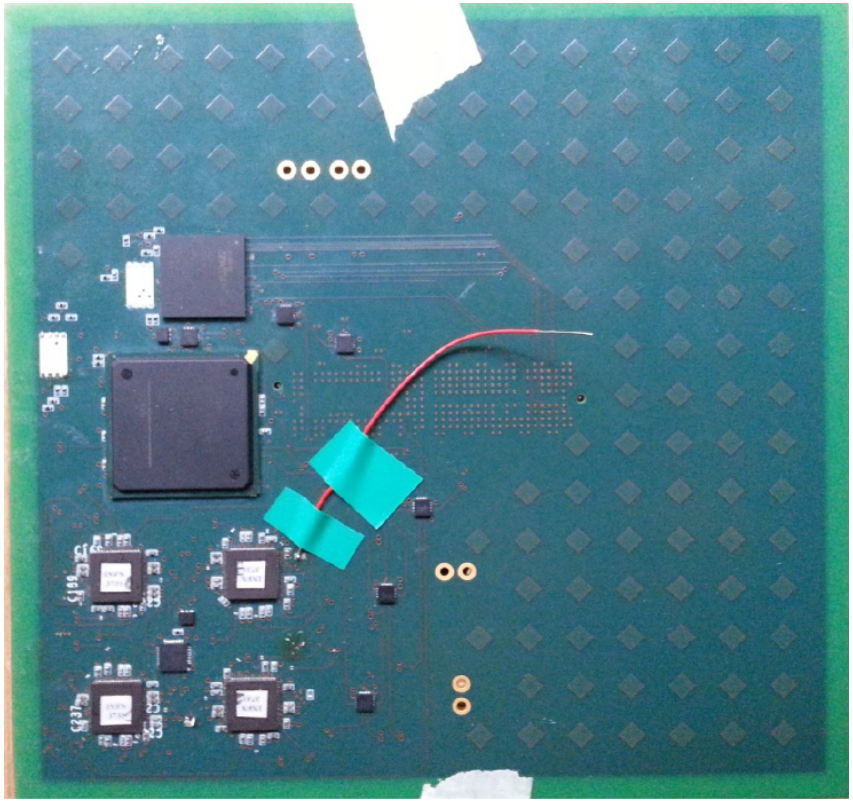
- Backplane is powered for FTK-type boards
- It's installed in an open rack for easy access to the boards for debugging purposes
- Linux CPU is now SLC6
- TDAQ-05-03-00 installed locally
- No need of fast internet connection to be used

The AMBSLP2 is a major component of the FTK Processing Unit (PU). It hosts the Associative Memory mezzanines (LAMB) and communicates thru a backplane connector with the AUX board.

- 12 input buses @ 24 Gbps
- 16 output buses @ 32 Gbps
- ARTIX-7 FPGA for input distribution
- ARTIX-7 FPGA for output distribution
- SPARTAN-6 FPGA for data control logic



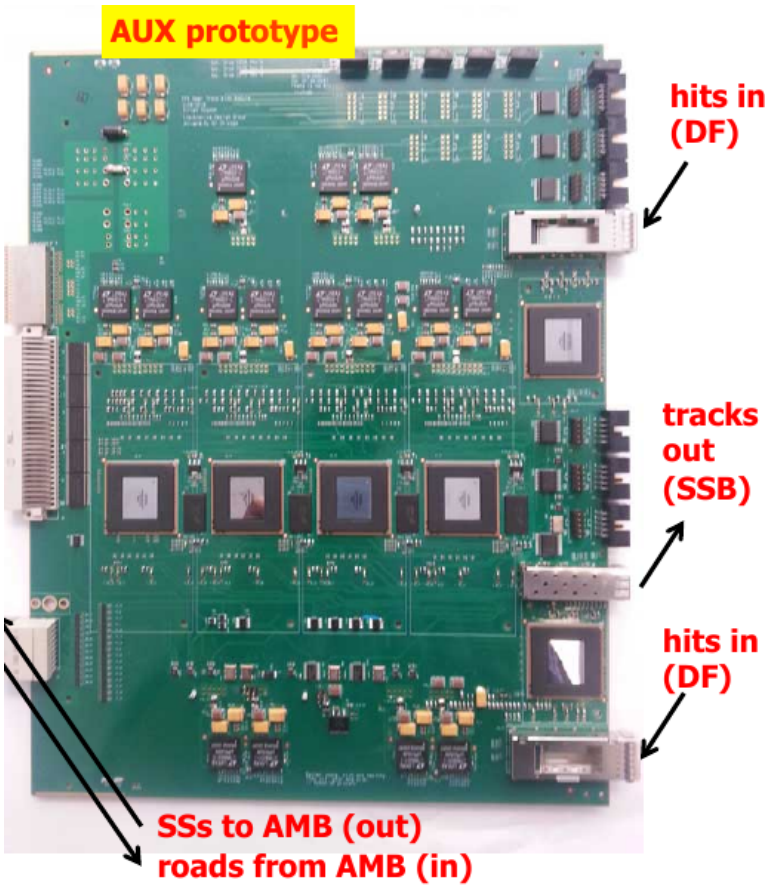
The miniLAMB is a LAMB-compatible board to test AMBSLP2-LAMB connections and functionalities.



- Chain of 4 miniasic AMchip connected to 4 serial inputs and 1 serial output
- SPARTAN-6 to test high speed serial links connected to the remaining 4 serial inputs and 3 serial outputs
- SPARTAN-6 to handle JTAG configuration of AMchips

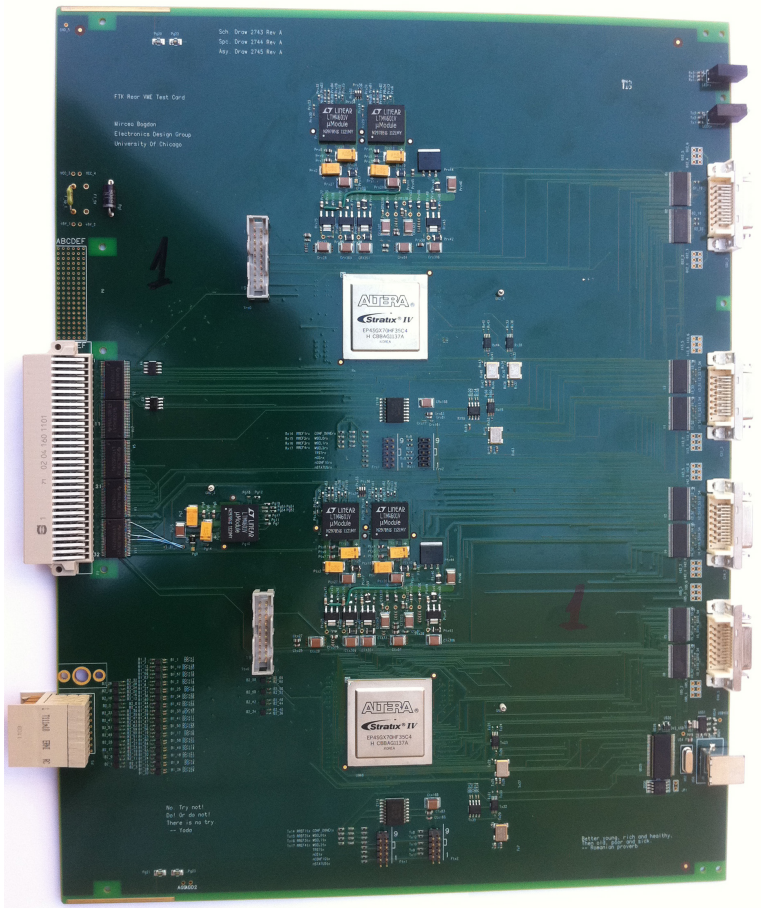
The AUX board receive data from the Data Formatter through fiber optic links, process it and then send hits / receive roads through the high speed serial links on the backplan to the AMBSLP2. It hosts the FPGAs for Data Organizer, Track Fitter and Hit Warrior functions.

- 2 ARIA-V FPGA for I/O with Data Formatter crates
- 4 ARIA-V FPGA for data processing and AMBSLP2 communication

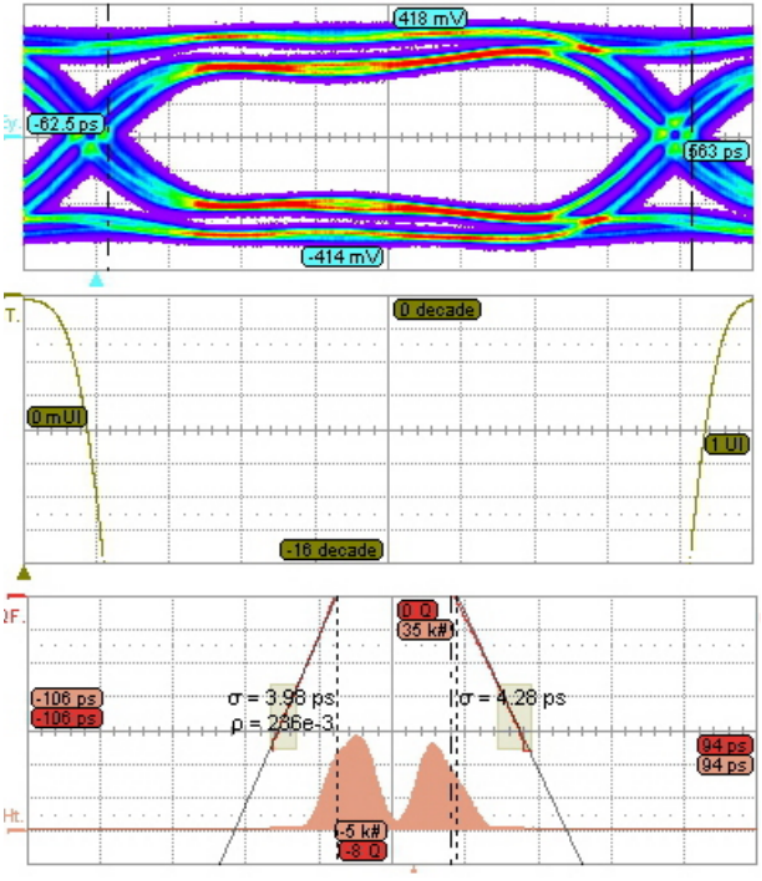


An AUX-compatible card was developed by University of Chicago specifically to test high speed serial links. This card is available in Italy, the AUX card is at CERN.

- 2 STRATIX-IV FPGA for serial link tests
- mechanics and backplane connectivity identical to AUX



Integration tests were performed to check the quality of the serial links



- AUX $\rightarrow$ AMBSLP2 with BER < 10^{-15}
- AUX $\leftarrow$ AMBSLP2 tests with new firmware are under way in CERN Lab 4
- AMBSLP2 $\leftrightarrow$ AMBSLP2 with BER < 10^{-14} (presented at TIPP 2014 by P. Luciano)

- All components needed for integration tests are available and in working order:
  - VME crate at CAEN is OK
  - AMBSLP2, AUX and miniLAMB are available and can communicate
- LAMB mezzanine with AMchip05 will be available soon
  - Once tests with this LAMB are completed we can declare M.2.2 done
  - D.2.5 should be a pubblication about this integration