Activity in Paris - WP6

A few words on myself

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- I am a physicist with good experience of Silicon Detectors and Digital Electronic design. In the past worked on ATLAS Pixel Detector designing the Module Controller Chip (MCC), participated to the FE-I4 design and to the integration and commissioning of the present ATLAS Pixel Detector.
- I also work on development and testing of the ATLAS AMChip for the FTK project.
- For INFN i am coordinating the Digital Design WG of ChiPix65, an italian project devoted to Pixel Chip design in TSMC 65nm technology.
- I am also coordinating the I/O WP of CERN's RD53 project.
- I am an INFN - Pisa employee, currently detached at LPNHE in Paris.

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WP6: Scope

Prototypes of a chip in 65nm CMOS process are being developed for the readout chip, to increase the component density of the readout chip and to allow a further reduction of the sensor pixel size. In all this, the power dissipation will play an important role and the high voltage distribution system will be one of the key ingredients in the evolution of the detector design.

Keep the FTK collaboration, in particular CAEN, in contact with the detector R&D evolution, that will be important in all the years of our project, given the fact that this detectors are studied for LHC Phase II, scheduled after 2020.

Participate to the pixel R&D and the running of the FTK test stand that will be installed at CNRS to allow firmware and test developments in Paris.

This WP has a reduced role compared to the electronics tasks, however it provides a solid link with the evolution of the on-going R&D for the silicon sensors and the front-end readout electronics in view of the high luminosity upgrade of the LHC.

This link is important for FTK since a constant dependence connects the evolving features of the future tracker (segmentation, geometry, expected hit efficiency, noise, readout speed) with the future of the FTK architecture.

IAPP and RD53 connections

Recently CERN started a new collaboration (RD53) that involves almost all HEP electronic designers.

Scope of the collaboration is to exploit the feasibility of a new FE chip, developed in 65nm (or lower) technology providing a full scale prototype in ~ 3 years:

1. 1Grad + 10^{16} n/cm^2: a new frontier for radiation effects in CMOS.
2. Development of tools expertise amongst the community.
3. Meet both ATLAS and CMS detector requirements for PhaseII.
4. High speed Serial Output links (2GB/s).
5. Off chip connectivity: Calculation, Simulation and Test of transmission performance with realistic interconnects.
6. Development of a specification for the system and a test setup.

Therefore there are many interconnections between WP6 and RD53.

My participation to RD53 is in the interest of IAPP, in order to exploit and strengthen those connections that are crucial for the project.

RD53 I/O WG: Main tasks

I am the convener of the I/O WG inside RD53. Main tasks of this WG are:

1. I/O: Evaluation and definition of I/O protocols supporting 2Gbps or higher serial links, command based triggering up to 1MHz rate and minimum dead-time.

   - 80Mbps or higher serial input, with command decoder to configure and operate the chip. Evaluation of a slow control protocol.
     Command and Clock should be encoded on a single line.

   - 2Gbps Serial Output links will require to evaluate different output data formats and compression alternatives.

   - A duplex solution where all I/O takes place on a single serial connection should be considered. Investigation of link redundancy schemes to be eventually used on less data demanding layers.

2. Interfaces: Evaluation of compatibility with defined interfaces such as LPGBT.

3. IP blocks related to I/O: interface driver, clock recovery, clock multiplier methods, LVDS driver and receivers. [Work to be shared with the IP group]

4. Off chip connectivity: Calculation, Simulation and Test of transmission performance with realistic interconnects. I/O should not stop at the chip pads but extend to the system immediately outside the chip. High speed cables and protocols and even test interfaces. Therefore the WG should develop a specification for the system around it and a test setup.