CLIC vertex detector R&D

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On behalf of the CLICdp collaboration

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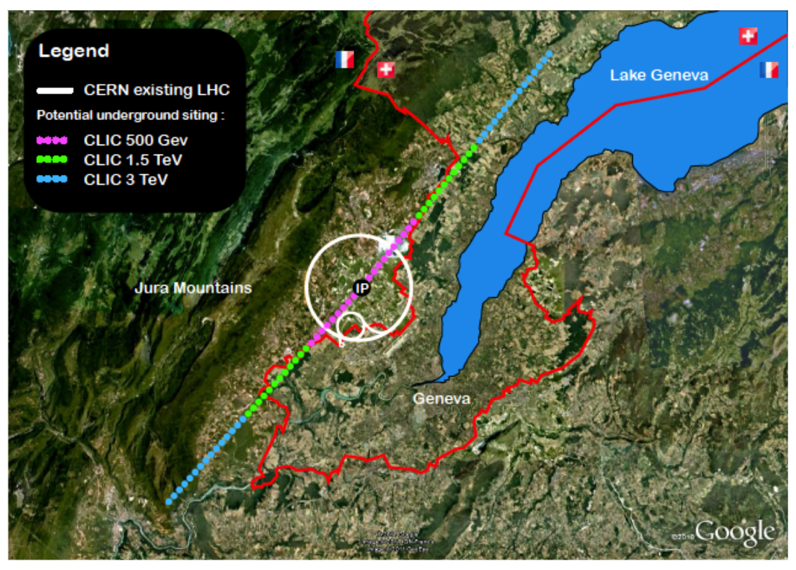
http://clicdp.web.cern.ch/

CLIC: the Compact Linear Collider

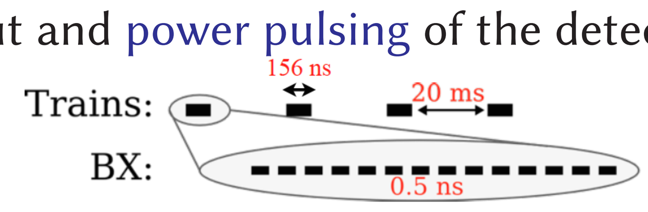
- Concept for a future e^+e^- linear collider
- Staged construction & operation:
  1. $\sqrt{s}$=350 GeV: Higgs, top physics inc. threshold
  2. $\sqrt{s}$=1.4 TeV: Higher precision Higgs, top Yukawa coupling, first BSM searches
  3. $\sqrt{s}$=3 TeV: double Higgs production, high sensitivity direct and indirect BSM
- Instantaneous luminosity at 3 TeV:
  - $\mathcal{L}$ =6 × 10^{34} cm^{-2} s^{-1}
- A possible realisation close to CERN:
  - Maximum length: ~50 km



CLIC detector concept

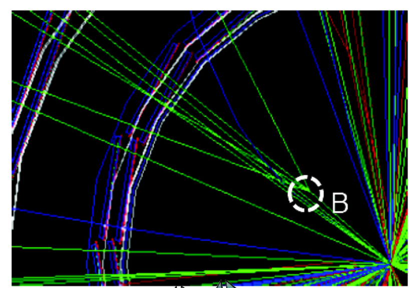
Beam structure allows for triggerless readout and power pulsing of the detectors:

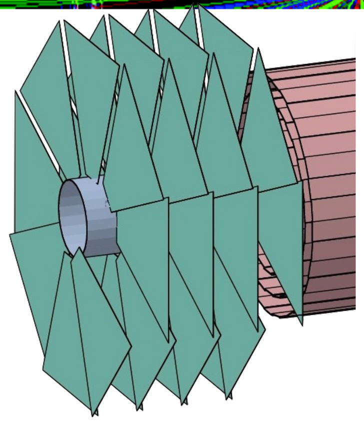
- 312 bunches per train of 156 ns
- Train repetition: 20 ms

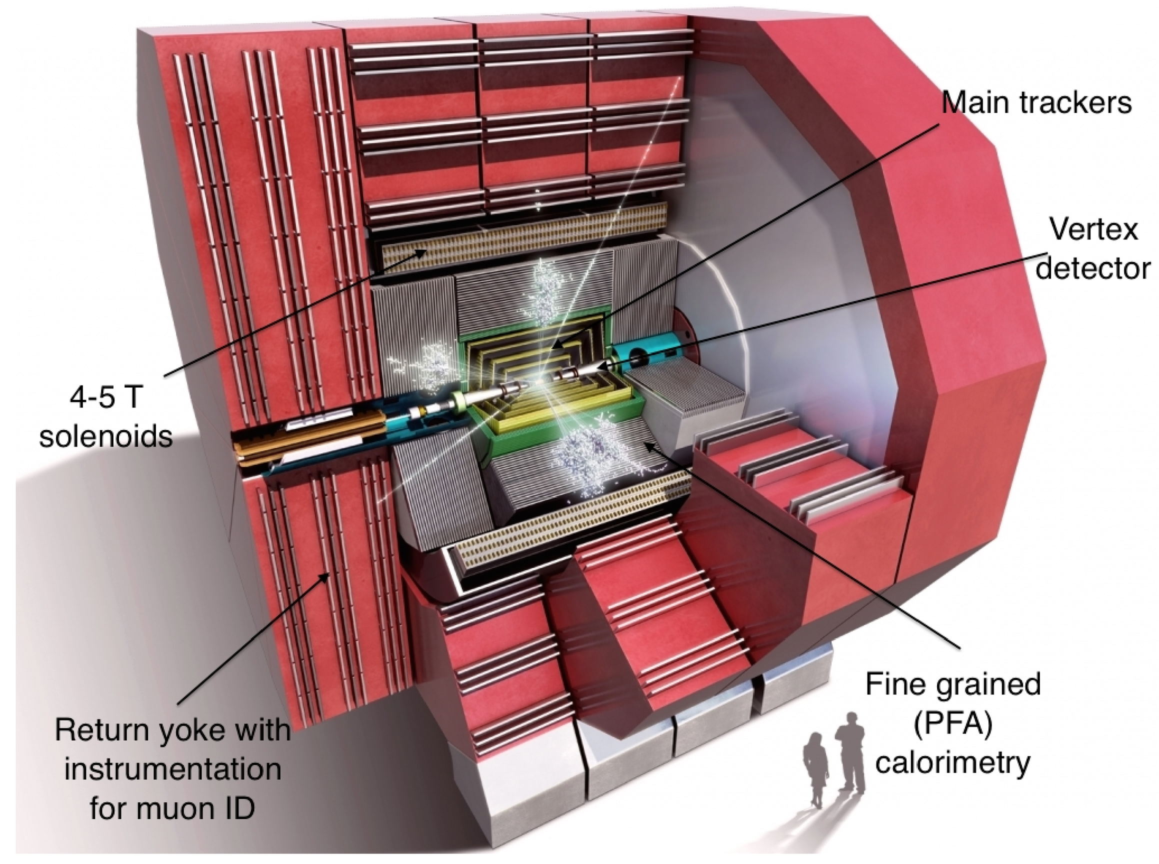


Vertex detector requirements

- Aim: efficient identification of heavy quarks in high occupancy.
- Multi-layer barrel and endcap pixel detectors.
- Goal for the pixel detectors: achieve a single point resolution of ~3 µm with 25 µm pixel pitch & analog readout.
- Time slicing of ~ 10 ns allows to reduce the impact of beam-induced backgrounds.
- Material budget of < 0.2% X_0 per layer implies:
  - 50 µm sensor on 50 µm ASIC.
  - Limit the power dissipation to 50 mW cm^{-2} in sensor area:
    ⇒ power pulsing
    ⇒ air-flow cooling: spiral arrangement of the modules in the vertex endcap regions



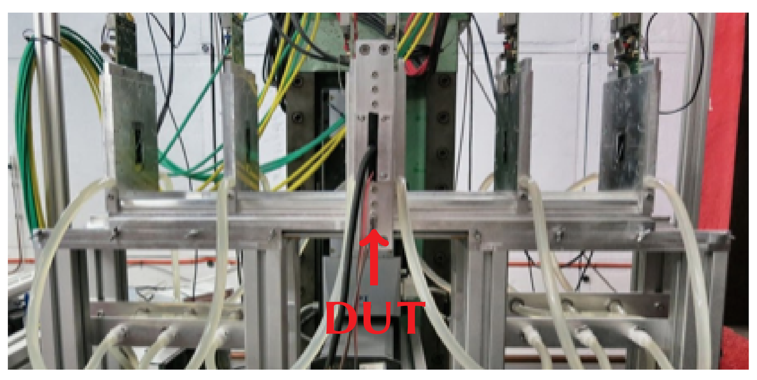




R&D on sensor and readout

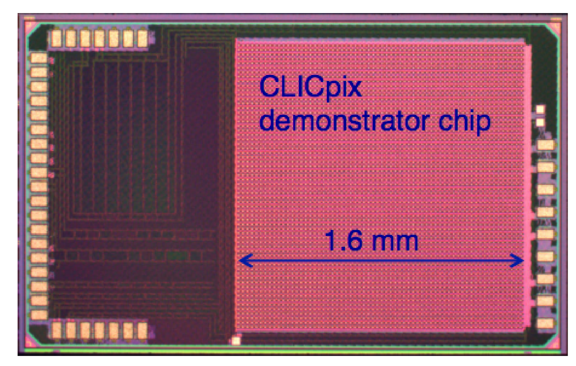
Test-beam campaigns

- Data recorded using the EUDET/AIDA telescope at:
  - DESY II: 5.6 GeV electron beam
  - CERN PS: 10 GeV mixed beam
  - CERN SPS: 120 GeV pion beam
- The telescope contains 6 planes of Mimosa26 pixel sensors with a tracking resolution of ~3 µm for 5.6 GeV electron beam.



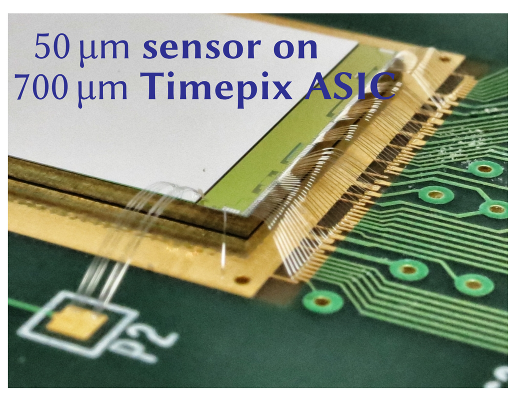
CLICpix readout chip demonstrator

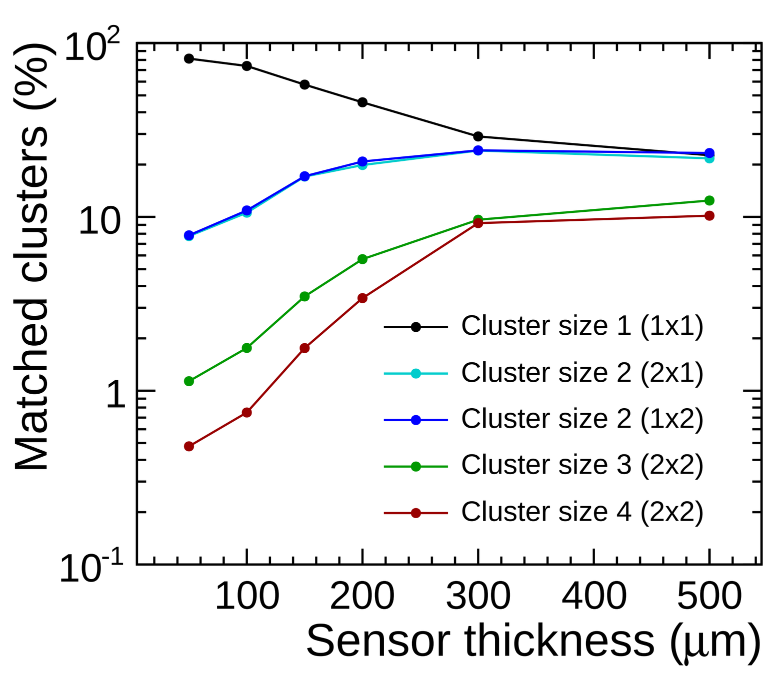
- ASIC in 65 nm CMOS technology.
- Matrix of 64 × 64 pixels, 25 µm pixel pitch.
- Simultaneous measurement of time of arrival (TOA) and time over threshold (TOT) per pixel.
- Compatible with power pulsing scheme.
- Selectable compression logic.

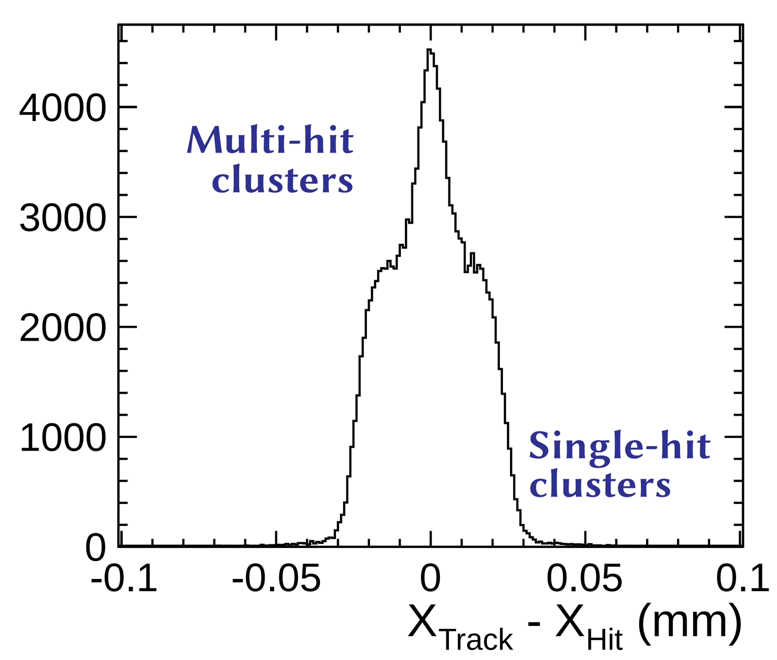


Planar sensors

- The feasibility of thin sensors is studied using the Timepix ASIC with 55 µm pixel pitch.
- 50 µm to 500 µm thick sensors are bump-bonded to 100 µm to 750 µm thick Timepix ASICs.
- Overall detection efficiency > 99%.
- Charge sharing and hit resolution depend on sensor thickness:
  - ~4 µm resolution achievable for 2-hit clusters (including the tracking resolution).
  - For single-hit clusters, the resolution is determined by the pixel size.

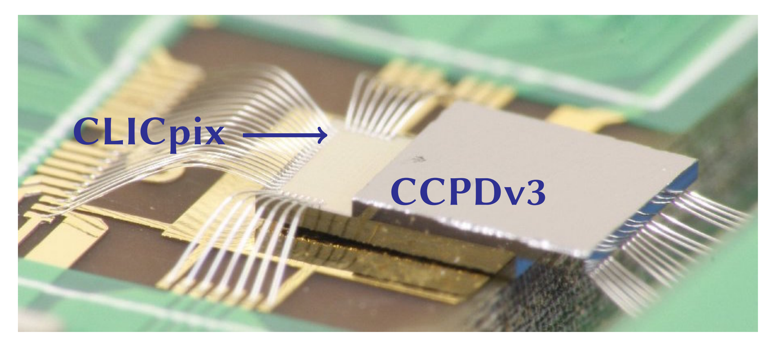


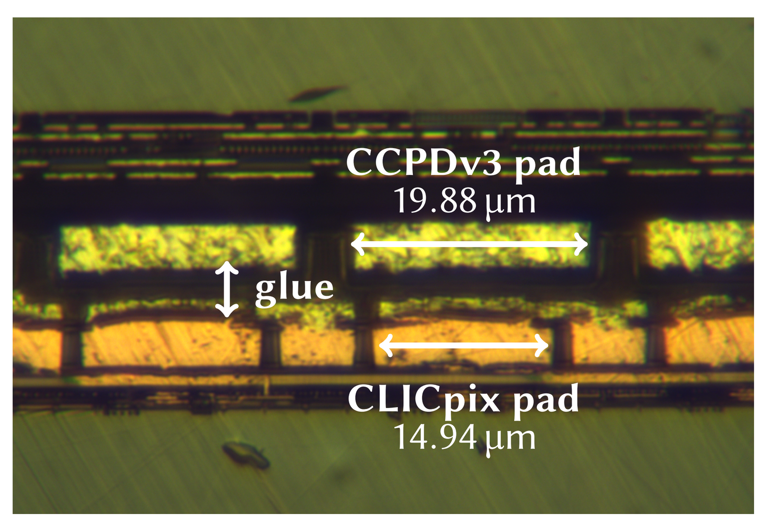


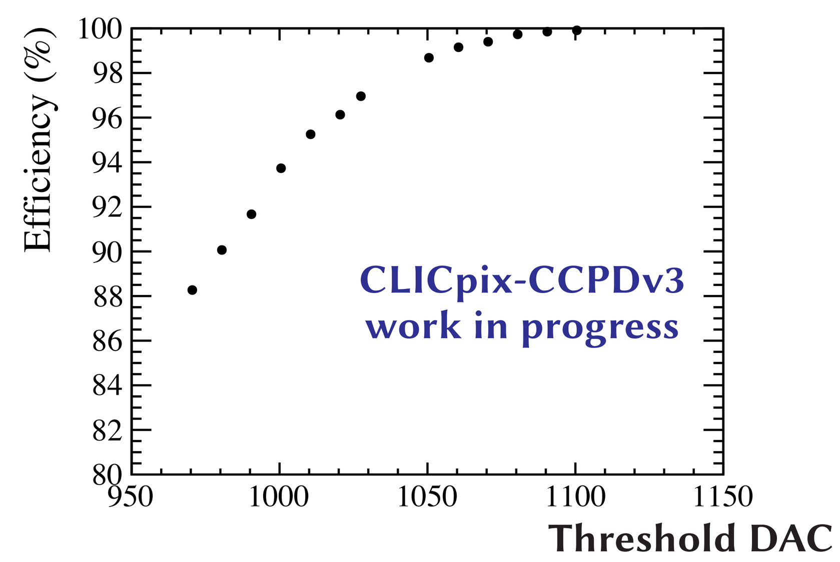


Active HV-CMOS sensors

- Capacitively coupled pixel detector (CCPDv3) is used as active sensor ⇒ integrates sensor and amplifier.
- Two-stage amplifier in each pixel.
- Through a layer of glue, the CCPDv3 chip is capacitively coupled from its amplifier output to the CLICpix readout ASIC ⇒ no bump-bonding.
- CCPDv3 is implemented in 180 nm HV-CMOS process and biased at 60 V ⇒ create a depletion layer with fast signal collection through drift.
- High single-hit detection efficiency (high threshold DAC corresponds to low threshold as the chip is operated in negative polarity):



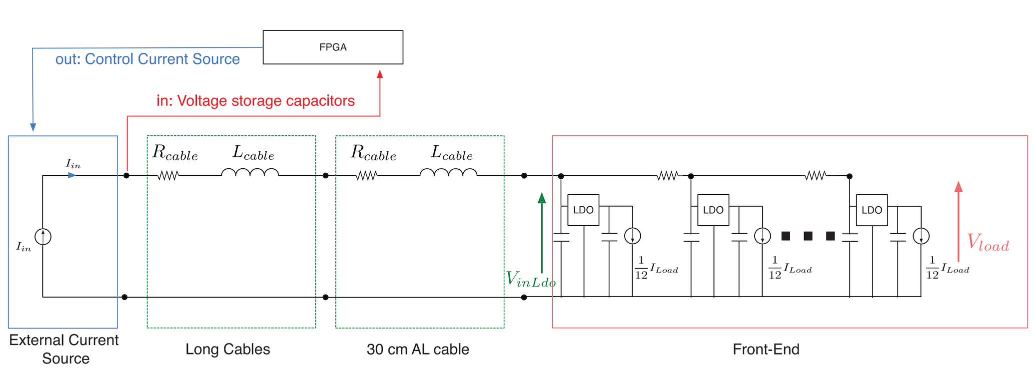


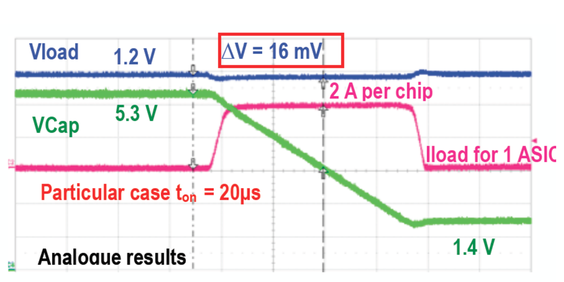


Power pulsing

Power-delivery and power-pulsing design for low-mass vertex detector:

- Turn off the front-end in gaps between bunch trains to reduce average power in ASIC.
- Local energy storage in Silicon capacitors and voltage regulation with low-dropout (LDO) regulators.
- FPGA-controlled current source provides small continuous current.
- Low-mass all-Kapton cables.
- Prototype built and tested: I_{ladder}=300 mA, P<45 mW cm^{-2}.





Air-flow cooling

Forced air-flow is foreseen for the heat removal of the vertex detector.

- Total heat load after power-pulsing: ~500 W
- Dry air flows through the barrel and the endcap regions.
- Thermal mockup built for vertex barrel and endcap regions:
  - Confirms the air-flow through the barrel and the endcap regions.
  - Temperature increase: ~10 °C to 35 °C