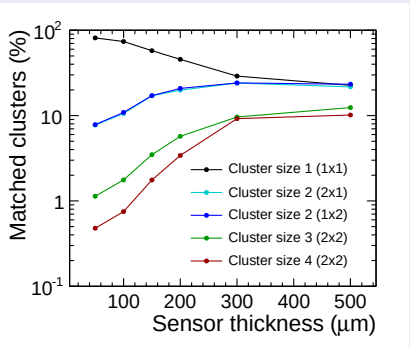
CLIC vertex detector R&D: sensor and readout

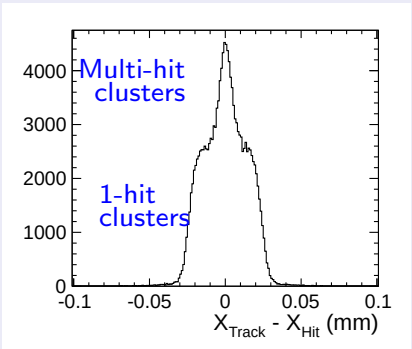
Requirements:

- Single point resolution of $\sim$3 µm: 25 µm pixel pitch & analog readout.
- Time slicing of $\sim$ 10 ns to reduce the impact of beam-induced backgrounds.
- Material budget of $< 0.2\% X_0$ per layer $\Rightarrow$ 50 µm sensor on 50 µm ASIC.

Planar sensors

- The feasibility of thin sensors (50 µm to 500 µm thick) is studied with Timepix ASIC (55 µm pixel pitch).

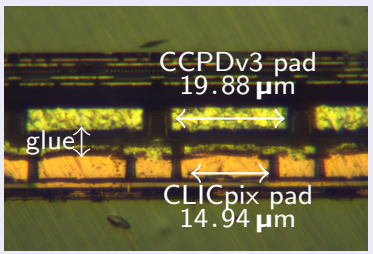


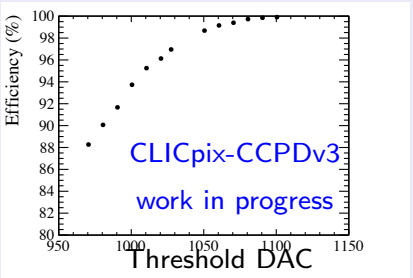


- $\sim$4 µm resolution achievable for 2-hit clusters (including the tracking resolution).

Active HV-CMOS sensors

- Capacitively coupled pixel detector (CCPDv3) is used as active sensor $\Rightarrow$ integrates sensor and amplifier.
- Through a layer of glue, the CCPDv3 chip is capacitively coupled from its amplifier output to the CLICpix readout ASIC $\Rightarrow$ no bump-bonding.





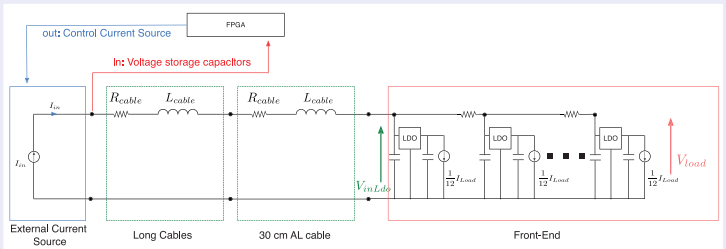
CLIC vertex detector R&D: powering and cooling

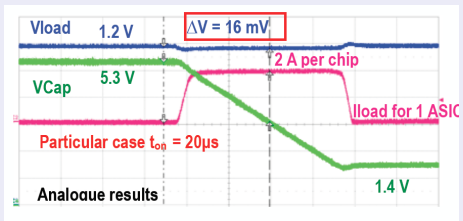
- Beam structure at CLIC allows for triggerless readout and power pulsing of the detectors.

Power pulsing

Power-delivery and power-pulsing design for low-mass vertex detector:

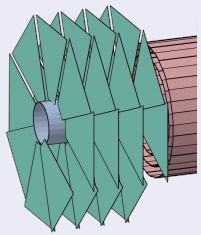
- Turn off the analog front-end of the readout chip in between bunch trains.
- Prototype built and tested: I_{ladder}=300 mA, P<45 mW cm^{-2}.





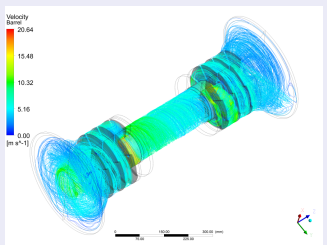
Airflow cooling

- To limit the material, no active elements can be used for cooling.



- Dry air flows through the barrel and the endcap regions ⇒ spiral geometry for the endcap regions.
- Total heat load after power-pulsing: ∼500 W

- Airflow streamlines.



- Thermal mockup.