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L1Track: a fast Level 1 track trigger for the ATLAS High Luminosity Upgrade

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With the planned high-luminosity upgrade of the LHC, the ATLAS detector will see its collision rate increase by approximately a factor of 5 with respect to the current LHC design. Due to this the pile-up collisions will increase by a similar factor.
The earliest hardware based ATLAS trigger stage (”Level 1”) will have to provide an higher rejection factor in a more difficult environment. The Level 1 trigger architecture needs therefore to be improved. A new Level 1 trigger architecture is under study, which, in addition of the “regions of interest”identified by the calorimetry and the muon chambers, also includes the possibility of extracting tracking information and use it for the decision taking process. The expected trigger rates at HL-LHC and the available latency are the key ingredients that will drive the new design.
A low-latency and accurate tracking trigger system is being developed in the context of this additional trigger refinement. The design results in a substantial modification of the ATLAS silicon detector readout philosophy: a precursor of the potential merging of detector and trigger architectures in the future silicon detectors at particle colliders.
In this context, we will discuss and review the design alternatives and potential approaches that are being actively considered to fulfill such demanding constraints and deliver tracks of quality sufficient to maintain trigger rejection power with a very limited time budget.

Collaboration

ATLAS Collaboration

Primary authors: Dr BOLD, Tomasz (AGH-UST); Dr CERRI, alessandro (LBNL); Ms PASTORE, francesca (CERN)

Presenter: Dr CERRI, alessandro (LBNL)

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