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Characterization of Depleted Monolithic Active Pixel Detectors with High-Resistive CMOS Technology

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We present the recent development of Depleted Monolithic Active Pixel Sensors (DMAPS), implemented with a Toshiba 130-nm CMOS process. Recent progress in CMOS technology enables to utilize a high-resistive silicon substrate as a charge sensitive layer and to fabricate CMOS electronics inside of nested-wells in the same substrate. Such technology offers truly monolithic devices as an alternative to hybrid detectors or charge coupled devices, and, hence, possibility of DMAPS with various technology is currently under intensive study. Compared to the conventional epi layer-based MAPS, DMAPS have several merits as charge-measurement detectors: since the substrate can be operated as a fully depleted bulk, the charge collection becomes faster and larger signal is available for signal processing. As a result, the radiation tolerance is expected to be much higher than the conventional MAPS detectors. In order to characterize the technology, we implemented a simple three transistor readout with a variety of collection electrode's layouts. This layout variety gives us a clue on sensor characteristics for future optimization, such as the input detector capacitance or leakage current.

In the presentation, we will show initial measurement results on the sensor and discuss the future perspective by comparing other DMAPS implementation based on different CMOS technologies.

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