# Characterization of Depleted Monolithic Active Pixel Detectors with High-Resistive CMOS Technology

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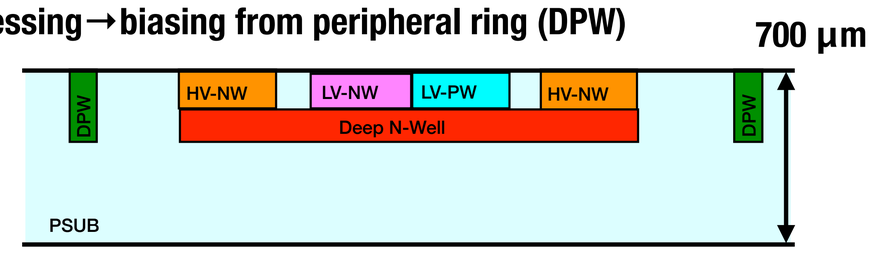
## 1. Motivation & Technological overview

Recent progress in CMOS technology enables to utilize a high-resistive silicon substrate as a charge sensitive layer and to fabricate CMOS electronics inside of nested-wells in the same substate. Such technology offers truly monolithic devices as an alternative to hybrid detectors or charge coupled devices, and, hence, possibility of DMAPS (Depleted Monolithic Active Pixel Sensor) with various technology is currently under intensive study.

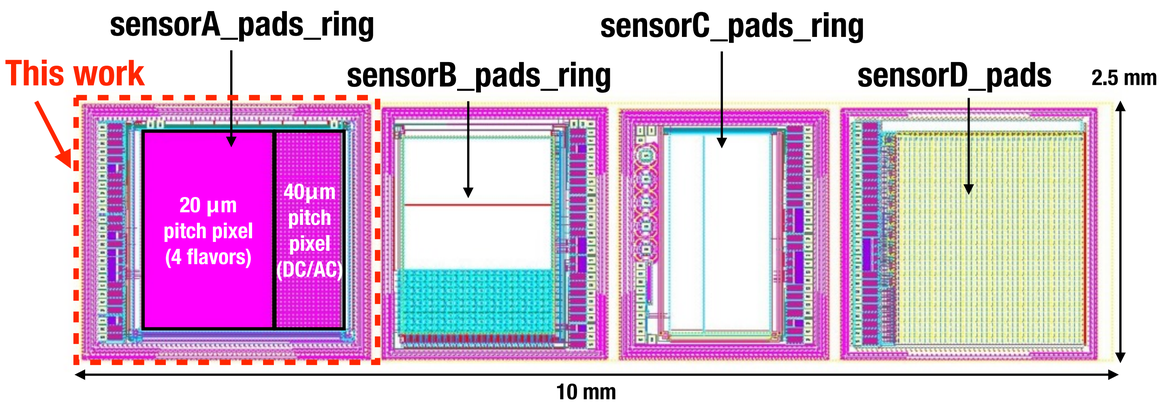
**Toshiba 130 nm CMOS process**

**-1.5 V core, 5 metals, high-R. p-substrate (~2 kΩ•cm)**
**-w/o backside processing→biasing from peripheral ring (DPW)**



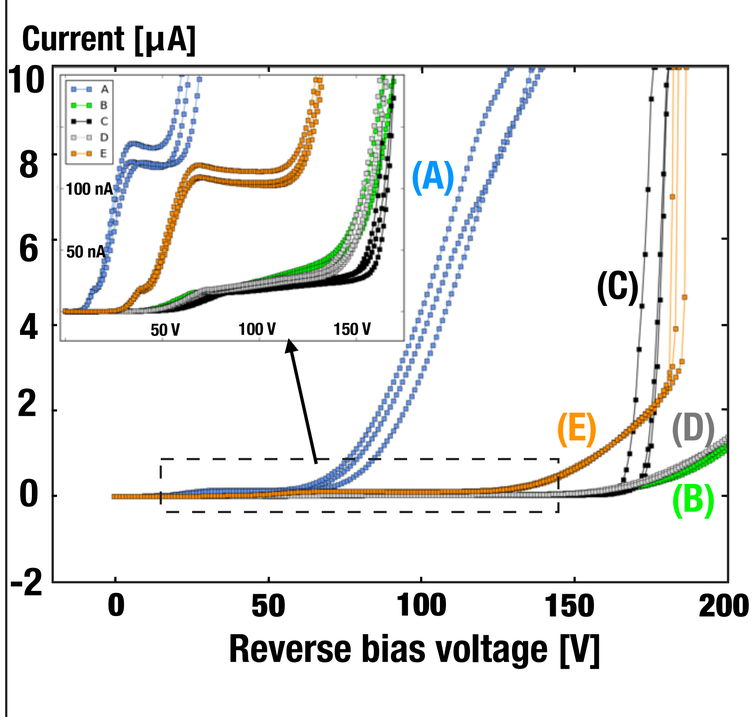

In order to characterize the technology, we implemented a simple three transistor (3T) readout with a variety of collection electrode's layouts and pixel pitches as shown below.

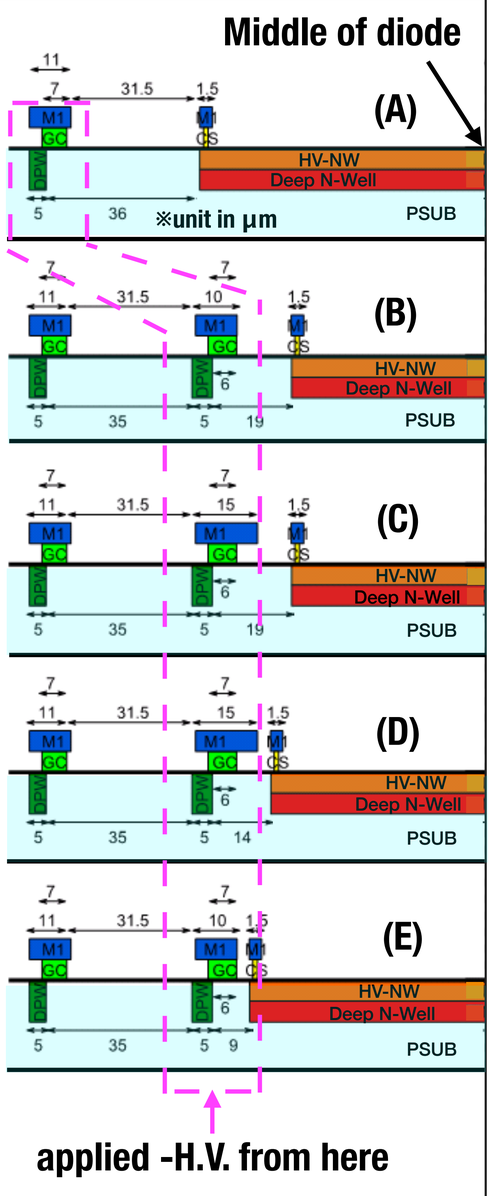
**Layout of the prototype chip**




## 2. Simple diode characteristics

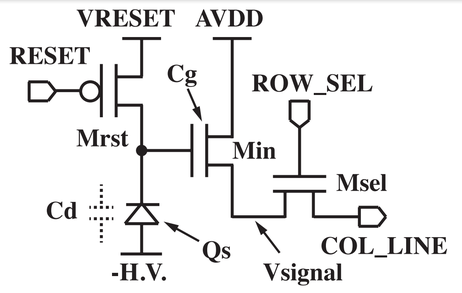
The diode breakdown voltage strongly depends on the bias ring structures, such as distance between DPW and DNW, and also metal overhang. The measurement shows that, depending on the diode and guard-ring layout, up to 200 V can be applied at room temperature.



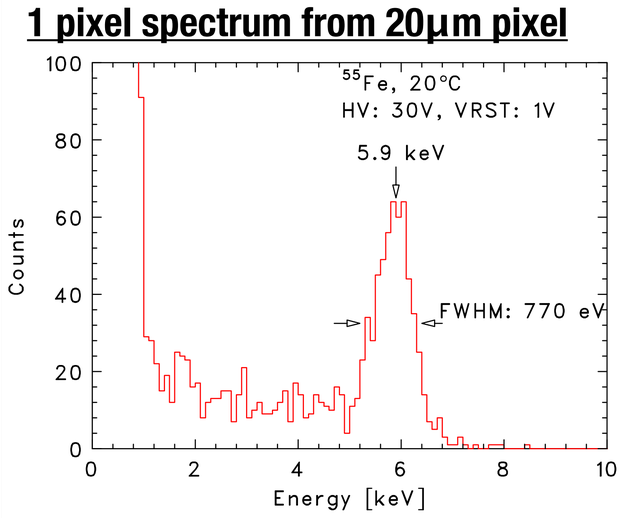

## 3. Input capacitance measurements

The input sensor capacitance was estimated with 3T readout scheme and $^{55}$Fe 5.9 keV peak. Three matrices with different DNW layout and input FET are implemented in 20 $\mu$m pixels. We also implemented metal-metal capacitance for an AC-coupling with 40 $\mu$m pixels.

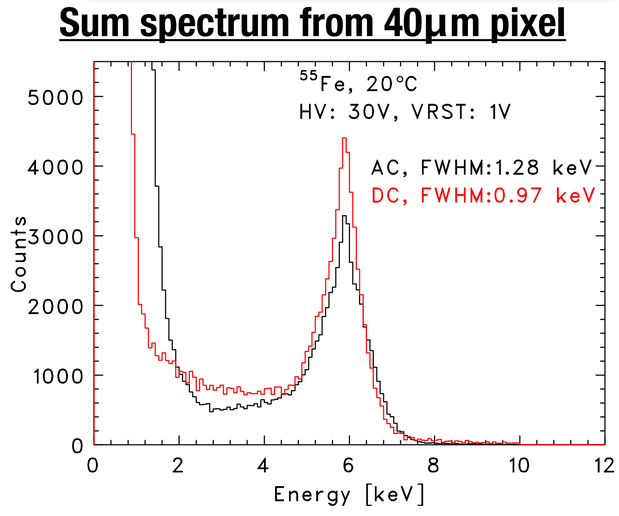



$$V_{\mathrm{signal}} = \frac{Q_{\mathrm{s}}}{C_{\mathrm{d}} + C_{\mathrm{g}}} \times \mathrm{S.F.\ gain} \equiv \frac{Q_{\mathrm{s}}}{C_{\mathrm{in}}}$$

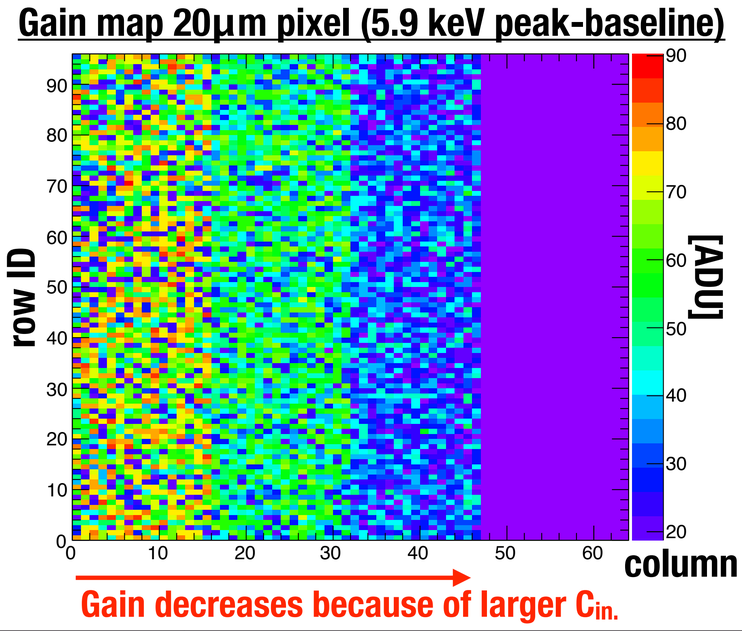
**1 pixel spectrum from 20µm pixel**



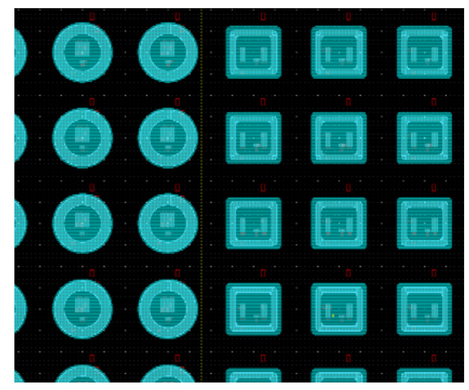

**Sum spectrum from 40µm pixel**




**Gain map 20µm pixel (5.9 keV peak-baseline)**




**Layout example of DNW layer**

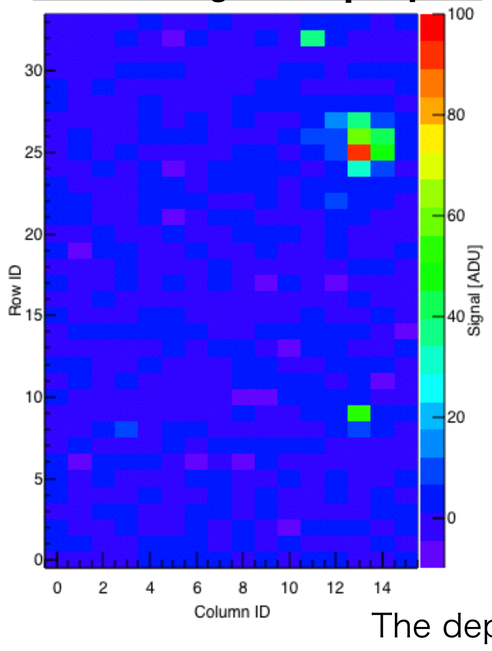


| pixel pitch | coupling | Size of input FET | Diode shape | C |
|---|---|---|---|---|
| 20 µm | DC | Lmin. | round | 31.2 fF |
| 20 µm | DC | 2×Lmin. | round | 38.9 fF |
| 20 µm | DC | Lmin. | square | 61.5 fF |
| 40 µm | DC | Lmin. | round | 81.2 fF |
| 40 µm | AC | Lmin. | round | 51.0 fF |

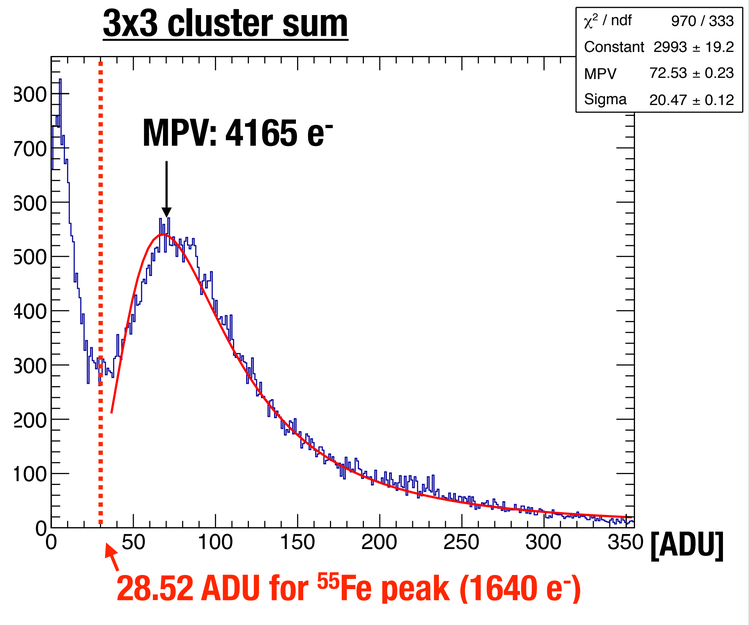
## 4. Irradiation tests with $^{90}$Sr

We used a $^{90}$Sr source with the matrices and successfully demonstrated the DMAPS working as a charged particle detector. The Landau distribution is clearly seen after extracting cluster events from the image.

**Cluster image of 40 µm pixel**




**3x3 cluster sum**




The depletion thickness can be estimated as ~50 um.

## 5. Summary

We presented the recent development of DMAPS with a Toshiba 130-nm CMOS process. The layout variety gives us a clue on sensor characteristics for future optimization. We are currently planning of backside processing and radiation tests.

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