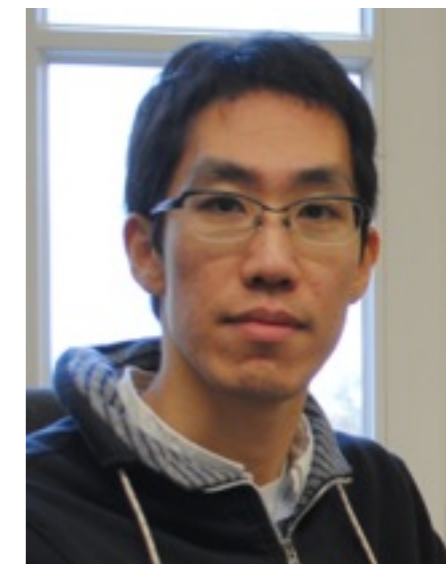


Characterization of Depleted Monolithic Active Pixel Detectors with High-Resistive CMOS Technology

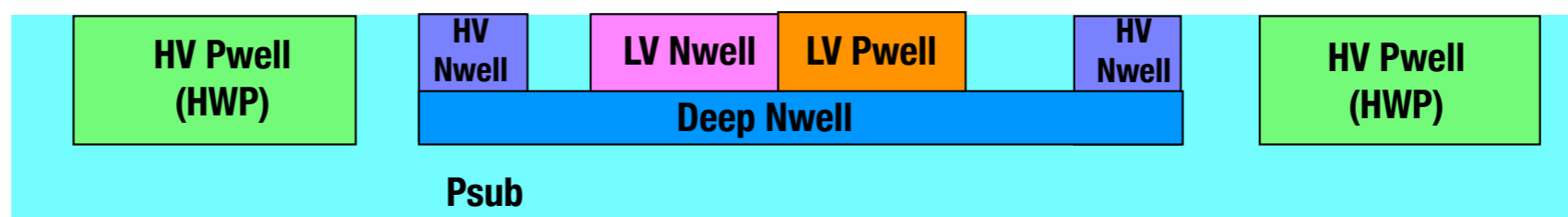
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T. Hemperek, P. Rymaszewski, T. Hirono, H. Krüger, and N. Wermes

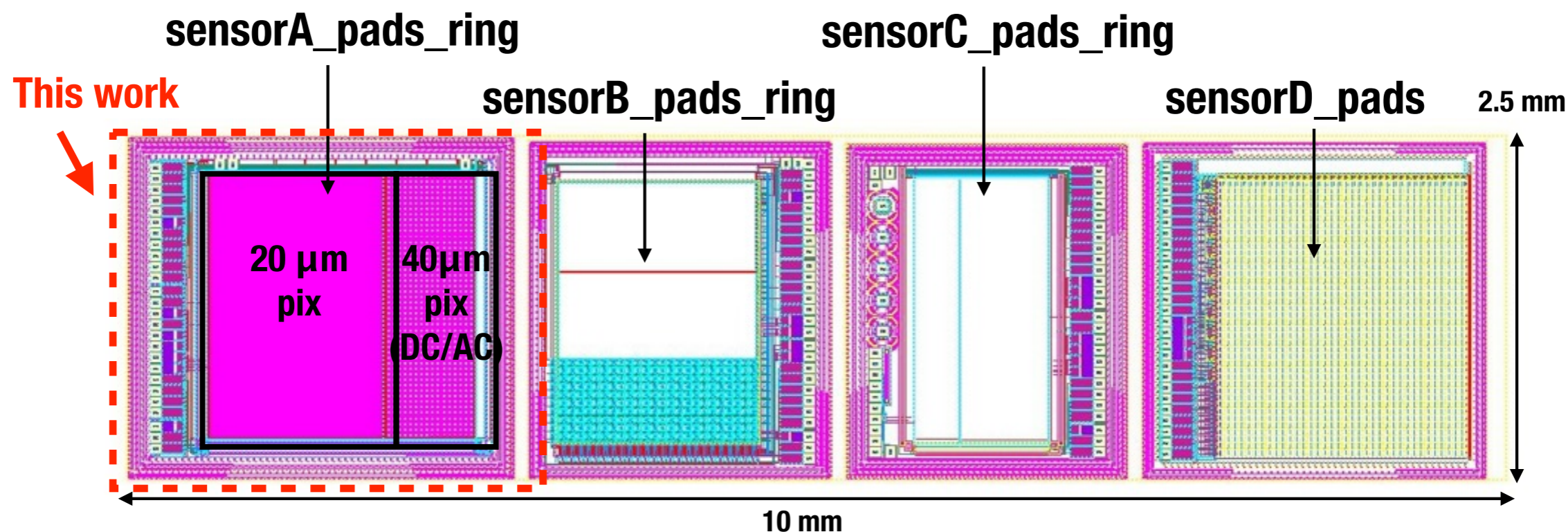


Technological overview

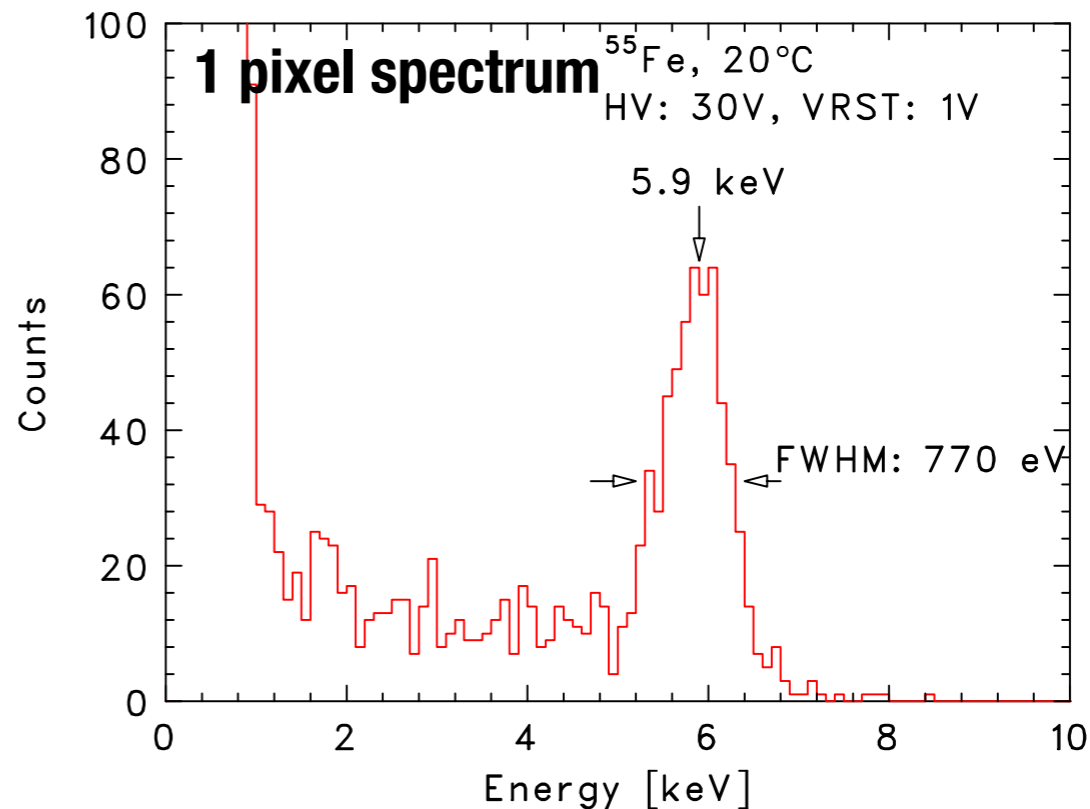
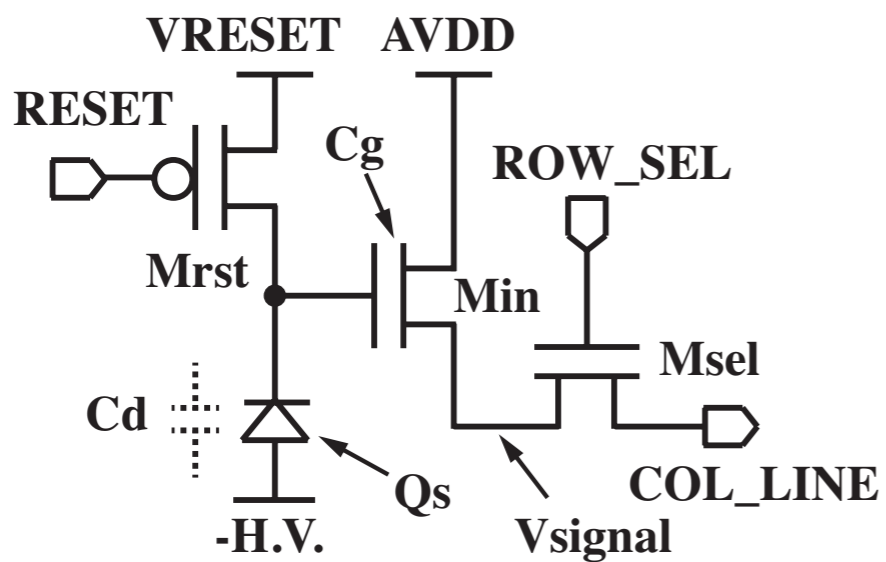
- Toshiba 130 nm CMOS process
- 1.5 V core, 5 metals, high-R. p-substrate ($\sim 2 \text{ k}\Omega\cdot\text{cm}$)
- w/o backside processing \rightarrow biasing from peripheral ring (DPW)



Layout of the prototype chip

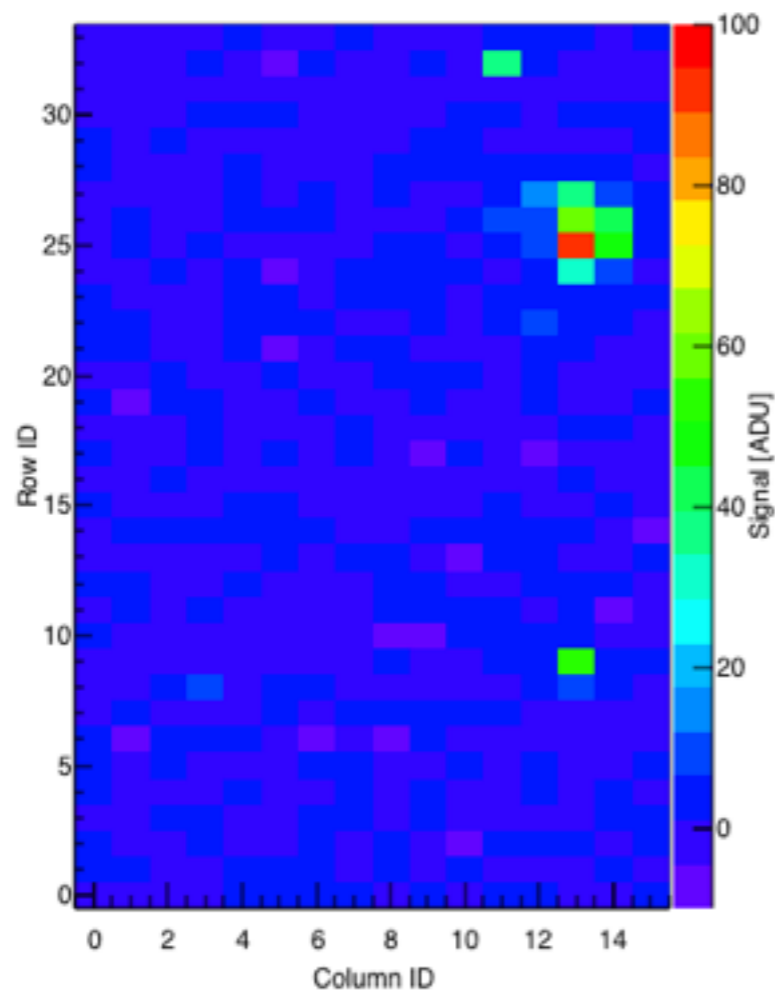


3T readout and spectrum from ^{55}Fe

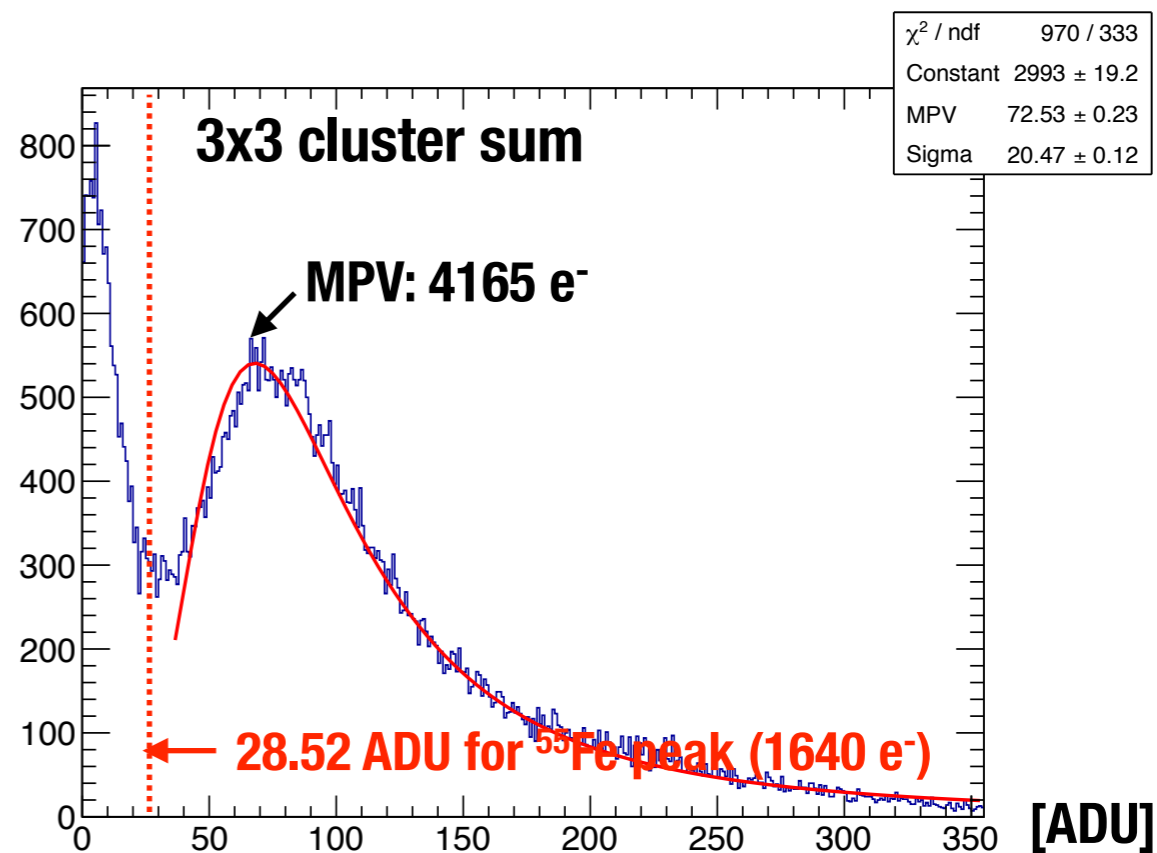


Irradiation test with ^{90}Sr

cluster image



Input capacitance was estimated from ^{55}Fe peak.



The depletion depth is ~50 μm , assuming full charge collection.