THE UPGRADE OF THE ATLAS FIRST LEVEL CALORIMETER TRIGGER

Shimpei Yamamoto (ICEPP/UTokyo)
on behalf of the ATLAS Collaboration

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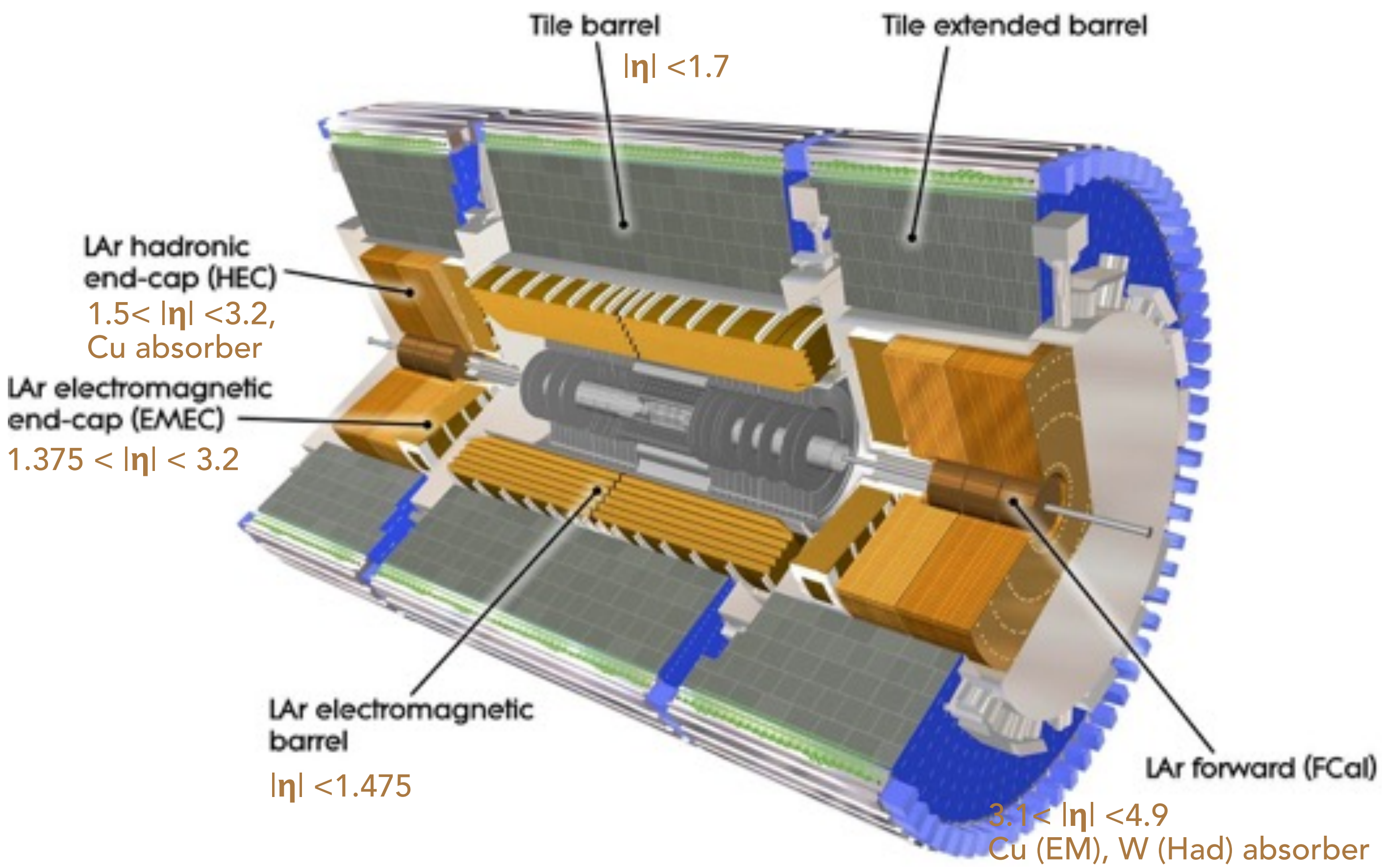
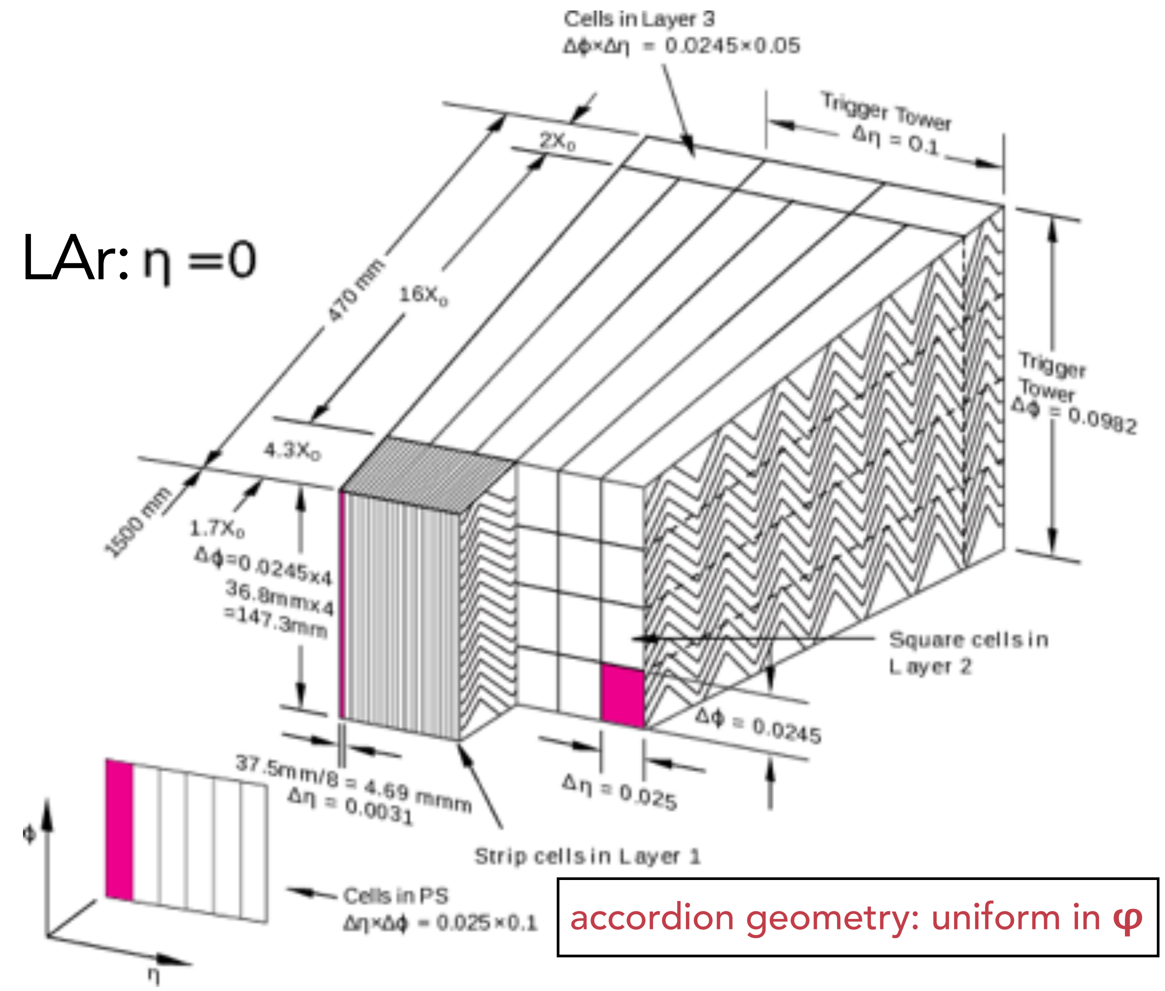
Outline

- Introduction
  - ATLAS Liquid Argon calorimeter and level-1 trigger
  - Challenges toward high luminosity runs
- Upgrading ATLAS level-1 calorimeter trigger
  - New Liquid Argon calorimeter trigger readout
  - New system architecture for trigger processing
  - Expected performances
- Summary

ATLAS Calorimetry





- **Liquid Argon (LAr) electromagnetic calorimeter**
  - Lead absorber, LAr as active material and copper/kapton electrode
  - Has fine segmentation: 4 layers, ~200k readout channels in total
- Hadronic calorimeters : Tile (steel&scintillator), LAr endcap/forward
- Plays a major role in identifying/measuring e, γ, τ, jet and missing E_T (offline) and provides inputs for their triggers at the hardware level (**L1Calo** triggers)
  - Higgs discovery! Lots of searches in variety of channels, precise measurements, ..

LHC and ATLAS trigger upgrade timelines

Staged upgrade plan:

- Run 1 (2010-2012)
  7-8TeV, $L \sim 0.8 \times 10^{34}\ cm^{-2}s^{-1}$, $<\mu>\sim 20$
  ⇐ LS1/**Phase-0** upgrade (2013-2014)
- Run 2 (2015-2017)
  13-14TeV, $L \sim 1.6 \times 10^{34}\ cm^{-2}s^{-1}$, $<\mu>\sim 40$
  ⇐ LS2/**Phase-1** upgrade (2018-2019)
- Run 3 (2020-2022)
  14TeV, $L \sim 3.0 \times 10^{34}\ cm^{-2}s^{-1}$, $<\mu>\sim 80$
  ⇐ LS3/Phase-2 upgrade (2018-2019)
- Run 4 (2025-2027)
  14TeV, $L \sim 7.0 \times 10^{34}\ cm^{-2}s^{-1}$, $<\mu>\sim 200$

- Instantaneous luminosity getting increased!!
  - Number of interactions per bunch crossing (μ) doubled, tripled and much more..
- ``Pile-up effects" significantly degrade the trigger performance:
  - **Degraded LAr signal due to its long drift time**: ~450ns drift time (with 2mm gap at 2 kV) vs. 25ns LHC bunch spacing (40MHz)
  - **Triggering electromagnetic objects suffers from huge multi-jets background**

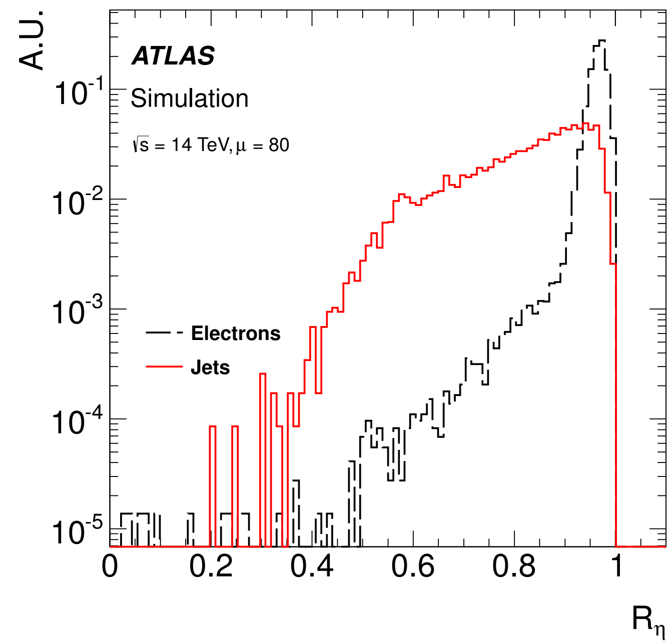
General upgrade concept

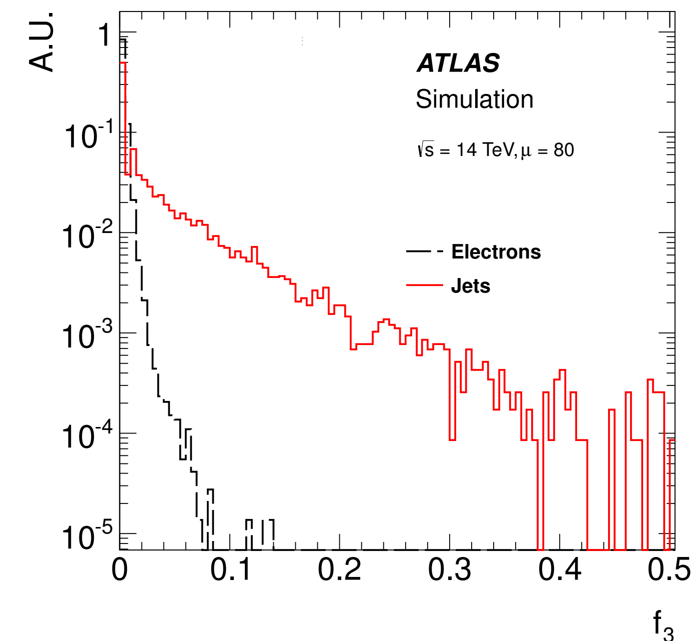
- Utilize more calorimeter shower shape information&event topology as in software algorithms — high-level triggers use this information as well.

e.g. e/jet separation

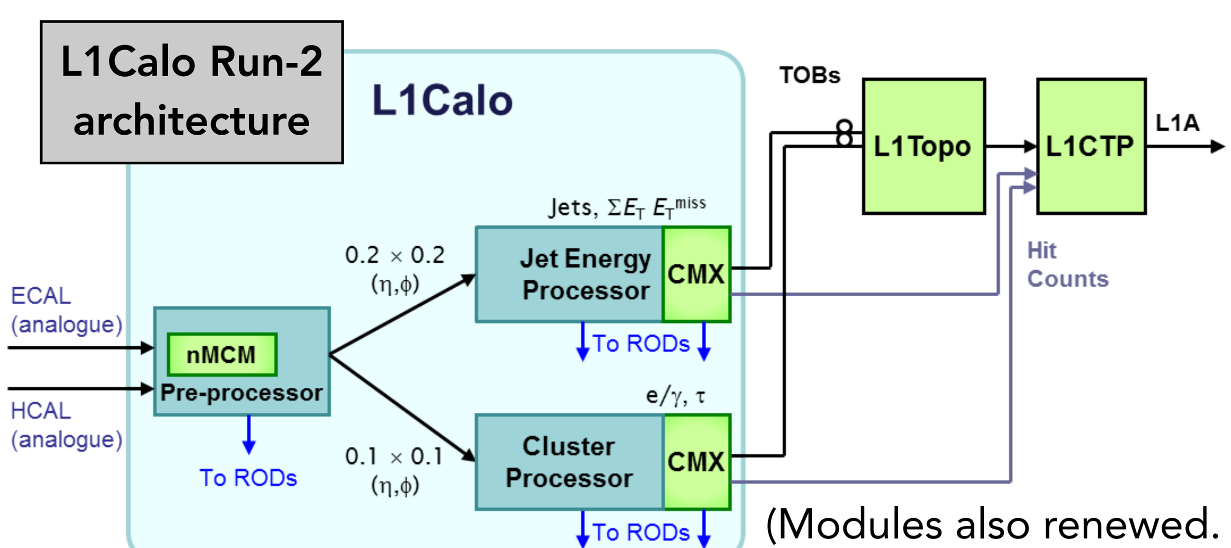
$$R_\eta = \frac{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.175\times0.2}}$$

$$f_3 = \frac{E^{(3)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.2\times0.2}}{E^{(1)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2} + E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2} + E^{(3)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.2\times0.2}}$$

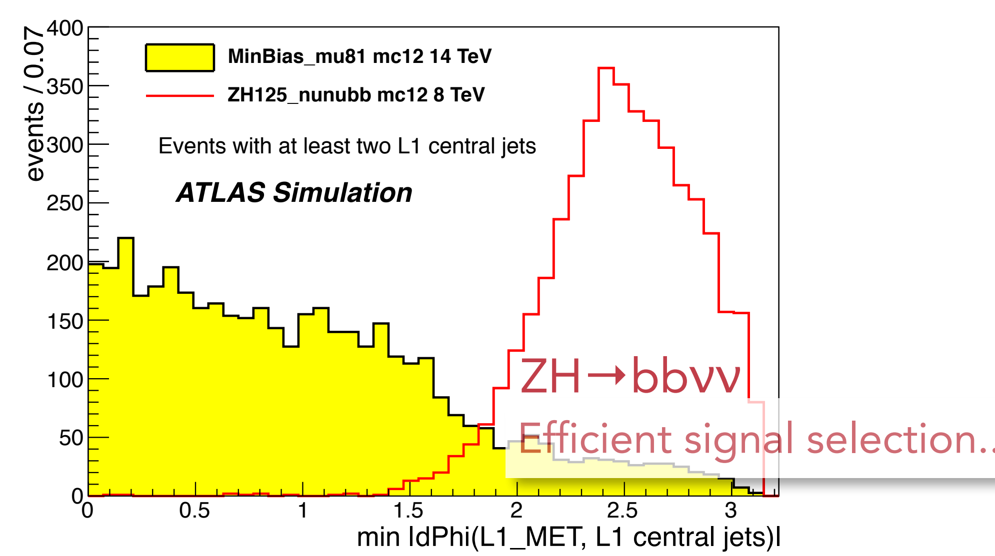




- Already partially implemented in Run-2: L1Calo provides trigger capabilities based on event topologies.
  - New module "**L1Topo**" installed. Can apply selection with topological variables as Δφ, Δη, ΔR, H_T, …



(Modules also renewed. Details in backup)



General upgrade concept (2)

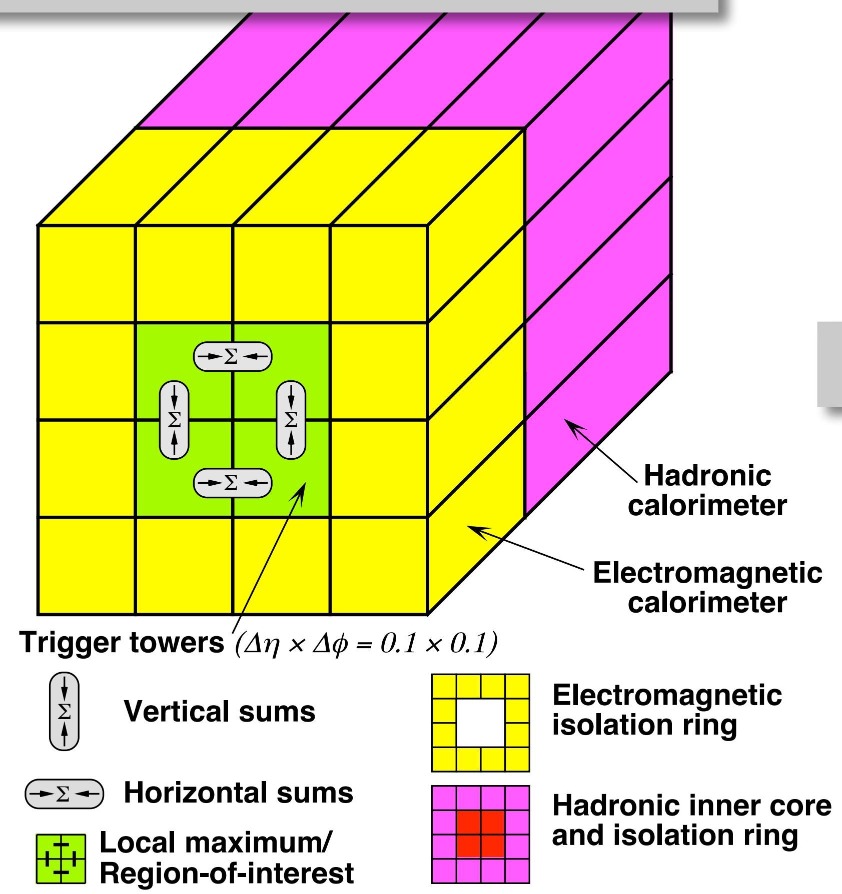
- To achieve these trigger features, develop new hardware for trigger readout and processing.
  - **LAr trigger readout**
    - Fully digitized readout with finer granularity & digital filtering for out-of-time pile-up correction and bunch-crossing identification
  - **L1Calo trigger processing**
    - Pile-up subtraction, employ selection fully based on object features and event topology information

- Challenges:
  - Highly dense electrical&optical circuit boards & high-speed optical links (up to ~10 Gb/s)
  - Signal mapping and data duplication among readout modules

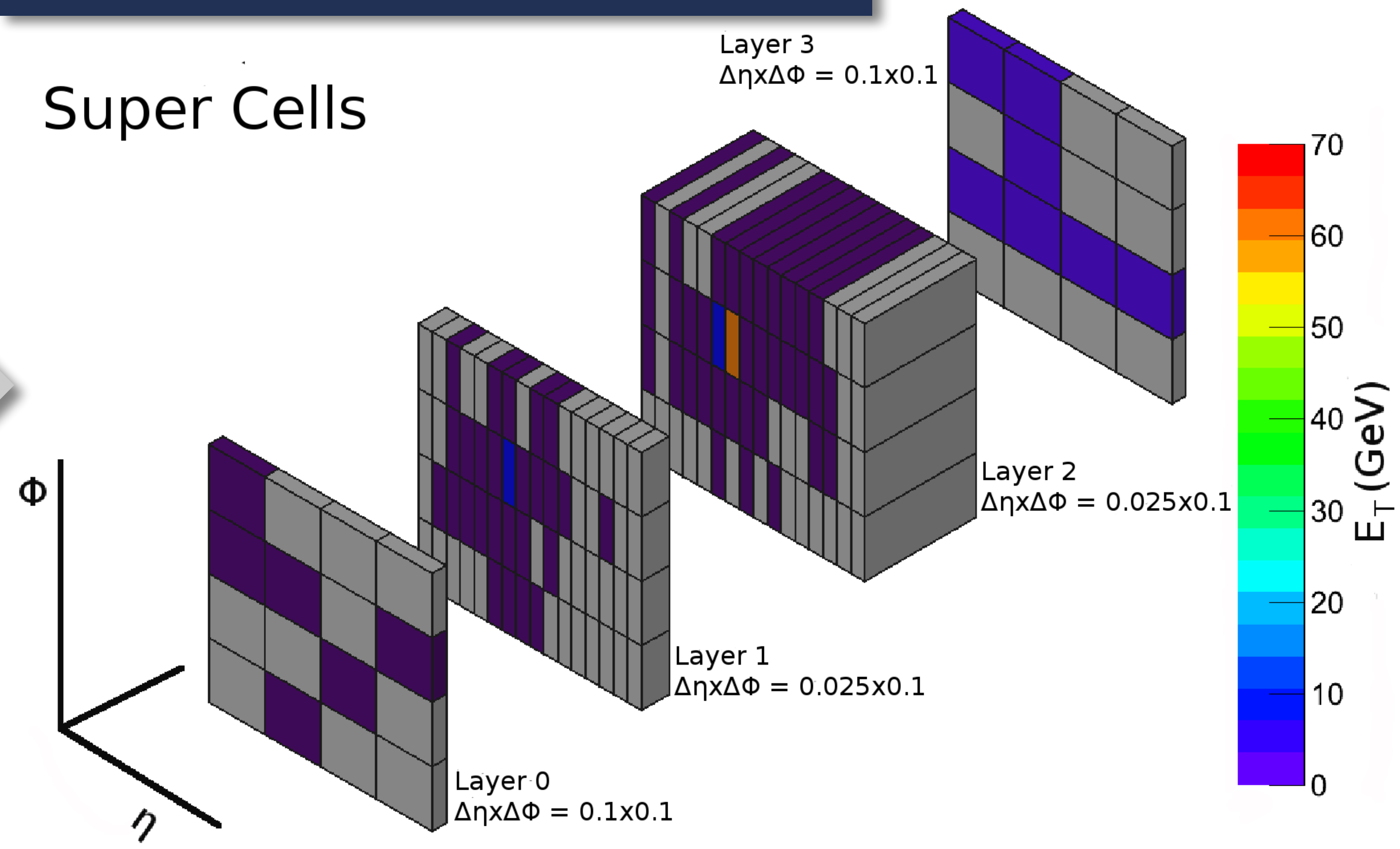
Upgrading LAr trigger readout: Super Cells

Trigger tower

Analog sum in $\Delta\eta\times\Delta\varphi$=0.1×0.1 (60 cells)



Run-2 readout geometry



(box: minimal readout element)

- Finer granularity: trigger tower $\Longrightarrow$ 10 Super Cells (SCs)
  - 60 cells $\Longrightarrow$ 4-8 cells in each layer
- Analog readout $\Longrightarrow$ 40MHz digital readout

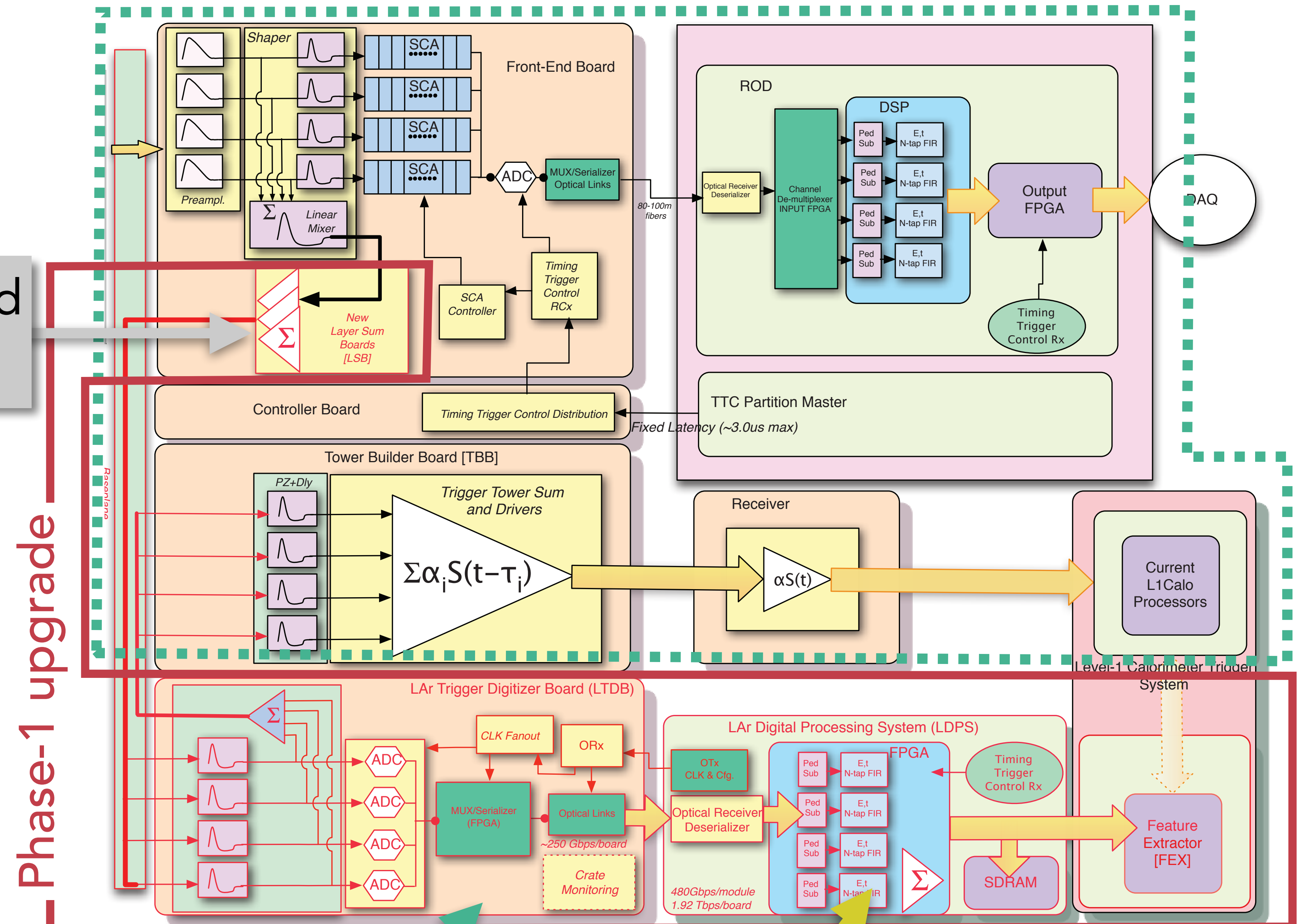
Upgrading LAr trigger readout: Scheme

Existing cell-readout

Sampled at 40MHz, stored in analog pipelines.

Digitized and transmitted when Level-1 accept received.

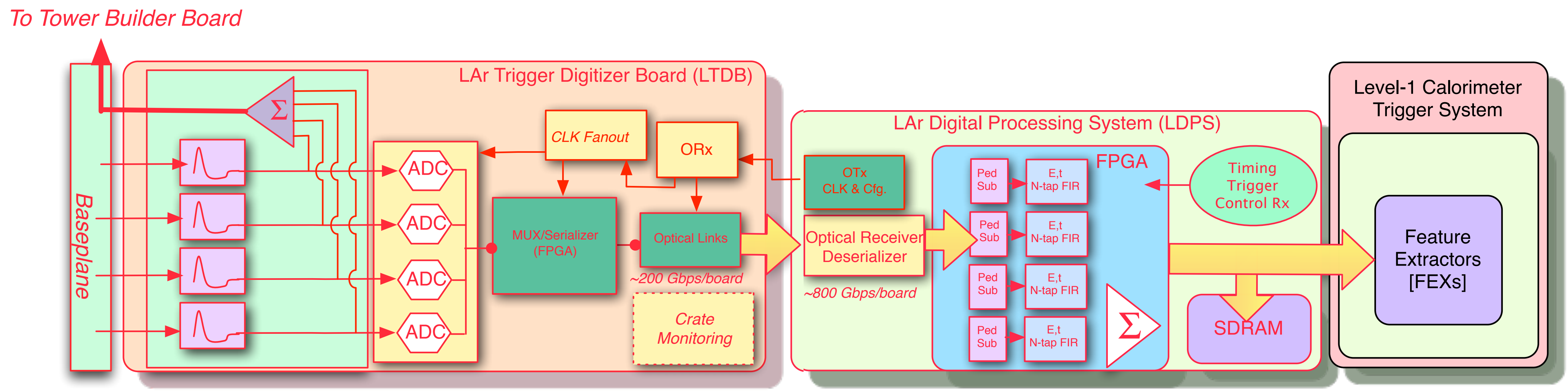
``Layer-sum board" renewed to produce SCs



New LAr Trigger Digitizer front-end Board (LTDB)

New LAr Digital processing back-end Board (LDPB)

LTDB & LDPB



LTDB

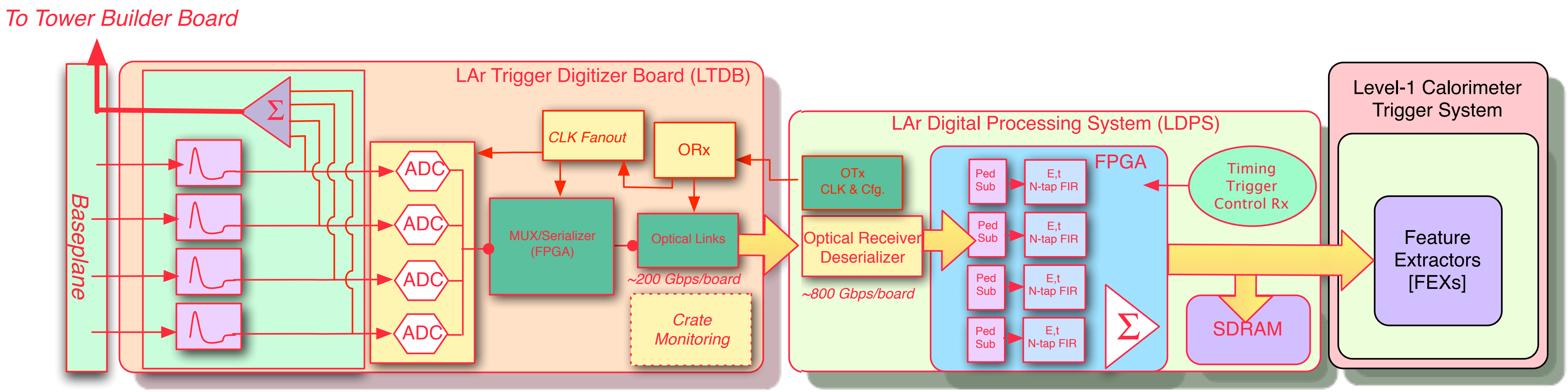
- 12-bit ADC (custom ASIC) @40MHz
  - Multiplexing 8 channels to 5.12Gb/s optical link, 200Gb/s for each board
- Handle up to 320 SC signals
- 124 boards in total (~25Tb/s)

LDPB

- ATCA standard, 4 Advanced Mezzanine Cards (AMCs) for each
- AMC:
  - high-speed optical transceivers to process 320 SCs with a short latency
  - Energy&timing measurements by FPGA digital filtering

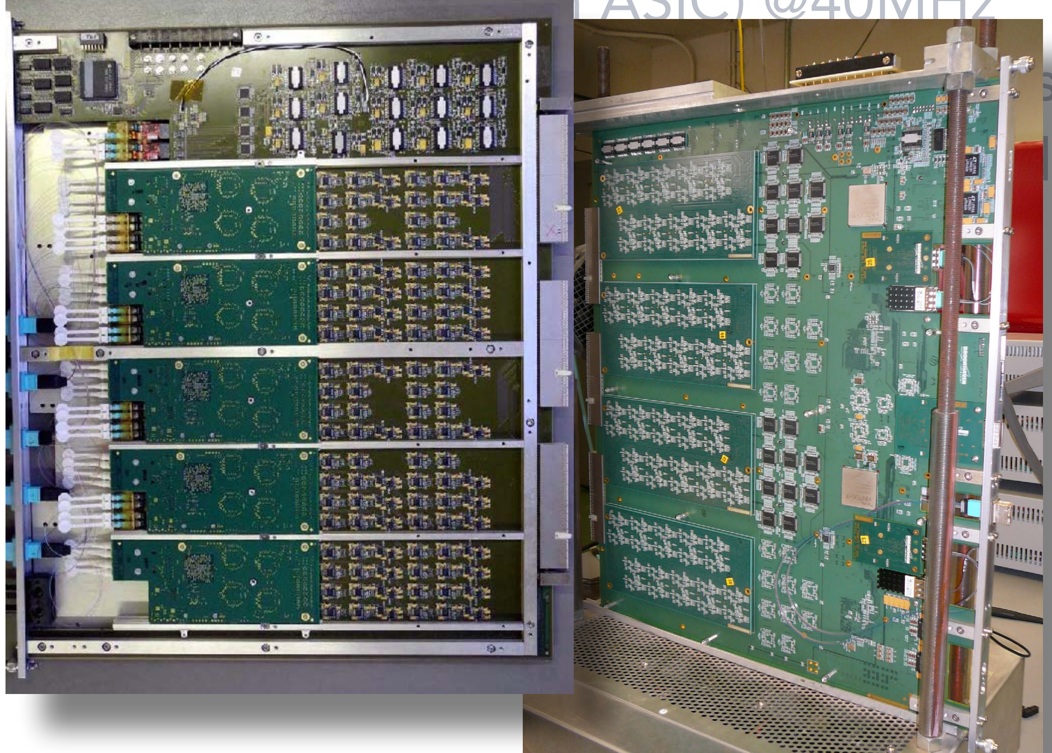
Both LTDB and LDPS prototypes integrated in the detector system and being demonstrated during Run-2 running.

LTDB & LDPB



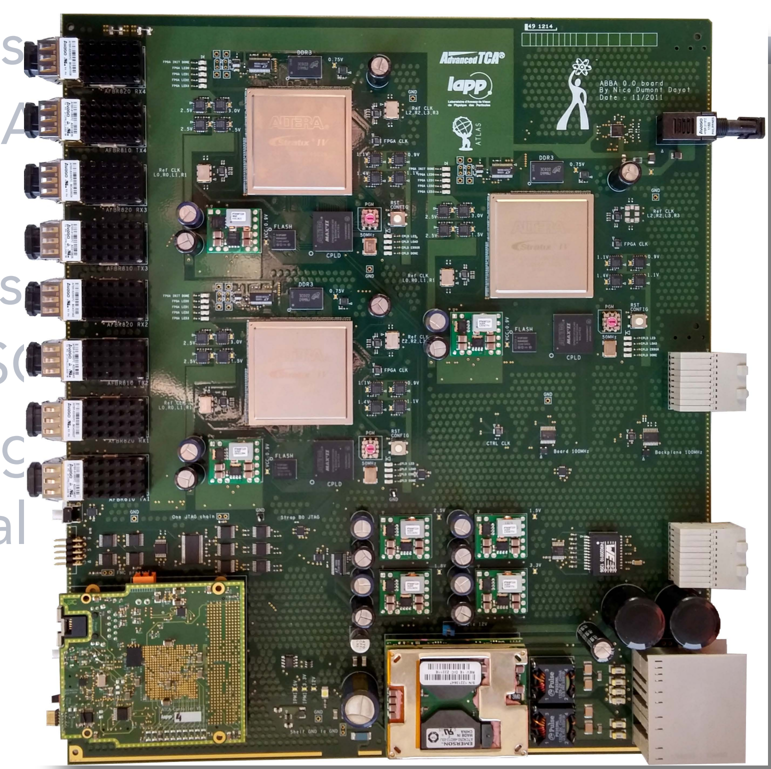
LTDB

12 bit ADC (custom ASIC) @40MHz



LDPB

- ATCA s… Cards (A… …nine
- AMC:
  - high-s… 320 S… …process
  - Energ… digital … FPGA



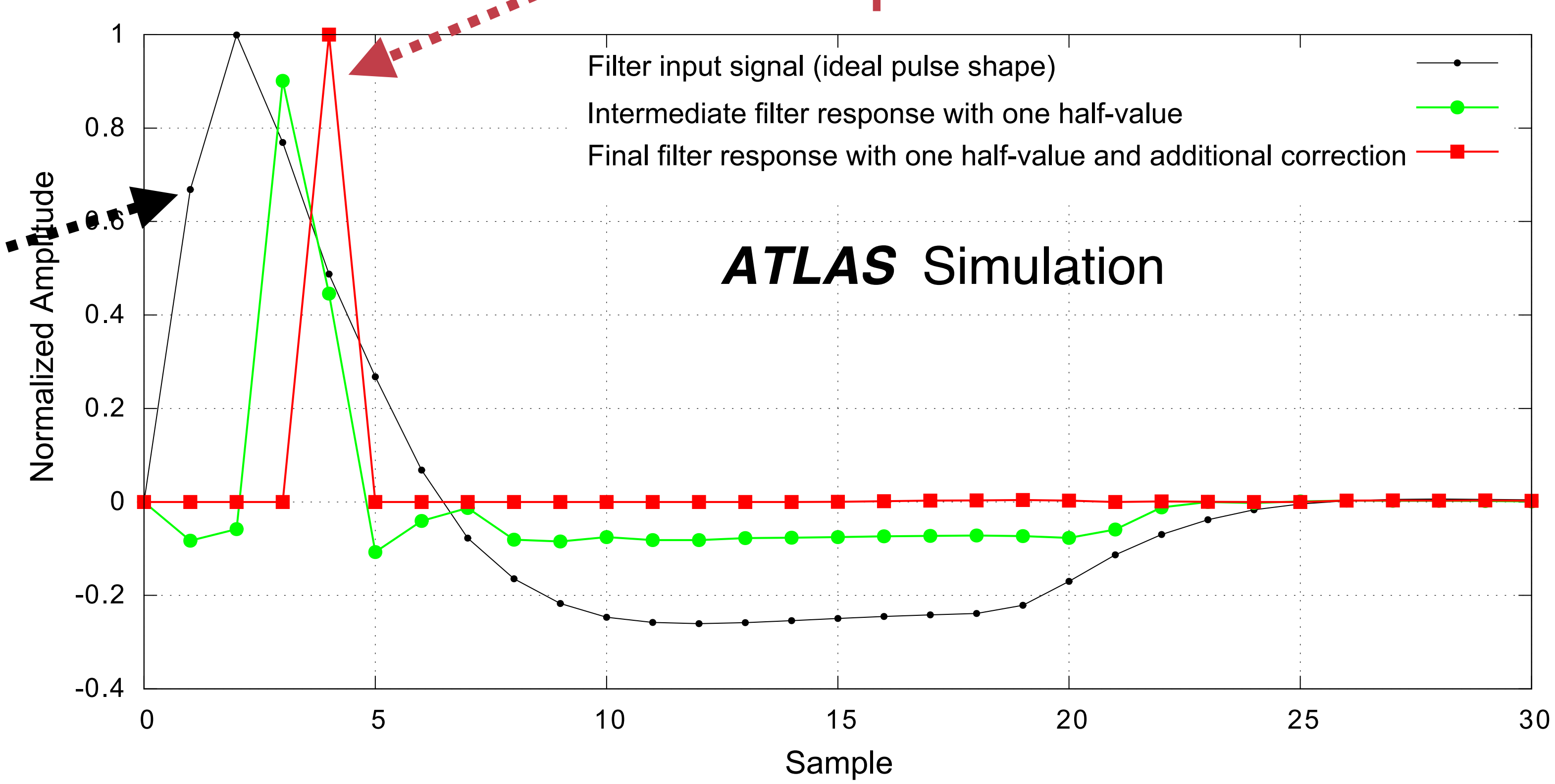
Both LTDB and LDPS prototypes integrated in the detector system and being demonstrated during Run-2 running.

SC signal reconstruction by digital filtering

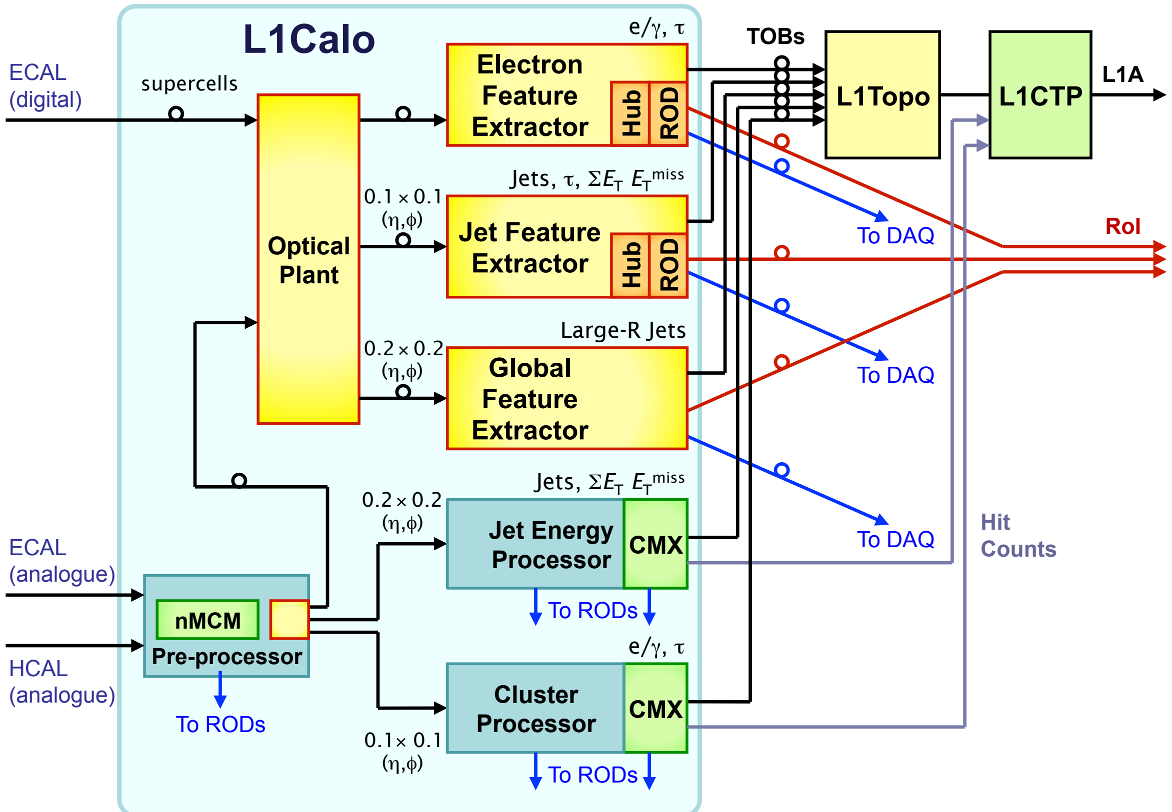
- LDPB can enhance performance on the SC energy reconstruction by processing 40MHz ADC samplings with dedicated digital filtering.
- Filtering algorithms under study.
  - e.g. Wiener filter:
    - Nice ``energy reconstruction” and ``bunch-crossing identification”
    - Expected to be pile-up robust by adopting an active forward pile-up correction

Filter output

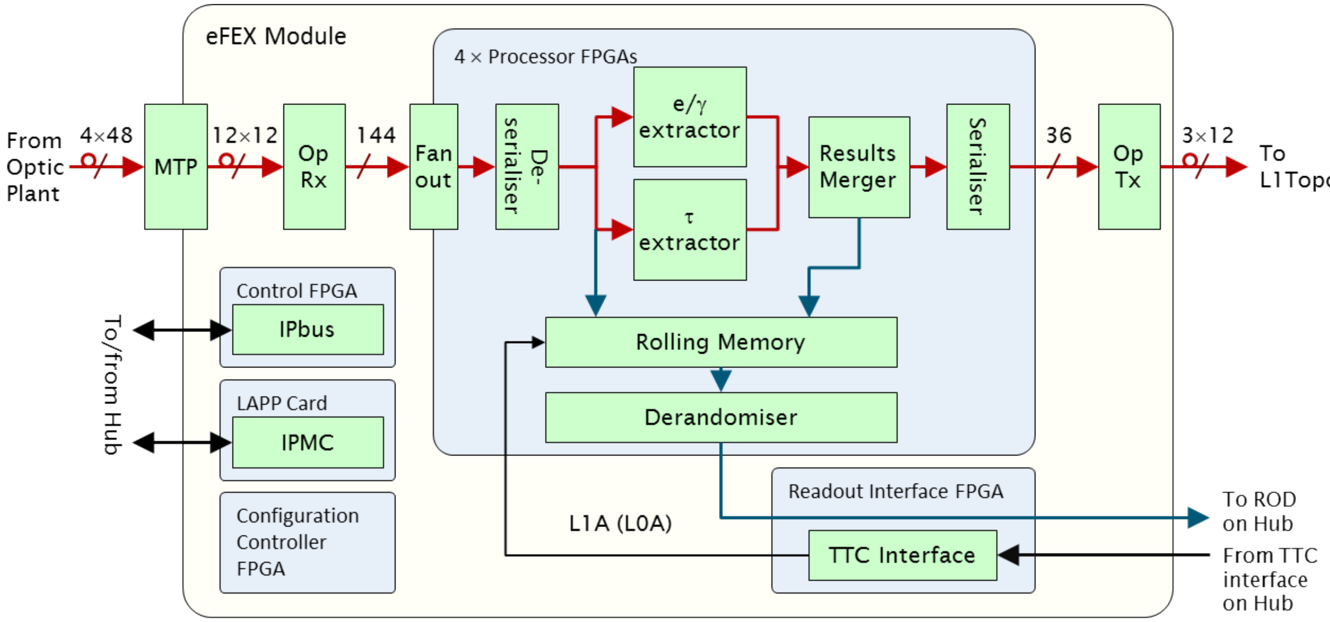
SC signal
(40MHz ADC sampling)



Upgraded L1Calo: System architecture



eFEX schematic view



Feature extractor modules integrated for Run-3.

eFEX:

Identify e/γ/τ using isolation & cluster shape variables. Flexible rejection algorithms.

jFEX:

Identify jet/τ and calculate H_T, missing E_T.

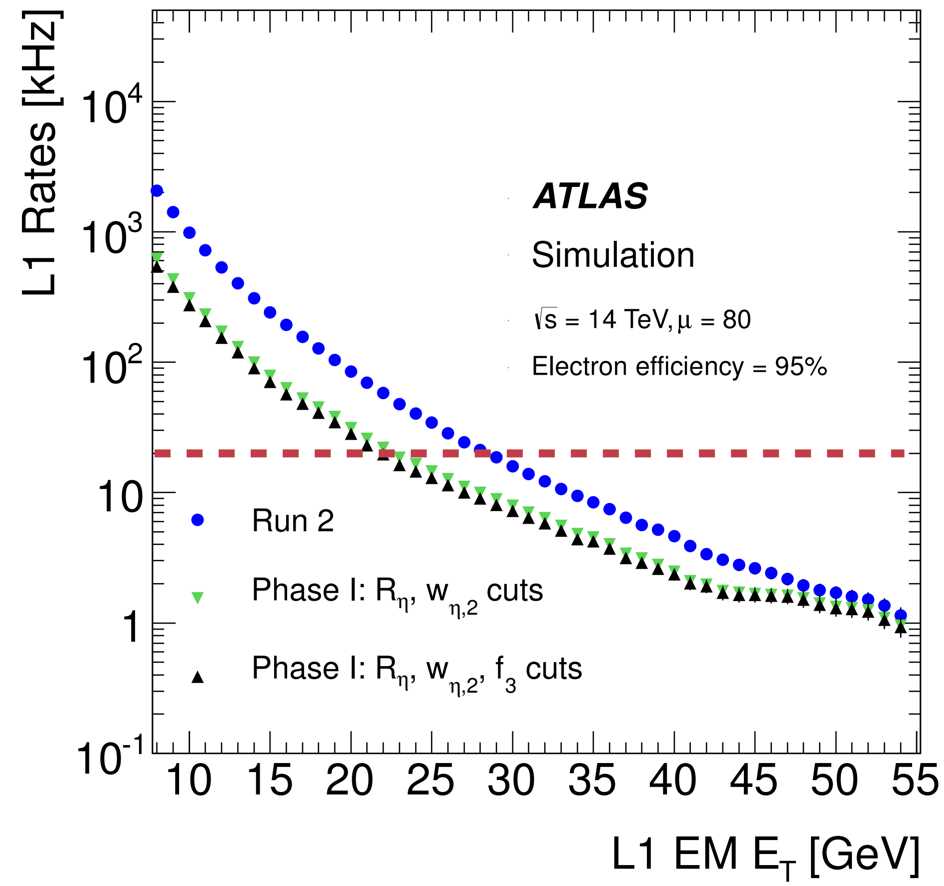
Enables pile-up suppression using event energy density

gFEX:

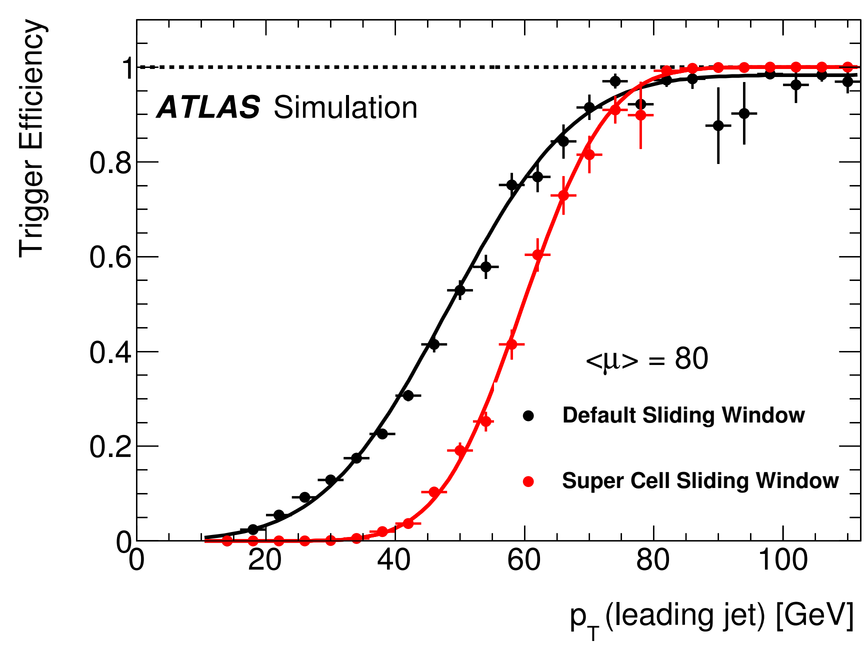
For global event processing, e.g. large-area jets for dedicated physics cases (boosted bosons, …)

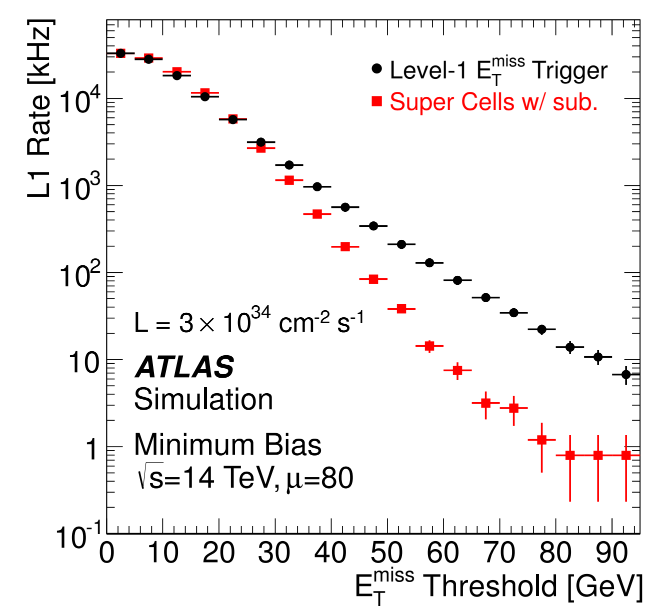
Expected performance: single-object triggers

- EM trigger rate:
  - Adopting jet rejection using shape variables, the threshold can be lowered by 7 GeV
    - Compared at reference points of 20kHz (Run-2 rate budget) and 95% efficiency
    - Can maintain high photon efficiency (>96%)



- Better trigger turn-on for jet and missing E_T triggers
    - Thanks to pileup suppression and dedicated jet reconstruction algorithm





Summary

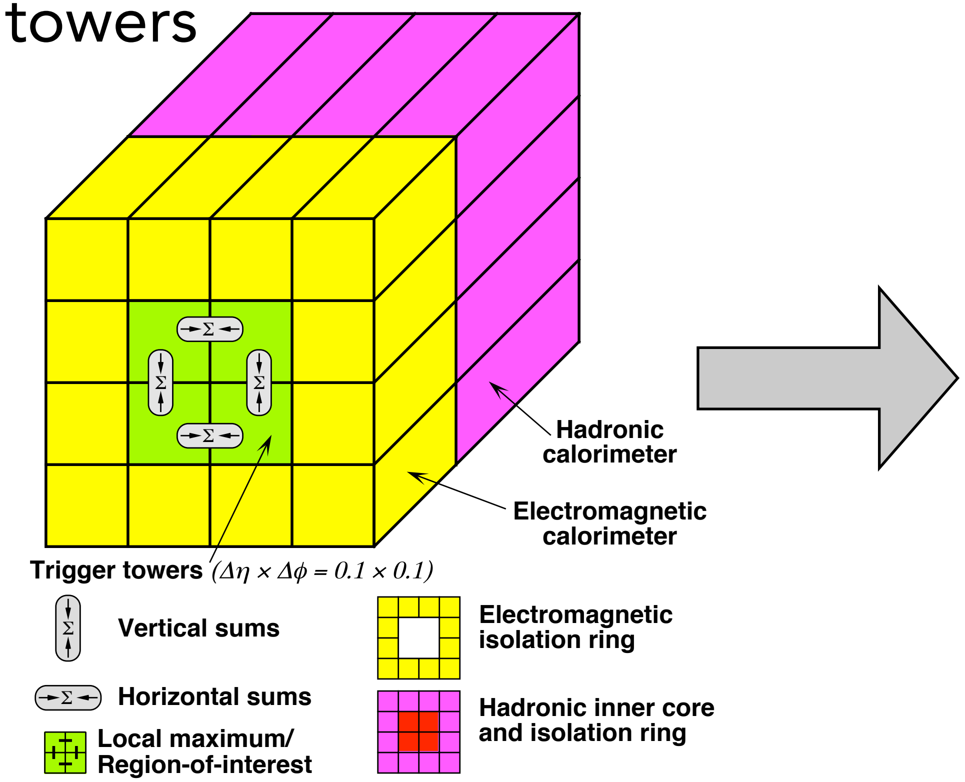
- Upgrade activities ongoing in order to explore full physics of the high-luminosity LHC runs.
- ATLAS is developing new hardware and system for calorimeter trigger readout and processing.
  - Expect improved trigger performances with the upgraded system even in severe pile-up conditions.
  - R&D, design and production in progress toward installation in 2018-2019 (Phase-1 upgrade)
  - Some of them are already integrated for ATLAS Run-2 running:
    - LTDB & LDPS prototypes for demonstration
    - Topological trigger with new L1Calo architectures

Backup

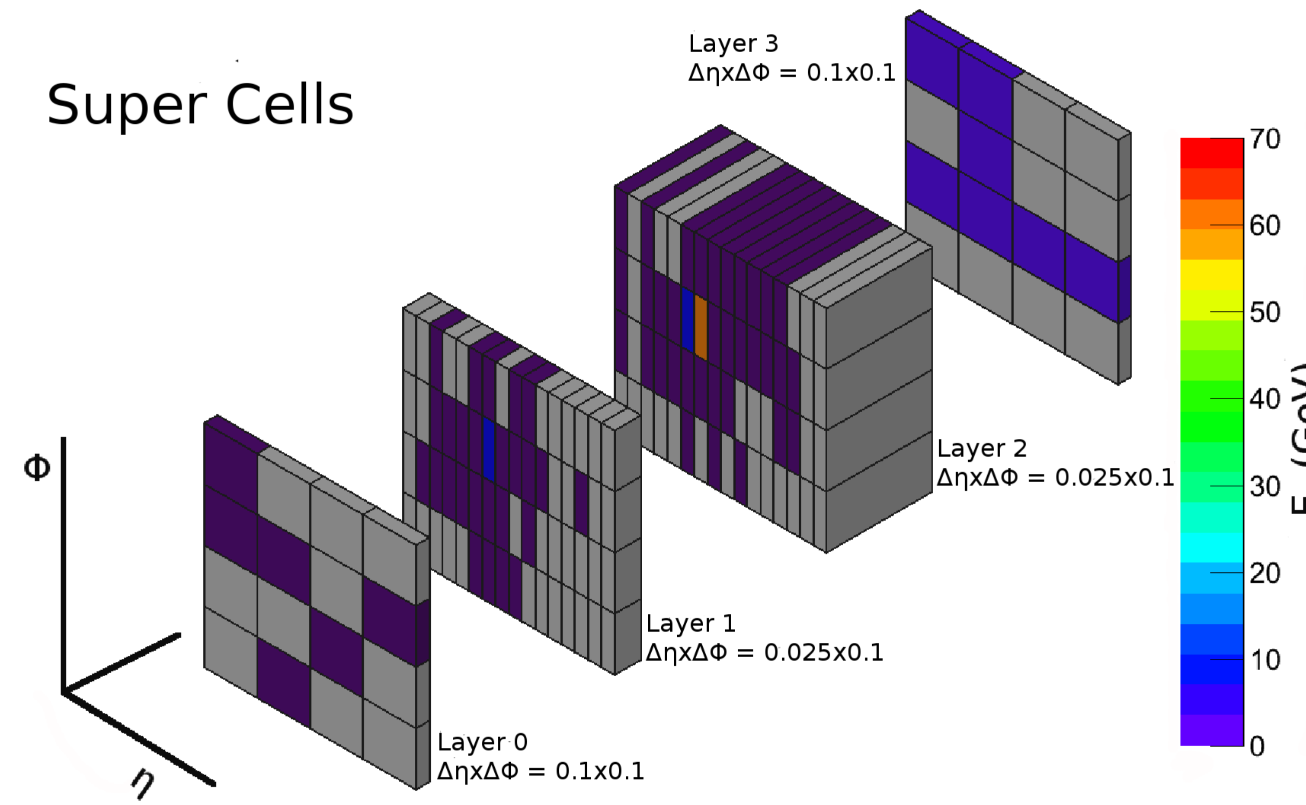
Super Cells

- Trigger tower ⟹ <u>10 Super Cells (SCs)</u>

Trigger towers

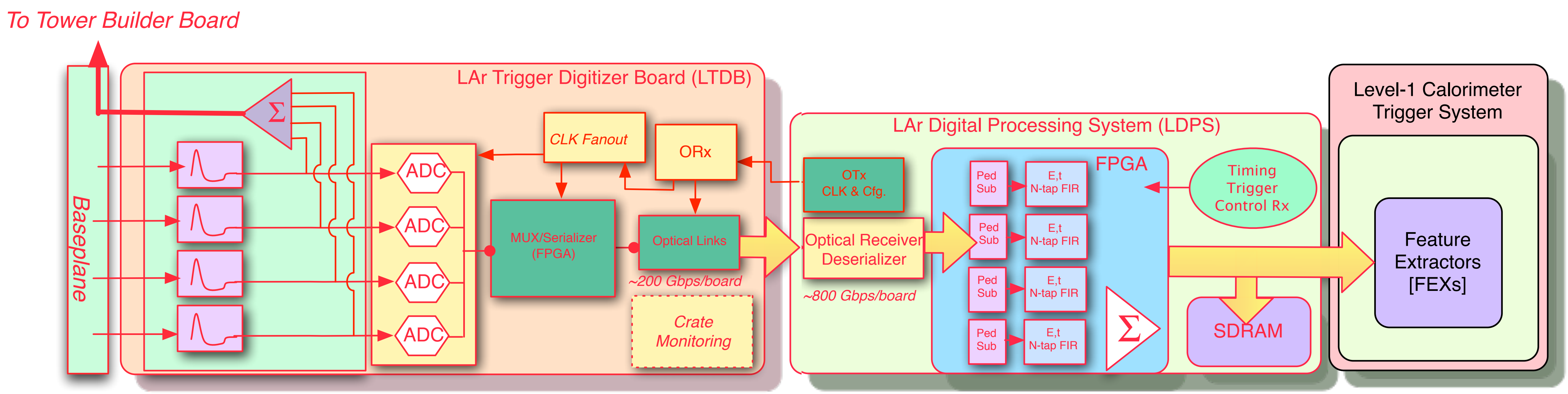


Super Cells



	Elementary Cell	Trigger Tower		Super Cell	
Layer (barrel)	$[\Delta\eta \times \Delta\varphi]$	$[n_\eta \times n_\varphi]$	$[\Delta\eta \times \Delta\varphi]$	$[n_\eta \times n_\varphi]$	$[\Delta\eta \times \Delta\varphi]$
Presampler (layer 0)	0.025 × 0.1	4 × 1	0.1 × 0.1	4 × 1	**0.1 × 0.1**
Front (layer 1)	0.003125 × 0.1	32 × 1		8 × 1	**0.025 × 0.1**
Middle (layer 2)	0.025 × 0.025	4 × 4		1 × 4	**0.025 × 0.1**
Back (layer 3)	0.05 × 0.025	2 × 4		2 × 4	**0.1 × 0.1**

LTDB & LDPB specifications



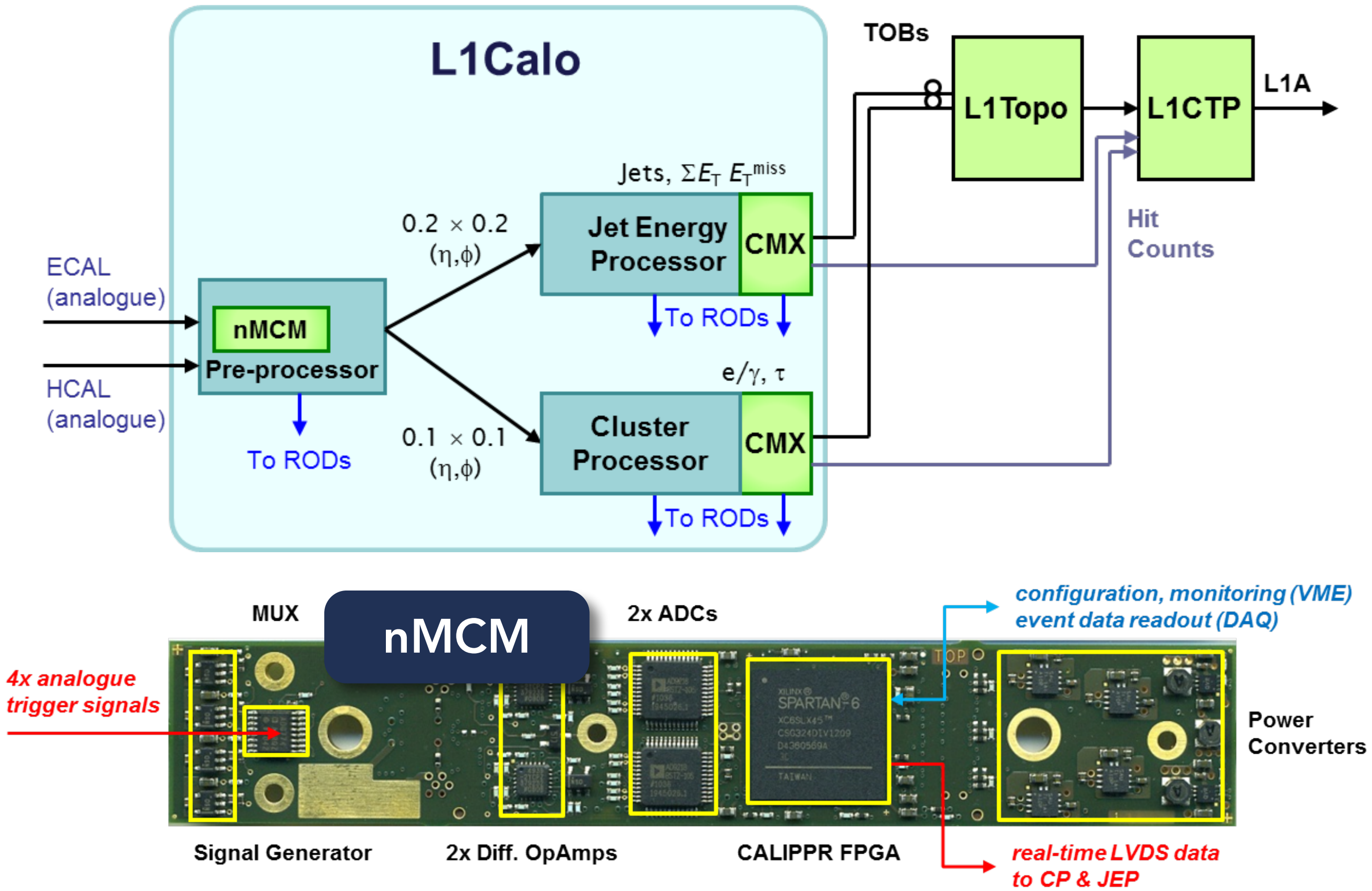
LTDB

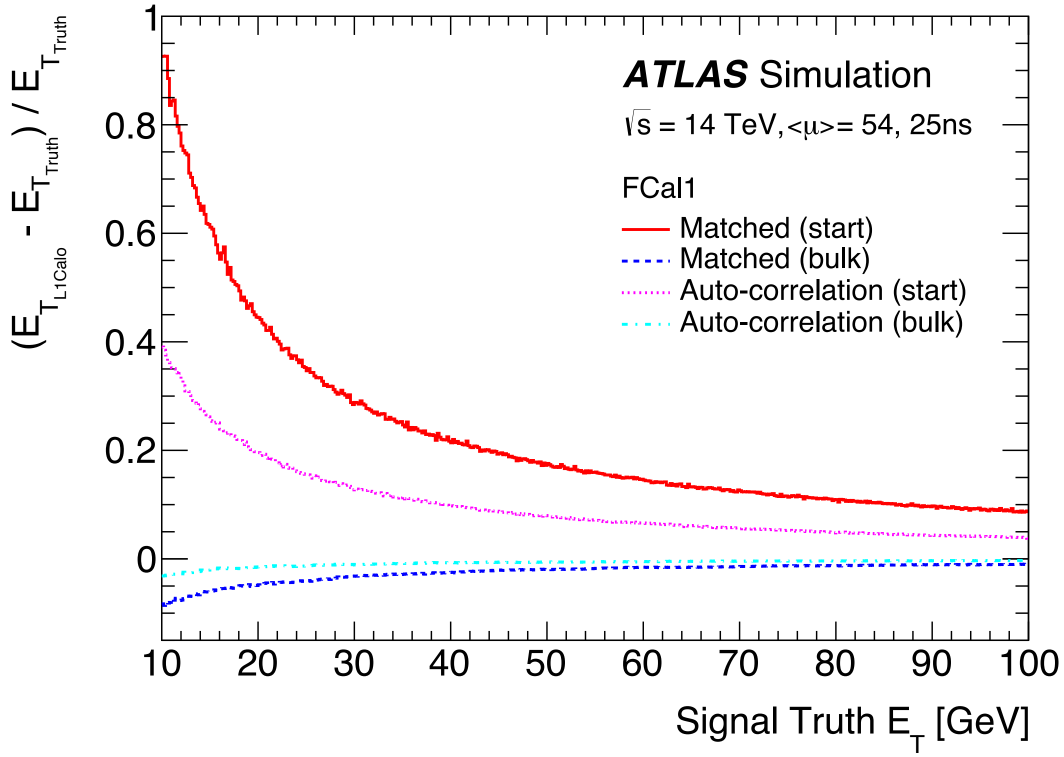
- Handle up to 320 SC signals
- 12-bit ADC @40MHz with low power consumption (custom ASIC)
  - <145 mW/channel
- Multiplexing 8 channels to 5.12Gb/s optical link, 200Gb/s for each board
- 124 boards in total (25Tb/s)

LDPS

- ATCA standard, 4 Advanced Mezzanine Cards (AMCs) for each
- AMC designed with FPGA and high-speed optical transceivers to process 320 SCs with a required latency (17 bunch crossings)
- Energy measurement&bunch-crossing identification by FPGA digital filtering Receive 25Tb/s (from LTDB) and transmit 41Tb/s (to L1Calo)

Upgraded L1Calo: Run-2 system architecture





Phase-0 upgrade (for Run 2)

New Multi Chip module (nMCM):

ASIC→FPGA replacement for digital signal processing

Better treatment of pile-up (autocorrelation FIR filter & dynamic pedestal subtraction)

Dedicated calibration for EM and hadron energy scale using dual-channel ADCs

New(extended) Common Merger Module (CMX):

160Mb/s backplane (data from processor modules), multiplicities→trigger objects.

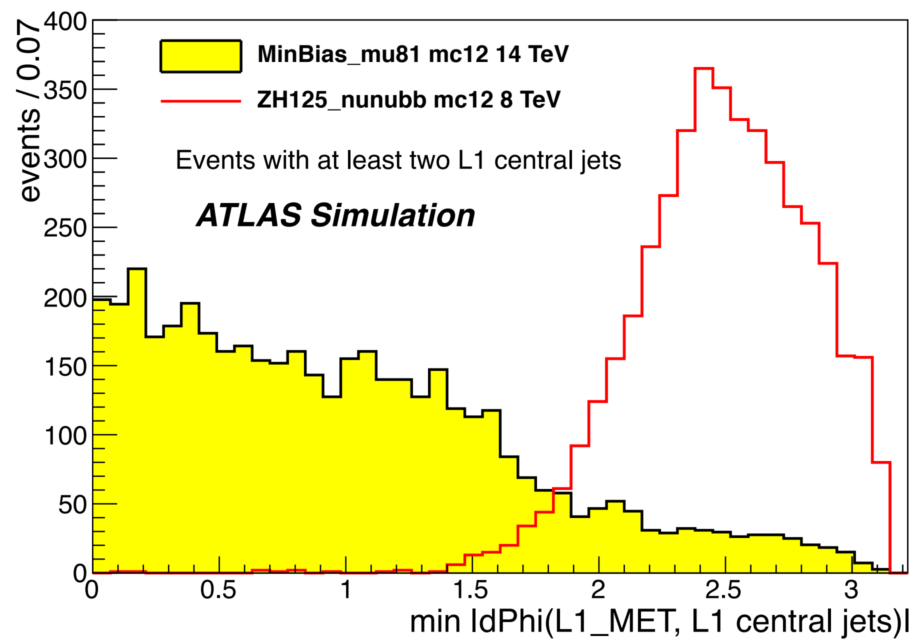
Link to L1Topo (24 opt. fibers at 6.4Gb/s)

Topological trigger module (L1Topo):

Enables composite triggers using trigger objects. Topological algorithms.

Expected performance: L1Topo, FEX

- L1Topo (already installed for Run-2)
  - Can apply selection with topological variables: Δφ, Δη, ΔR, H_T, …
  - Challenging analyses will benefit from that.
    - ZH→ννbb, di-tau etc.



- jFEX (Run-3)
  - Gaussian filter: jet energy reconstruction using Gaussian weights
    - Less sensitive to pile-up, significant rate reduction thanks to improved trigger turn-on.
    - Expect much better performance by adopting calibrations and optimizing in terms of pile-up.