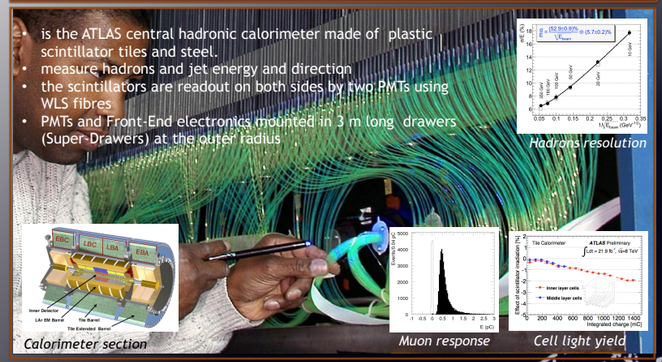
Upgrade of the ATLAS Tile Calorimeter for the High Luminosity LHC

G. Usai
U. Texas at Arlington
on behalf of the ATLAS Tile Calorimeter system

Tile Calorimeter

- is the ATLAS central hadronic calorimeter made of plastic scintillator tiles and steel.
- measure hadrons and jet energy and direction
- the scintillators are readout on both sides by two PMTs using WLS fibres
- PMTs and Front-End electronics mounted in 3 m long drawers (Super-Drawers) at the outer radius



Calorimeter section

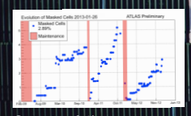
Hadrons resolution

Muon response

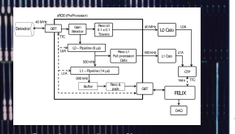
Cell light yield

Upgrade motivations

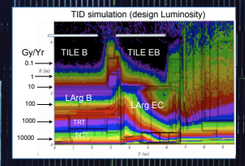
- The LHC upgrade in 2023 aim to a factor (5-10) luminosity increase
- better radiation tolerance is desirable
- better precision and finer granularity in the trigger to cope with increased interaction rate
- ageing of components exceeding the design lifetime
- improve the reliability
- reduce and simplify the maintenance needs including radiation exposure for personnel (ALARA)



Detector failures



Read-out data flow

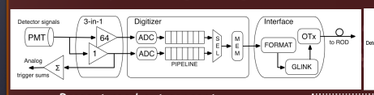


Read-out architecture

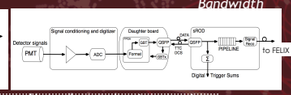
- complete replacement of Front-End and Back-End electronics
- digital information with full granularity and precision for L0/L1 trigger levels
- pipelines moved to the BE electronics
- three FE options being investigated

Up Link only	Present	Upgrade
Total BW	~ 160 Gbps	~80 Tbps
Nb fibers	256	8192
Fiber BW	640 Mbps	10 Gbps
Nb RODs	32	329
In BW/ROD	5 Gbps	2 Tbps
Out BW/ROD $_{LAR}$	2.56 Gbps	~ 20 Gbps
Out BW/ROD $_{TILE}$	Analog FE	< 80 Gbps

Bandwidth

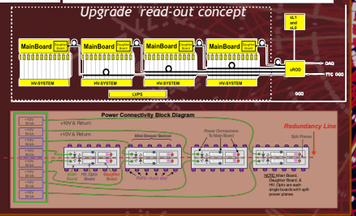


Present read-out concept



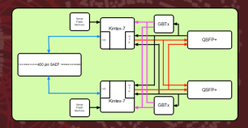
Upgrade read-out concept

- improve reliability with less interconnections and boards stack and implement redundancy
- minimise impact of failures with smaller DAQ elements: 4 independent mini-drawers with full redundant data path and powering



The optical interface and BE electronics

- the DaughterBoard and the ROD demonstrator prototype interface the new FE with the current ROD and Detector Control System
- 8 read-out links/super-drawer: 1+1 (redundancy) x 4 mini-drawers 10.24 (4.8) Gb/s up (down)
- Luxtera Active Optical links,4 bi-directional channels, excellent error rate: BER < 10^{-18} (~1err/3y)
- new methods used on the DB to mitigate radiation impact: CRC, internal scrubbing and redundant logic triplication



DaughterBoard principle

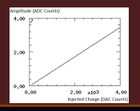
redundancy line

DaughterBoard Rev. 3

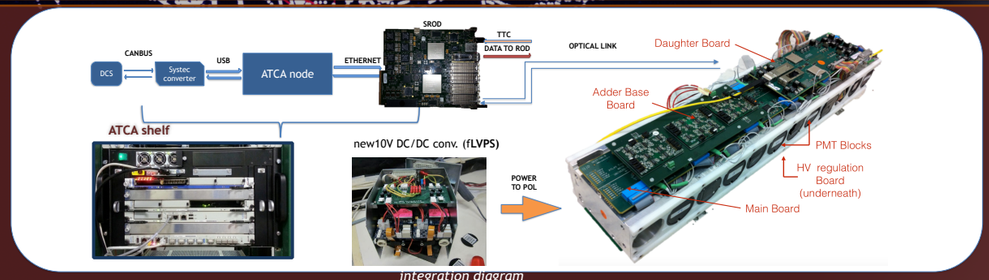
sROD/pre-processor prototype

Demonstrator prototype

- hybrid prototype to be integrated into ATLAS for evaluation of the new architecture
- full compatibility with the current system, provide both analog/digital trigger (use the 3in1 FE option)
- sROD prototype receive TTC/CANbus commands and send data back to the current ROD
- setup with a compete SD operational at CERN
- DCS integration well advanced
- calibration data (Charge Injection,LED pulses, ped) used to asses the performance



CI linearity



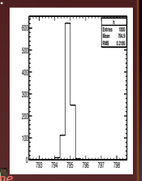
integration diagram

HV regulation

two options are being investigated:

- local HVOpto regulation (present)
- HV remote regulation + long cables
- active dividers are used to assure good PMT linearity in cells with large minimum bias currents

HVOpto prototype



HV stability

Radiation test

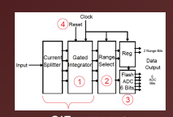
Done	On going	Preliminary
	Scheduled	*Not needed*

Subsystem	TID	NIEL	SEE
COTS Regulators			
3-in-1			
Main Board			
Daughter Board			
Modulator			
HV_Opto			
LVPS			
Adders			
Active bases			

Front End R&D

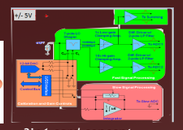
3 FE board options are being investigated. Final choice after test-beam:

- improved 3in1 FE (current system) using discrete components + separate board (MainBoard) for digitisation and servicing
- ASIC solution (FATALIC) combining current conveyor, 3 shaping stage and 12-bits ADCs at 40 MHz
- QIE chip fron FNAL, charge integration and encoding at 40 MHz



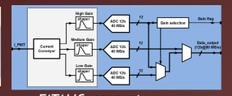
QIE concept

3in1 card



3in1 card concept

FATALIC FE prototype



FATALIC concept

Conclusions: a Tile demonstrator prototype was built and is being validated towards the integration into the ATLAS detector during the 2016 Christmas shutdown. Revision of many components is ongoing to improve performances. Exposure to beam test is planned during 2015/16, and the final technology choice thereafter.