In-pixel conversion with a 10 bit SAR ADC for next generation X-ray FELs

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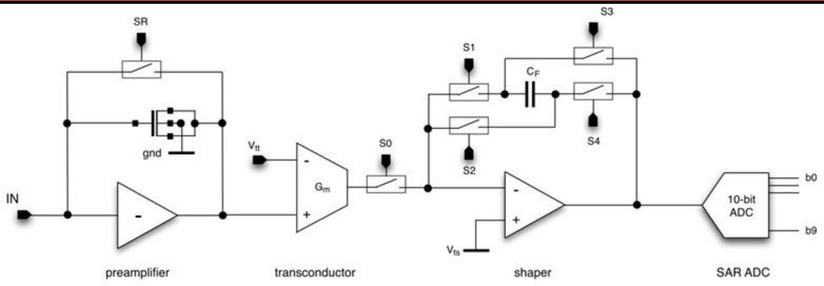
Abstract

This work presents the design of an interleaved Successive Approximation Register (SAR) ADC, part of the readout channel for the PixFEL detector. The PixFEL project aims at substantially advancing the state-of-the-art in the field of 2D X-ray imaging for applications at the next generation free electron laser (FEL) facilities, through the adoption of cutting-edge microelectronic technologies and innovative design and architectural solutions. For this purpose, the collaboration is developing the fundamental microelectronic building blocks for the readout channel. This work focuses on the design of the ADC carried out in a 65 nm CMOS technology: to obtain a good tradeoff between power, conversion speed and area occupation, an interleaved SAR ADC architecture was adopted.

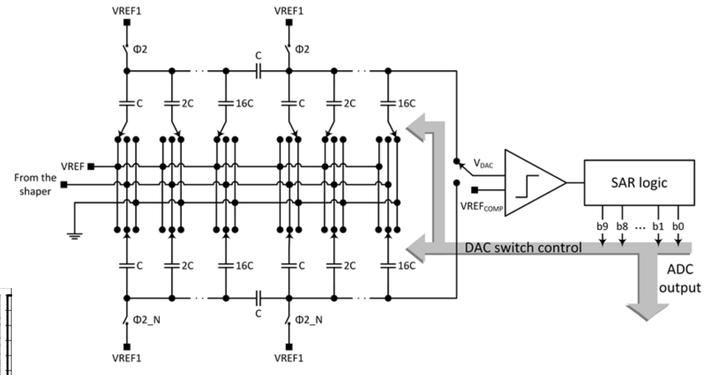
PixFEL readout channel



The signal from the detector is processed by a charge sensitive amplifier with a dynamic compression feature based on the nonlinear behaviour of a MOS capacitor in the feedback network. The integrated charge is reset through the SR switch. The voltage at the preamplifier output is converted to a current by means of a transconductor with enhanced linearity properties. Trapezoidal, time-variant shaping of the signal is performed through a so called flip-capacitor filter, whose operation is based on the appropriate timing of switches S0 to S4. The sample at the channel output is converted to a digital word by means of an A-to-D converter.

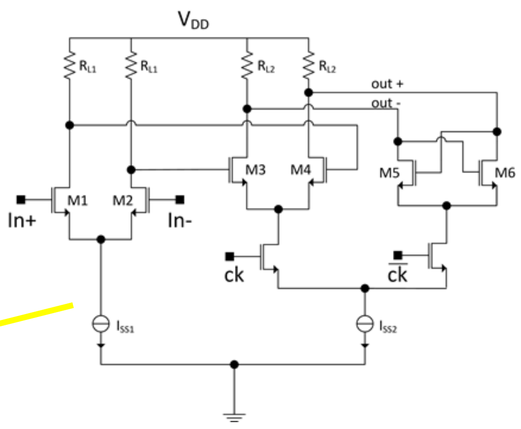
Interleaved SAR ADC

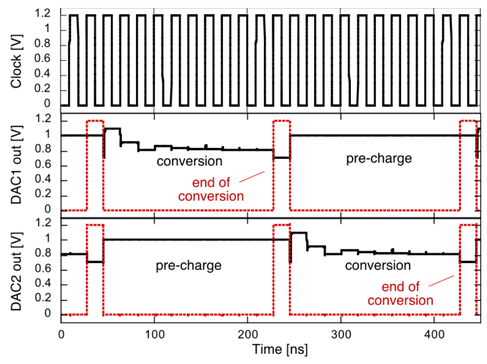
- 10 bits resolution
- Charge redistribution architecture, with a split capacitor approch → $2^{N/2}$ area occupation saving
- A time-interleaved structure serves the purpose of speeding up the ADC operation, while avoiding large current peaks during the charging phase of the capacitive DAC, with the drawback of doubling the area occupation. During each sampling period, one DAC is precharged directly by the output stage of the previous block of the readout channel (the shaper), while the sample stored in the other during the previous sampling period is being converted.



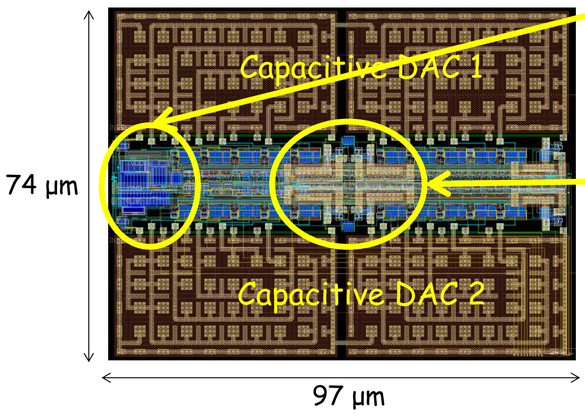
Comparator

The discriminator is a three stage circuit including a preamplification block and a dynamic latched comparator consisting of a second gain stage and a latch.
The dynamic latched comparator suffers from the problem of kickback noise: for this reason, a preamplification stage is added to decouple the noisy dynamic latched comparator input from the split capacitive DAC output.



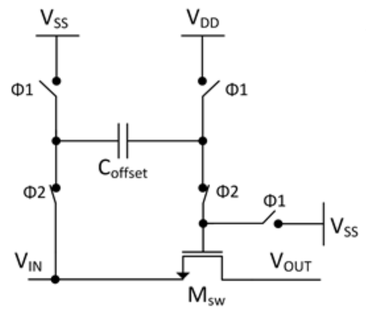


The figure shows the simulation results where the same sample is converted first after storing in one DAC, then in the other at the maximum sampling frequency of 5 MHz. The resulting binary word is read out at the end of the conversion period. At the same time, the end of conversion signal is released.



Power consumption at maximum sampling rate is 85 µW, with a static 70 µW contribution from the discriminator and 15 µW of dynamic power consumption from the SAR logic and DAC switches.

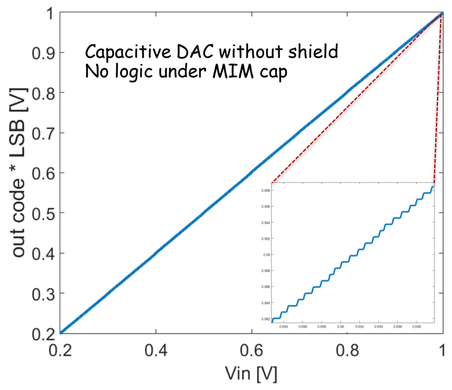
Bootstrap switch



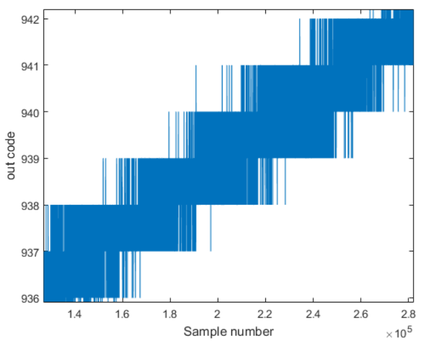
A bootstrap structure ensures a uniform behaviour of the input switch through the whole input range, from 200 mV to 1 V. It works in two non-overlapping phases:

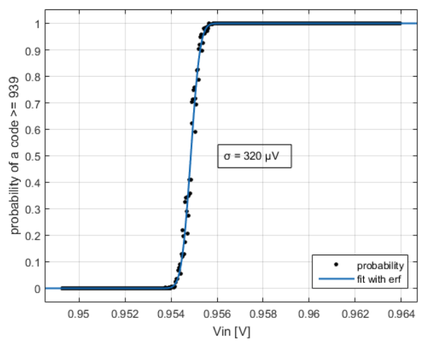
- at first the capacitance C_{offset}, disconnected from the switch transistor M_{SW}, is precharged to V_{DD}.
- than one of its terminals is connected to the input voltage and the other to the gate of M_{SW}, such that the gate-source voltage of the switch transistor, when it is on, is always equal to the voltage across the capacitance (V_{DD}).

Experimental results



- Complete static characteristic through the whole input range.
- Inset showing the final part of the characteristic, where single photon resolution is required for FEL application.
- DNL and INL in that region is less than 0.5 LSB.



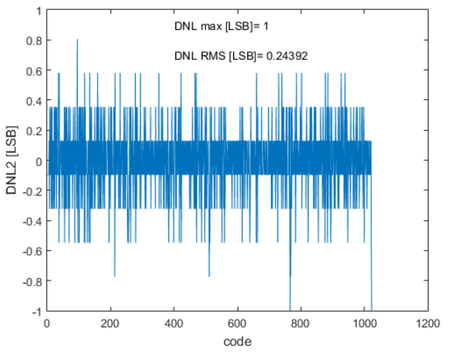


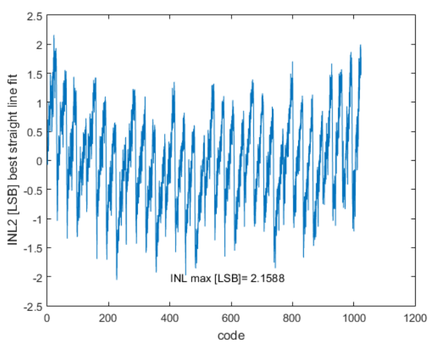
- Input referred noise about 320 µV (~0.4 LSB).
- Probability of having an output code ≥ n

$$P(\text{code} \geq n) = \frac{1}{2} + \frac{1}{2}\text{erf}\left(\frac{V_{in} - V_t}{\sqrt{2}\sigma}\right)$$

V_t = transition voltage from n-1 to n

- Linearity performance measured with a clock conversion of 20 MHz.





Layout version	Area [µm²]	DNL max [LSB]	DNL rms [LSB]	INL max [LSB]
Capacitive DAC shielded; no logic under MIM cap	97 × 74	2,2	0,45	2,1
Capacitive DAC shielded; logic under MIM cap	97 × 58	2,3	0,40	2,4
Capacitive DAC without shield; logic under MIM cap	97 × 58	1,6	0,33	3,6
Capacitive DAC without shield; No logic under MIM cap	97 × 74	1,0	0,24	3,2

Conclusion

- A 10-bit SAR ADC for application to X-ray FEL experiments has been designed with extremely small area and power consumption.
- An interleaved approach has been proposed to speed up the ADC operation and avoid large current peaks during DAC charging phase.
- Different solutions have been integrated to investigate the effects of digital signal switching and metal shielding on the performance of the converter.
- The first static characterization results show that a good performance, with a DNL ≤ 1 LSB and smaller than 0.5 LSB in the single photon resolution region, is obtained for at least one of the four tested versions of the ADC.
- Dynamic characterization of the ADC is in progress.