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The RD53 effort towards the development of a 65 nm CMOS pixel readout chip for extreme data rates and radiation levels

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The next generation of silicon pixel detectors for the phase-II upgrade of ATLAS and CMS at the High Luminosity LHC sets unprecedented requirements to the microelectronic readout systems. Front-end integrated circuits must provide advanced analog and digital functions in pixel readout cells with a pitch of a few tens of a um. Operating at low power dissipation, they must handle huge data rates and stand extreme radiation levels. The community of designers is studying the 65nm CMOS technology as a tool to achieve the ambitious goals of these future pixel systems, and has organized itself in the RD53 project to tackle the challenges associated with mixed-signal design in this process. The tolerance of 65nm CMOS to extreme radiation levels is a major subject of RD53, and this paper will review the current status of radiation effects studies. Various solutions are being explored for analog circuits performing signal amplification and analog-to-digital conversion in the pixel readout cells. RD53 is studying a pixel matrix digital readout architecture that handles huge hit rates in a power-efficient way, delivering data off the chip with a large output bandwidth. RD53 has submitted small prototype chips with the goal of testing various options for the analog cells and for their integration in a mostly digital environment. Test results on these chips provide the basis for future submissions of larger prototypes towards the goal of fabricating a full-scale integrated circuit in 2016.

Collaboration

on behalf of RD53

Summary

The next generation of silicon pixel detectors for the phase-II upgrade of the ATLAS and CMS experiments at the High Luminosity LHC sets unprecedented and extreme requirements to the microelectronic systems that are used to read out the sensors. Front-end integrated circuits have to provide advanced analog and digital signal processing functions in pixel readout cells with a pitch of a few tens of a um. They have to handle huge data rates and stand extreme levels of radiation without degrading their performance. Presently, the community of designers is studying the 65 nm CMOS technology as a tool to achieve the ambitious goals of these future pixel systems, and has organized itself in the RD53 project to tackle the specific challenges associated with the development of readout chips for the innermost pixel layers of experiments at the HL-LHC. This paper is focused on the specific features of the design of these mixed-signal front-end circuits in a nanoscale CMOS process.The tolerance of the 65 nm CMOS technology to the extreme radiation levels of inner pixel layers at HL-LHC is a major subject of RD53, and this paper will review the current status of radiation effects studies, of the understanding of the underlying damage mechanisms and of the design criteria that must be followed to achieve the required degree of radiation resistance. Besides radiation tolerance, the analog front-end circuits in the pixel readout cells have to satisfy low noise and small threshold dispersion requirements, achieving a high hit detection efficiency while taking into account typical constraints such as

low power dissipation and small available silicon area. This paper will provide an overview of the architectures that are currently being explored by RD53 for signal amplification and filtering, hit detection and analog-to-digital conversion. A major requirement is that low-noise amplifying stages have also to be isolated from the mostly digital environment of the chip. The digital readout system of the pixel matrix must handle a huge hit rate in a power-efficient way, delivering data off the chip with a very large output bandwidth. The progress accomplished by RD53 towards the development of the readout architecture of the pixel matrix will be reviewed, with an overview of the novel solutions that can be pursued within a 65 nm CMOS technology. Finally, RD53 has already submitted a first set of small prototype chips with the goal of testing various options for the design of the analog readout cells and for their integration in a mostly digital pixel readout chip. This paper will review the experimental results that RD53 got on these chips, which are providing very useful information in view of the design of a next round of submissions of larger prototypes. The paper will discuss the current plans of RD53 towards the goal of fabricating a full-scale integrated circuit in 2016.

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