A New Front-end ASIC for GEM detectors with Time and Charge Measurement Capabilities

FRONTIER DETECTORS FOR FRONTIER PHYSICS
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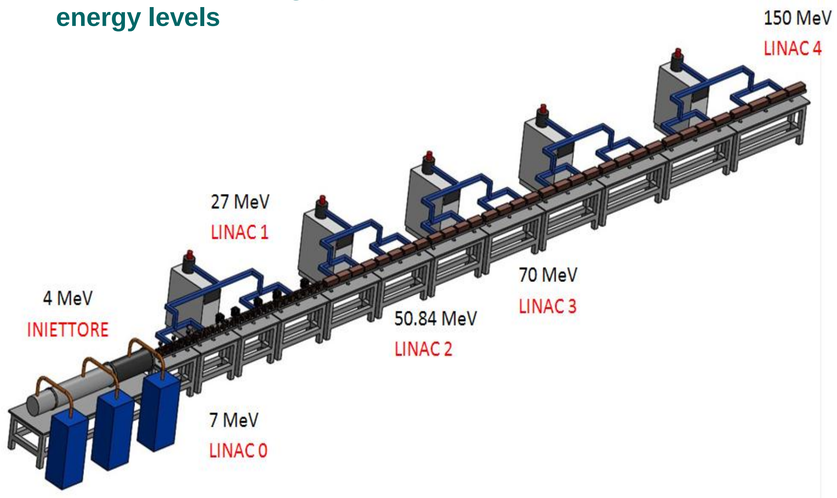
Motivations and purposes

The AMIDERHA project

- Construction of a new proton-therapy facility in the Apulia region
- Based on multi-stage, cascaded LINAC to obtain different energy levels



Beam monitoring

- Accurate system of beam monitoring needed
- Based on Gas Electron Multiplier (GEM) detectors
  - Flexibility in size and geometry
  - High rate capability (up to 50MHz/cm^2)
  - Good spatial resolution (down to 50÷100 μm) and time resolution (down to 4.5 ns)
  - Low mass contribution
  - Large gain with triple GEM structures

Development of the GEM for AMIDERHA: mechanical gas volume

Front-end ASIC for GEM detectors

- Multichannel ASIC needed for compactness and power consumption
- Charge measurement capability, to improve the spatial resolution (charge centroid technique)
- Accurate trigger signal, to allow for coincidence analysis among different GEM layers

ASIC main features

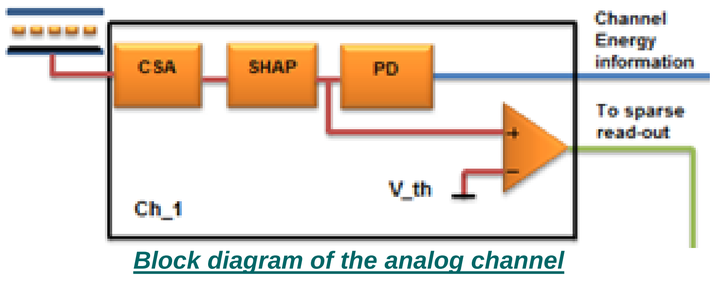
- Technology CMOS AMS 0.35μm
- 32 channels
- Power supply voltage 3.3V
- Integrated 8 bit ADC
- Fast LVDS link for data transfer

Sensitivity	15mV/fC
Dynamic range	80fC
Non-linearity error	< 1%
Equivalent input noise charge (ENC)	< 650e-
Detector capacitance	≅10pF

Main specifications for the GEM front-end

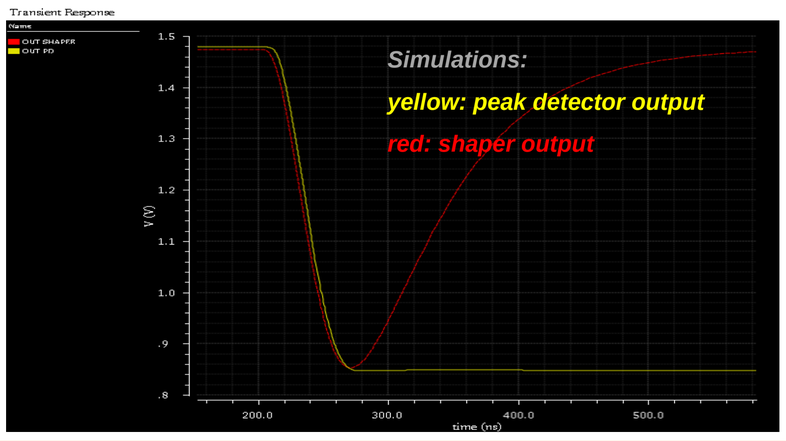
Main building blocks of the ASIC

Analog channel

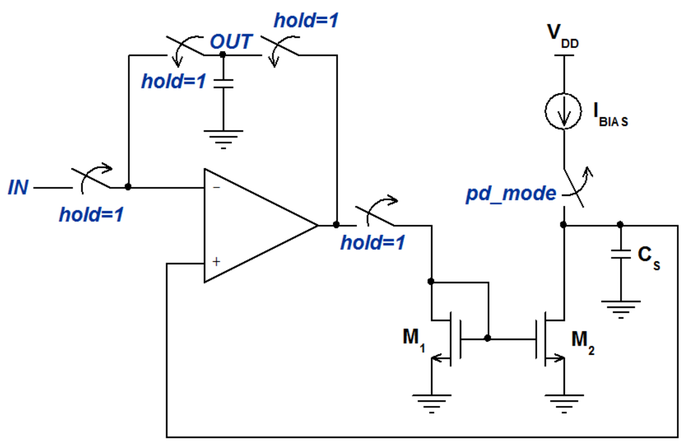


Block diagram of the analog channel

- Classic CSA+shaper front-end structure
- CSA: straight cascode with active reset of the integration capacitance C_F=180fF (PMOS with adjustable bias current)
- Second order shaper with adjustable output baseline, peaking time ≅ 80ns
- Peak detector, working as an analog memory, to store the charge information during the read-out
- Leading edge comparator with adjustable threshold



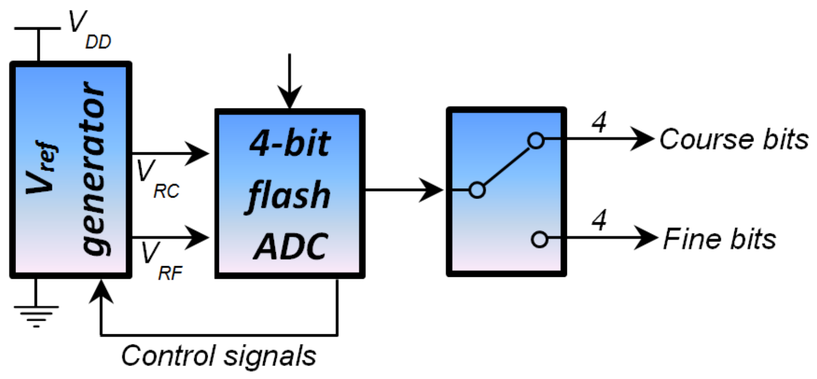
Peak detector



Three operating modes:

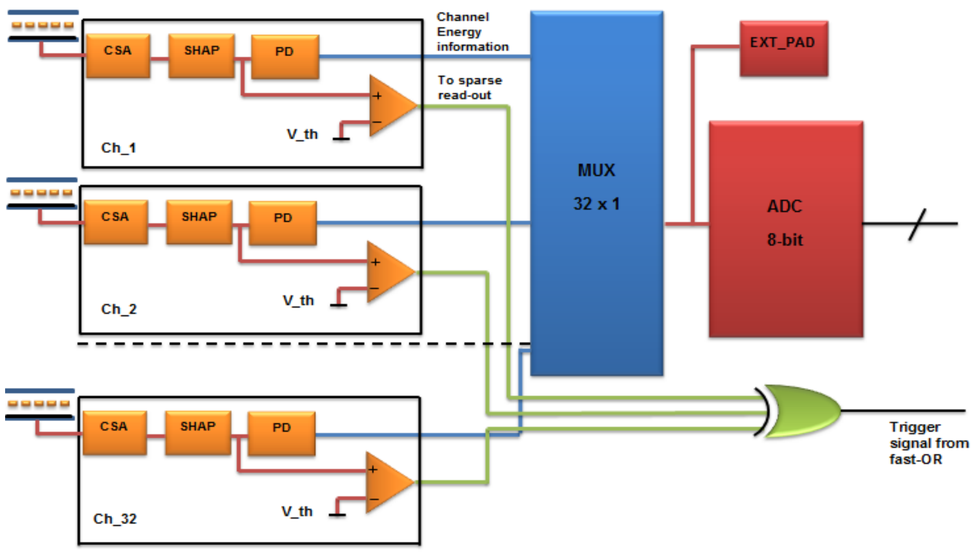
- *pd_mode*=0, *hold*=0: voltage follower mode
  The voltage on C_S follows the input
- *pd_mode*=1, *hold*=0: peak detection mode
  The voltage on C_S tracks the peak of the input
- *pd_mode*=1, *hold*=1: analog memory
  The voltage on C_S is buffered on the output node

Two-step flash, subranging 8-bit ADC



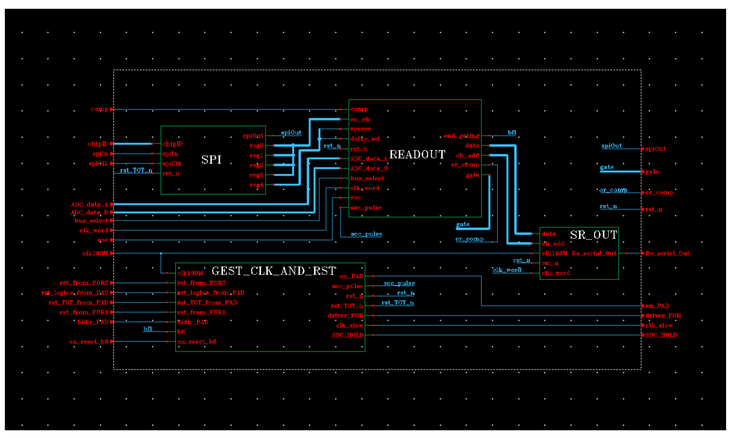
- Two-phase conversion: coarse and fine, exploiting the same comparators and different references V_{RC} and V_{RF}
- Resistor ladder for reference generation
- Two ADC modules working in interleaving: one conversion per clock cycle, maximum conversion rate 20MS/s
- Correction logic for "bubble" errors
- Total power consumption 24mW

Architecture of the ASIC



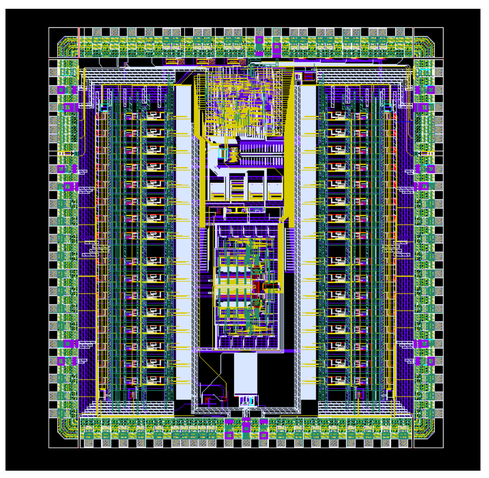
- PD outputs multiplexed to the ADC input
- Trigger formation: fast-OR of the comparator outputs
- Channel maskable through configuration flags
- Internal bias generator based on bandgap reference

Digital part

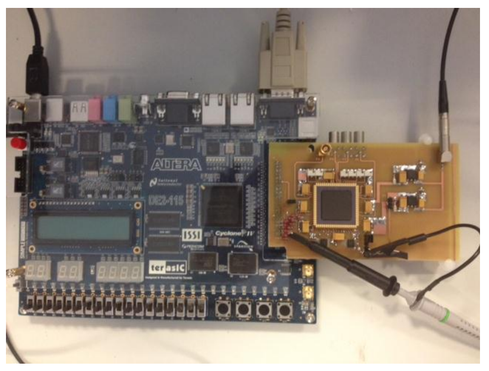


- READOUT: management of the sparse and serial read-out modes
- SPI: configuration interface (two 8-bit DACs, three 10-bit DACs, channel masking, setting of the read-out mode, test mode)
- SR_OUT: data serializer for the 100Mbit/s LVDS output link
- GEST_CLK_AND_RST: clock and reset management

Layout



- 4.6 x 4.9 mm2, package JLCC 84 pins



- ASIC assembled on the test board