A New Front-end ASIC for GEM detectors with Time and Charge Measurement Capabilities

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Motivations and purposes

The AMIDERHA project
- Construction of a new proton-therapy facility in the Apulia region
- Based on multi-stage, cascaded LINAC to obtain different energy levels
- Multichannel ASIC needed for compactness and power consumption
- Peak detector, working as an analog memory, to store the charge information during the read-out
- Good spatial resolution (down to 50 \( \mu \)m)
- Low mass contribution
- Large gain with triple GEM structures
- Two GEST_CLK_AND_RST: clock and reset management

Front-end ASIC for GEM detectors
- Accurate system of beam monitoring needed
- Based on Gas Electron Multiplier (GEM) detectors
  - Flexibility in size and geometry
  - High rate capability (up to 50MHz/cm²)
  - Good spatial resolution (down to 50-100 \( \mu \)m)
  - Low mass contribution
  - Large gain with triple GEM structures
- Accurate trigger signal, to allow for coincidence analysis among different GEM layers
- Technology CMOS AMS
- Large gain with triple GEM structures
- Two ADC modules working in interleaving: one conversion per clock cycle, maximum conversion rate 20MS/s
- Total power consumption 24mW

Main building blocks of the ASIC

Analog channel
- Classic CSA+shaper front-end structure
- CSA: straight cascode with active reset of the integration capacitance \( C_{int} \) (PMOS with adjustable bias current)
- Second order shaper with adjustable output baseline, peaking time \( t_{peak} \) \( \approx \) 80ns
- Peak detector, working as an analog memory, to store the charge information during the read-out
- Leading edge comparator with adjustable threshold

Peak detector
- Three operating modes:
  - \( \text{pd\_mode}=0, \text{hold}=0 \): voltage follower mode
    - The voltage on \( C_1 \) follows the input
  - \( \text{pd\_mode}=1, \text{hold}=0 \): peak detection mode
    - The voltage on \( C_1 \) tracks the peak of the input
  - \( \text{pd\_mode}=1, \text{hold}=1 \): analog memory
    - The voltage on \( C_1 \) is buffered on the output node

Two-step flash, subranging 8-bit ADC
- Two-phase conversion: coarse and fine, exploiting the same comparators and different references \( V_{ref} \) and \( V_{int} \)
- Resistor ladder for reference generation
- Two ADC modules working in interleaving: one conversion per clock cycle, maximum conversion rate 20MS/s
- Correction logic for “bubble” errors
- Total power consumption 24mW

Digital part
- READOUT: management of the sparse and serial read-out modes
- SPI: configuration interface (two 8-bit DACs, three 10-bit DACs, channel masking, setting of the read-out mode, test mode)
- 16R OUT: data serializer for the 100Mbit/s LVDS output link
- GEST_CLK_AND_RST: clock and reset management
- PD outputs multiplexed to the ADC input
- Trigger formation: fast-OR of the comparator outputs
- Channel maskable through configuration flags
- Internal bias generator based on bandgap reference

Layout
- 4.6 x 4.9 mm², package JLCC 84 pins

ASIC assembled on the test board

Development of the GEM for AMIDERHA: mechanical gas volume