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The readout of the upgraded ALICE-ITS

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During the second long shutdown of LHC the ALICE experiment will undergo a major upgrade. As part of this program the current Inner Tracking System (ITS) consisting of six layers of silicon detectors (two pixel, two drift and two strips) will be replaced with a new device comprising seven layers of pixel detectors. The increase to 50 kHz of the peak interaction rate of Pb-Pb collisions, which is planned by LHC, will lead to a combined data rate produced by the ITS of up to 300 Gbit/s.
As part of this program two families of pixel chips based on the TowerJazz CMOS Imaging Process are under development as candidates for use in the future ITS. One of the designed pixel chips is ALPIDE, which implements priority encoder readout. The other one is MISTRAL-O and utilises a rolling shutter solution. Both can operate in the continuous mode, with ALPIDE also supporting the triggered option and will format the output data stream into the same 8-bit serial protocol. This allowed the R&D process of higher level Readout Unit to concentrate on a single solution applicable to both cases. All of the components of the readout chain have been modelled in a system level simulation that has been used to optimise its topology and various parameters like the size of pixel chip buffers and readout link bandwidths.
We will report on the progress of the R&D efforts, test results of hardware components and the overall expected performance of ALICE-ITS readout system.

Collaboration

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