FRONTIER DETECTORS FOR FRONTIER PHYSICS
13th Pisa Meeting on Advanced Detectors

24-30 May 2015 - *La Biodola, Isola d'Elba (Italy)*

Readout of the upgraded ALICE-ITS

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on behalf of the ALICE Collaboration

28th May 2015

Motivation for upgrade and design objectives

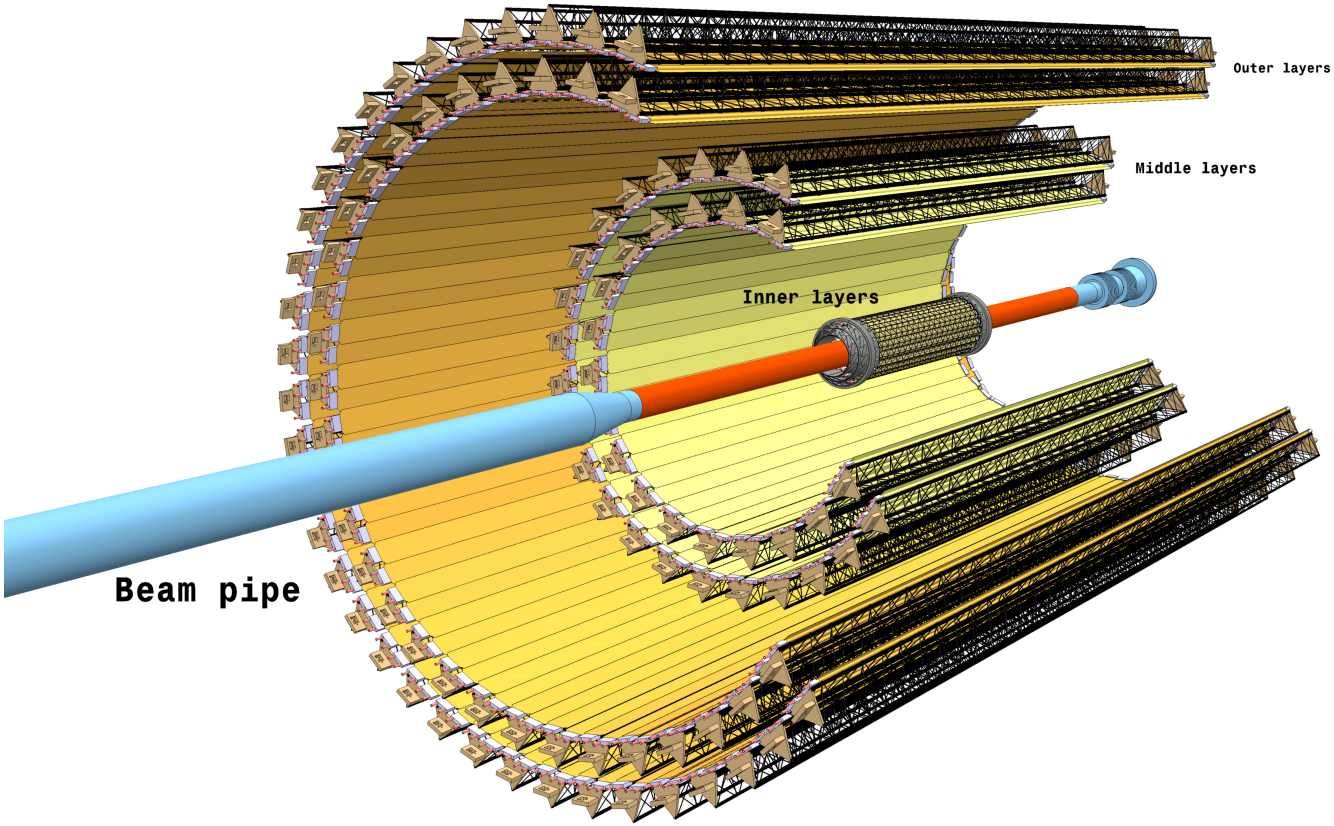
Motivation:

- Precise measurement of Pb-Pb collisions with focus on wide range of observables (with p_T from less than 100 MeV/c to 100 GeV/c)
- Gaining a factor **100** in statistics collected over the combined Run1 (2009-2013) and Run2 (2015-2018) programmes

ITS Design objectives:

- Improving impact parameter resolution by a factor of ~3
- Improving tracking efficiency and p_T resolution at low p_T
- Fast readout of **Pb-Pb** interactions at **>100 kHz** and pp interactions at several 10^5 Hz

New ITS Layout

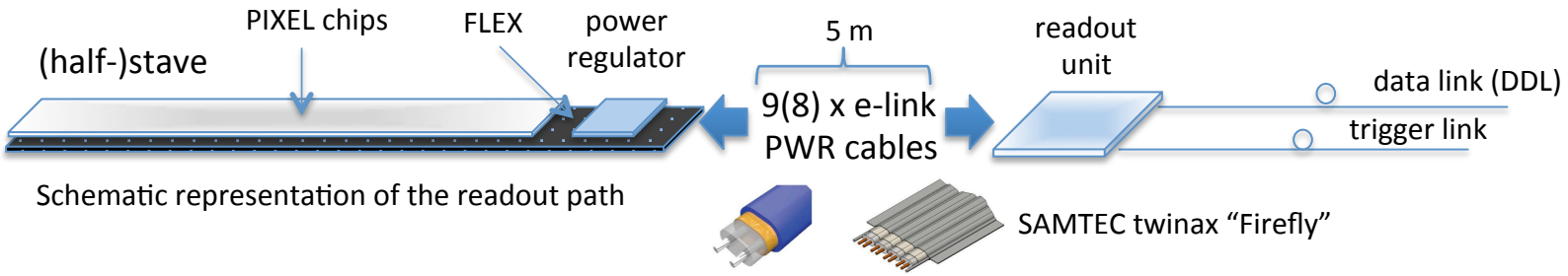


<u>7-layer barrel geometry based on MAPS</u>

- r coverage: 23 – 400 mm
- η coverage: $|\eta| \leq 1.22$ for tracks from 90% most luminous region

- **3** Inner Barrel layers (**IB**)
- **4** Outer Barrel layers (**OB**)
- Material /layer : 0.3% X_0 (IB), 1% X_0 (OB)

Readout – general scheme

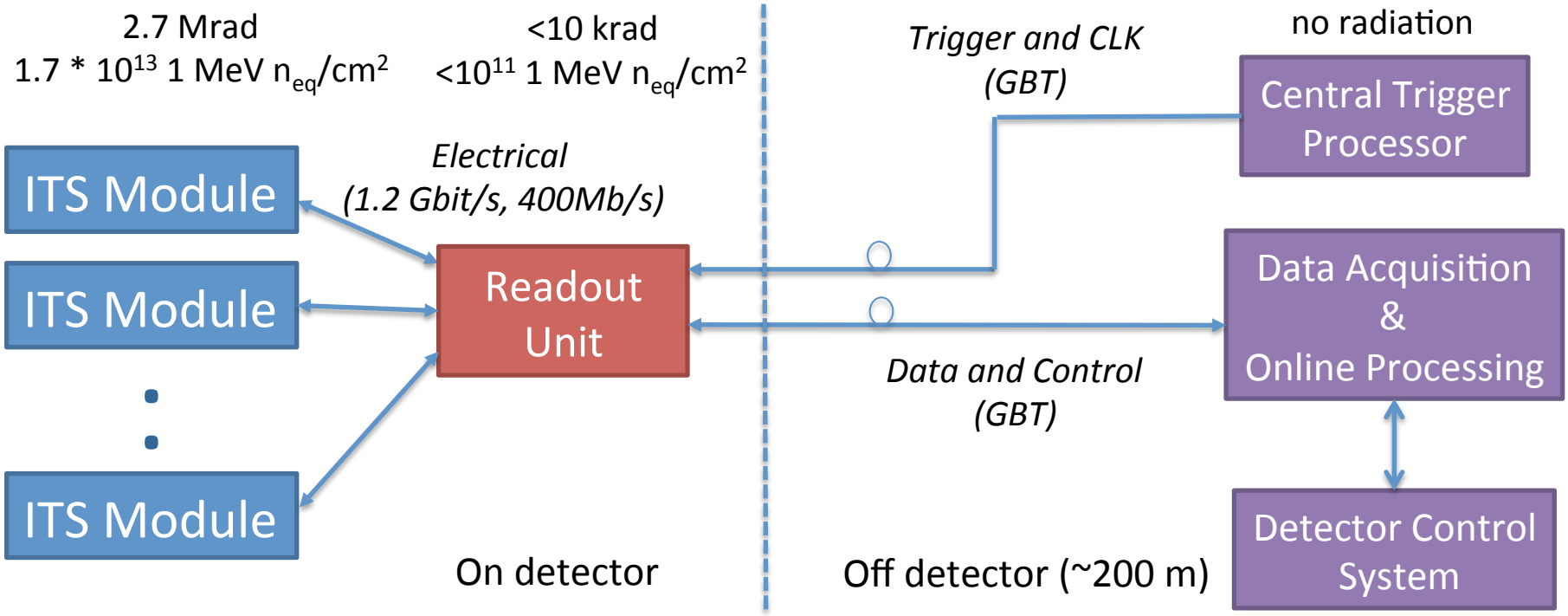


Average data throughput 324 Gbit/s

3816 data, 624 clock, 624 control links

192 * 3 DAQ optical links + 192 Trigger links

GBT – radiation hard optical link



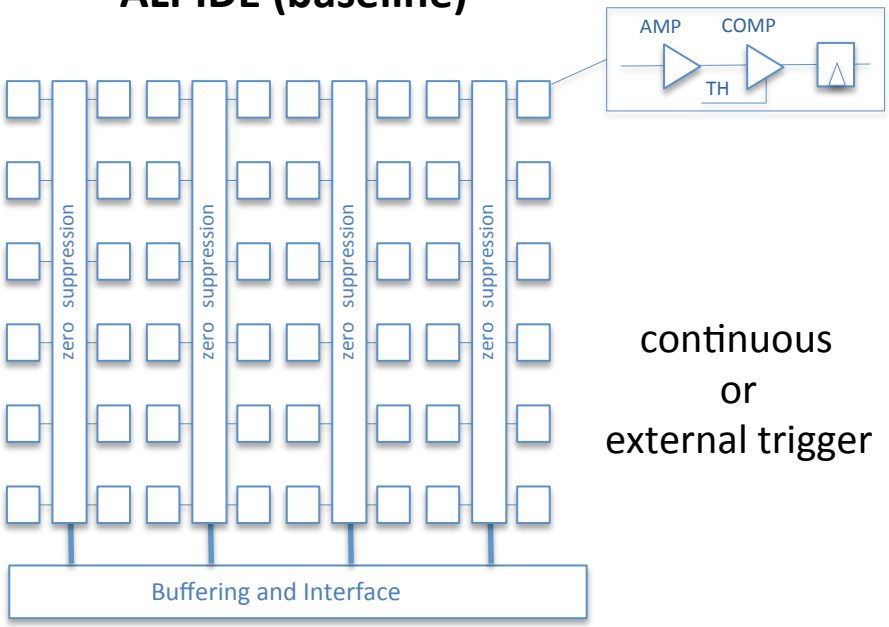
PIXEL Chip – General Requirements

Parameter	Inner Barrel	Outer Barrel
Silicon thickness	50 μm	
Spatial resolution	5 μm	10 μm
Chip dimensions	15 mm x 30 mm	
Power density	< 300 mW/cm^2	< 100 mW/cm^2
Event time resolution	< 30 μs	
Detection efficiency	> 99%	
Fake hit rate	< 10^{-5} per readout frame	
TID radiation hardness (*)	2700 krad	100 krad
NIEL radiation hardness (*)	1.7x10^{13} 1MeV n_{eq}/cm^2	10^{12} 1MeV n_{eq} / cm^2

(*) 10 x radiation load integrated over approved programme (~ 6 years of operation)

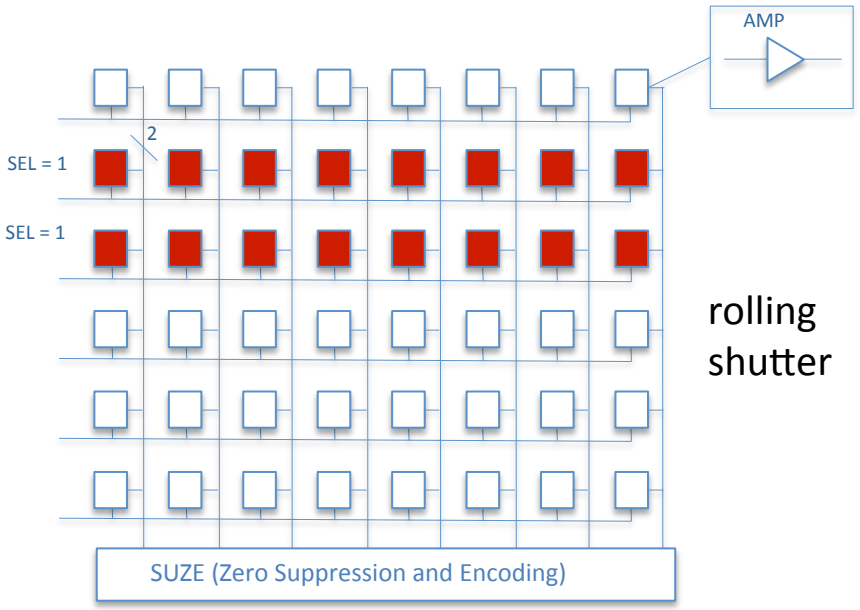
ITS Pixel Chip – two architectures

ALPIDE (baseline)



continuous
or
external trigger

MISTRAL - O



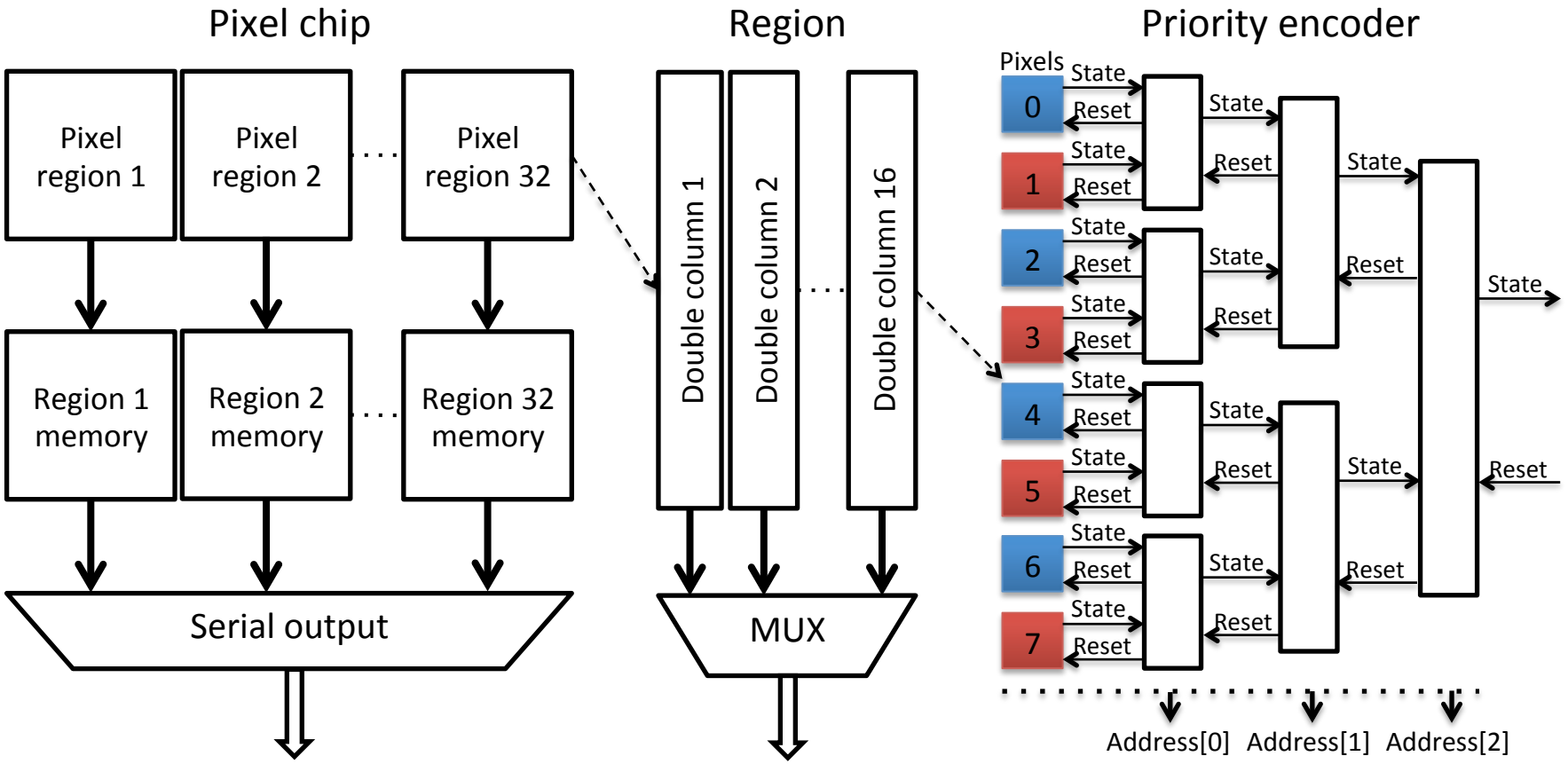
rolling
shutter

Pixel pitch	28μm x 28μm	Pixel pitch	36μm x 64μm
Event time resolution	<2μs	Event time resolution	~20μs
Power consumption	39mW/cm^2	Power consumption$^{(*)}$	97mW/cm^2
Dead area	1.1 mm x 30mm	Dead area	1.7 mm x 30mm

ALPIDE and MISTRAL-O have same dimensions (15mm x 30mm), identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

$^{(*)}$ might further reduce to 73mW/cm^2

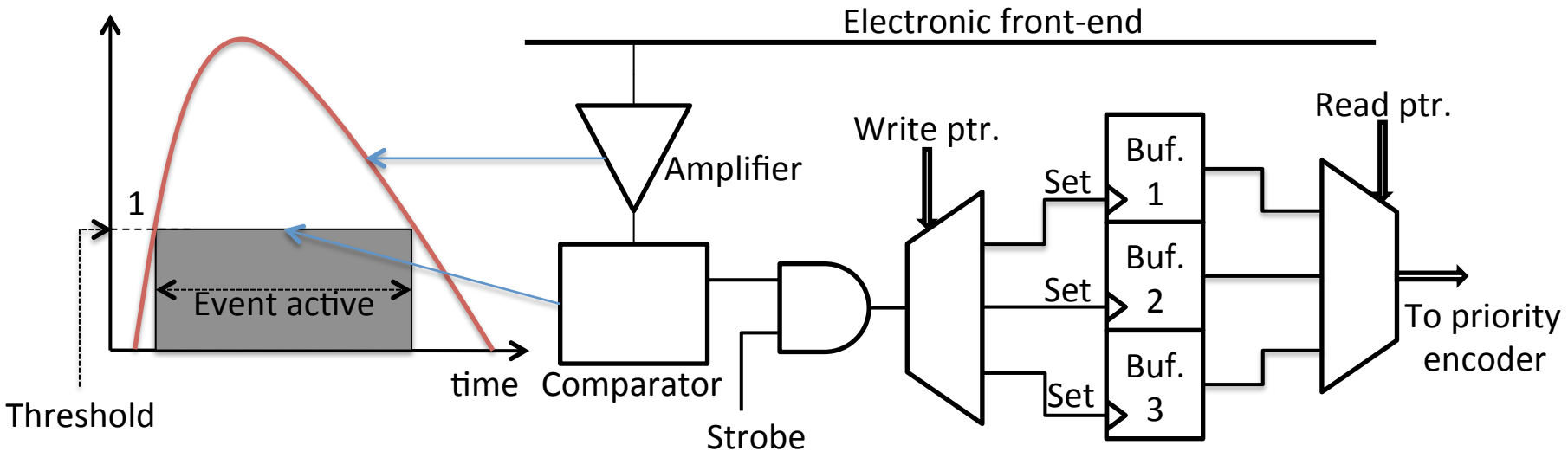
ALPIDE readout



- Regions of 32 columns and 512 rows
- Regions are read out in parallel
- The data is buffered in the memories
- The memories are multiplexed and connected to a serializer

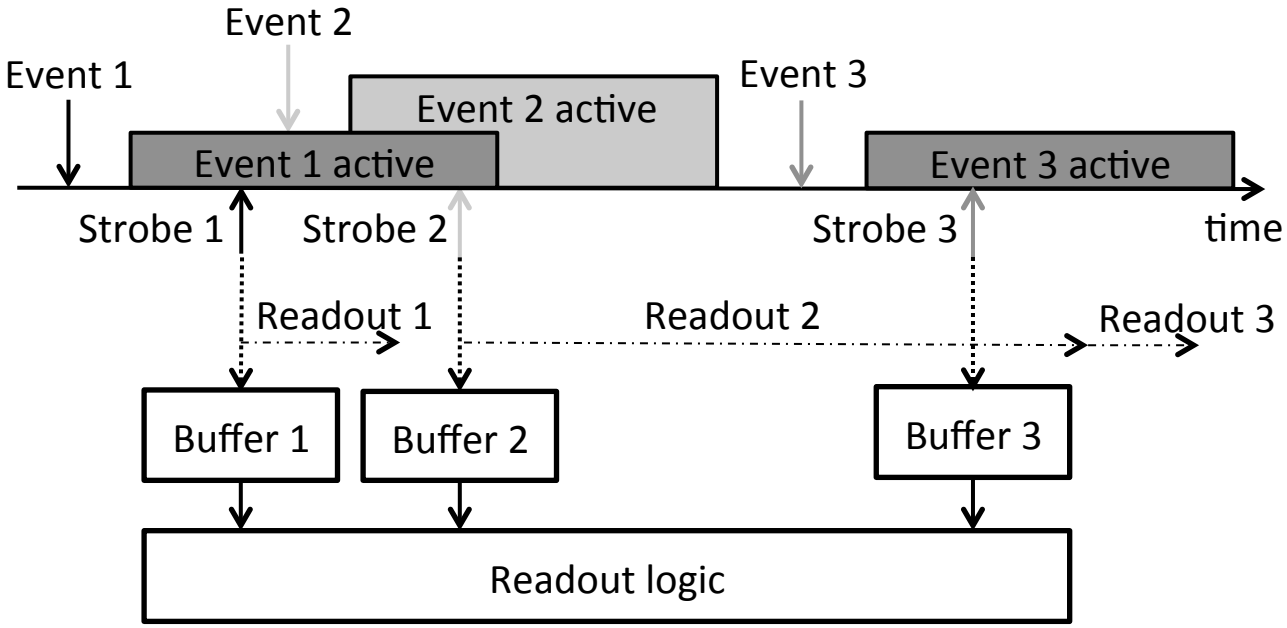
- The addresses of fired pixels are generated hierarchically
- The address is read and the pixel is reset
- No free-running clock in the priority encoder

ALPIDE pixel cell



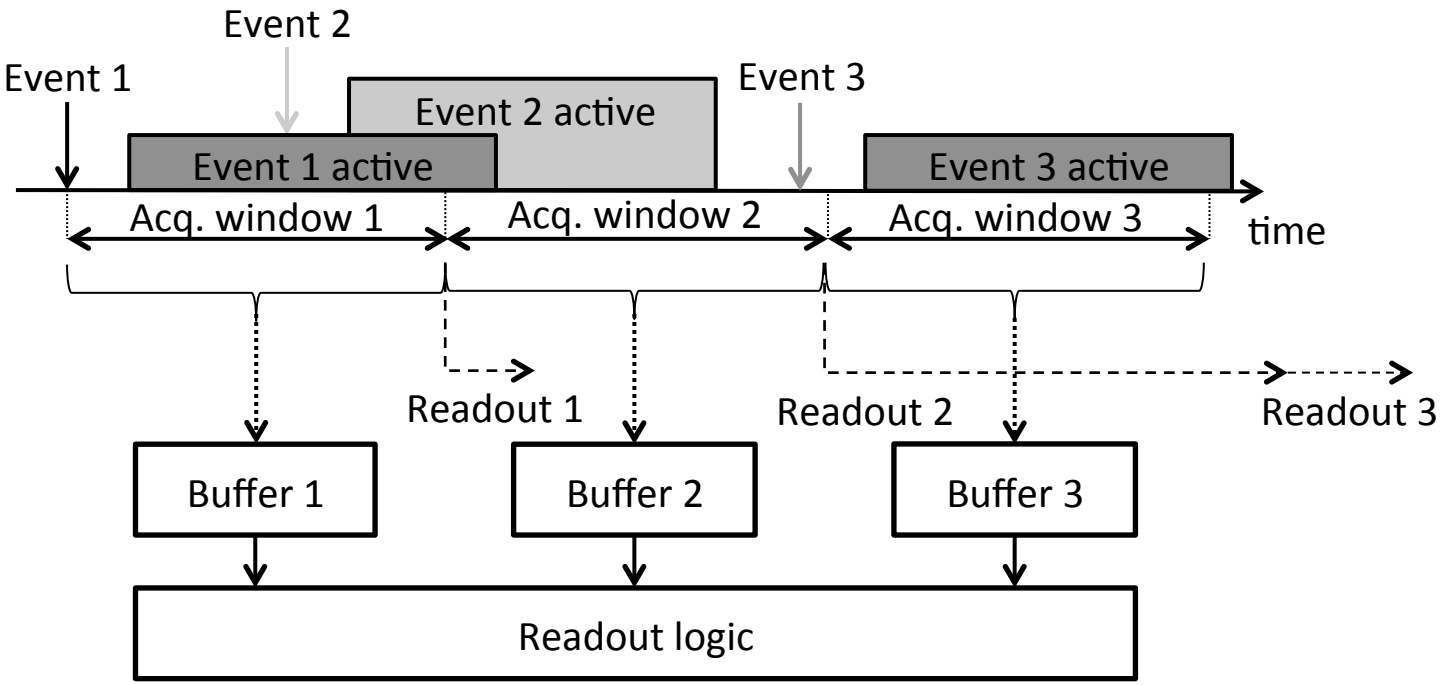
- Front-end serves as analogue memory
- Pixel cells contain 3 level-deep multiple event memory
- When the strobe signal is asserted the state of the output of the comparator is latched in one of the buffers
- If the buffer is active it is passed to the zero suppression circuit (priority encoder)
- Readout time depends on event multiplicity

ALPIDE triggered mode



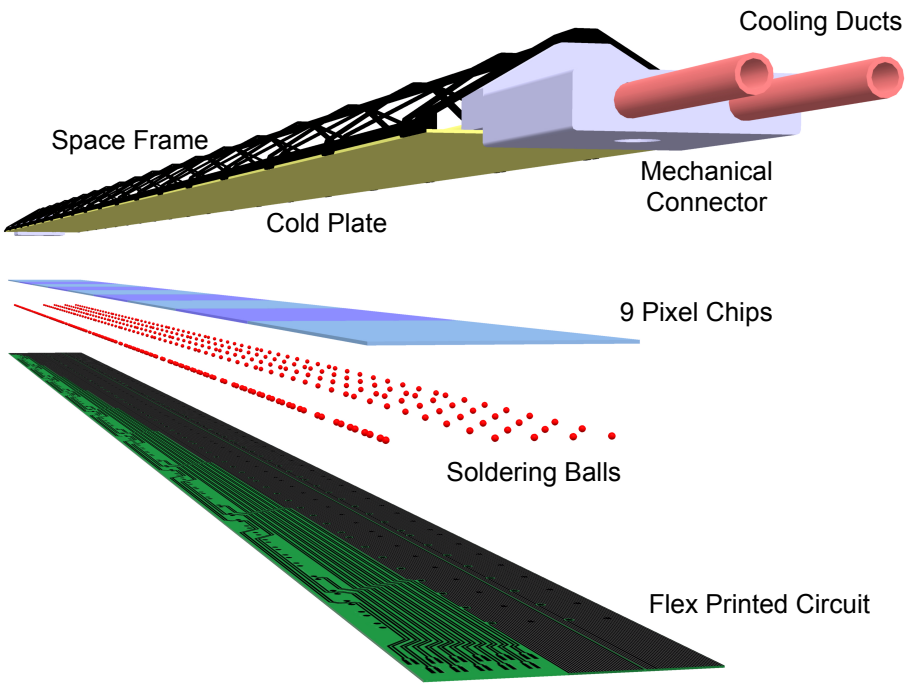
- The system is triggered by an external signal (CTP)
- Event active time depends on the threshold setting of the in-pixel comparator
- When the strobe is generated the state of the front-end is stored in one of the front-end buffers
- The readout is performed on a snapshot of the state of the whole front-end taken at the moment of the strobe
- Events may be recorded and read out multiple times

ALPIDE continuous mode

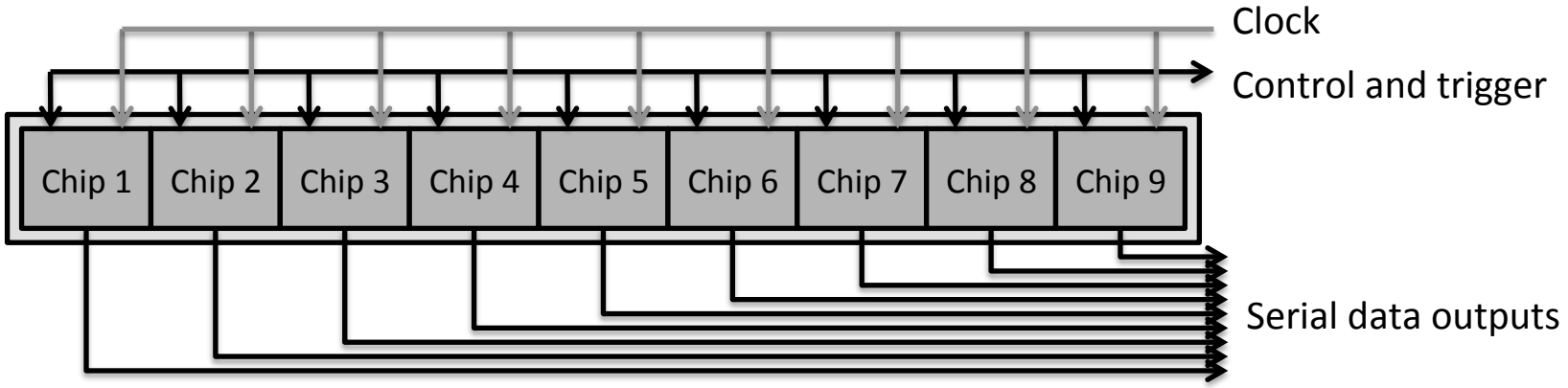


- The strobe signal is asserted for a configurable amount of time (acquisition window)
- All the pixels fired during that time will be stored in one of the front-end buffers
- The readout of those snapshots begins after the strobe signal is deasserted
- Events may be recorded and read out multiple times

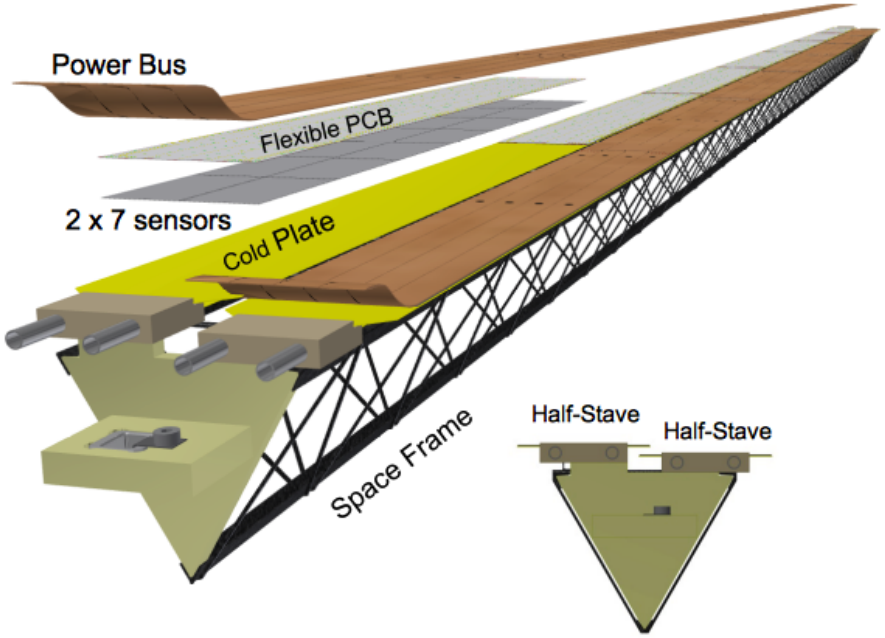
Readout – inner layers



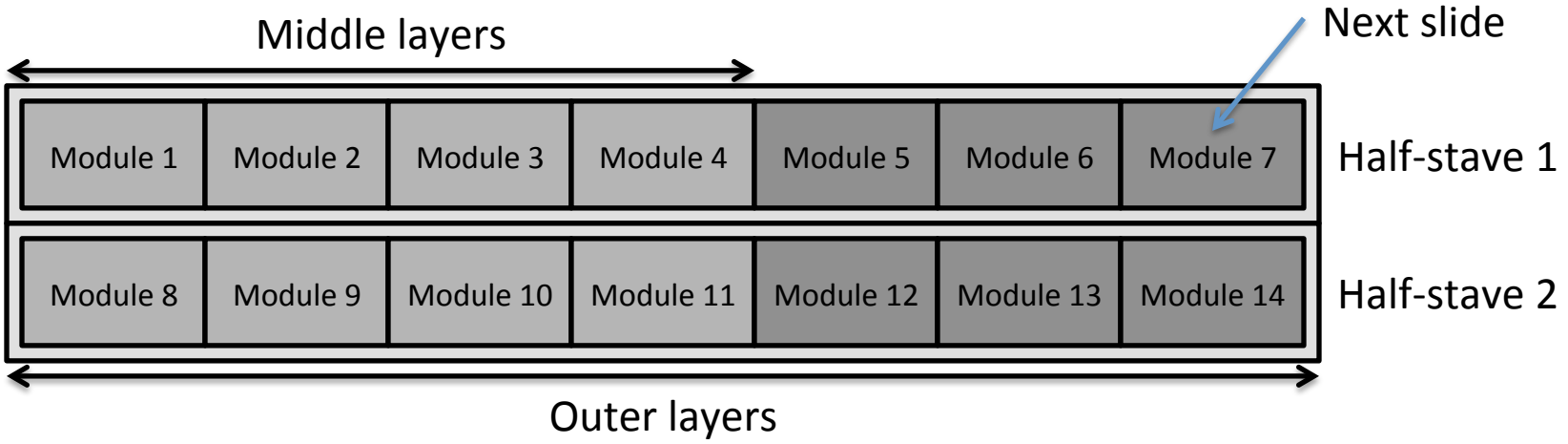
- 3 layers with 12, 16 and 20 staves
- Radial positions (mm): 23, 31, 39
- 9 chips per stave
- Separate serial link for each chip with available bandwidth of 1.2 Gbit/s (including 8b/10b encoding)
- One link per stave for clock distribution
- One link per stave for control and trigger commands



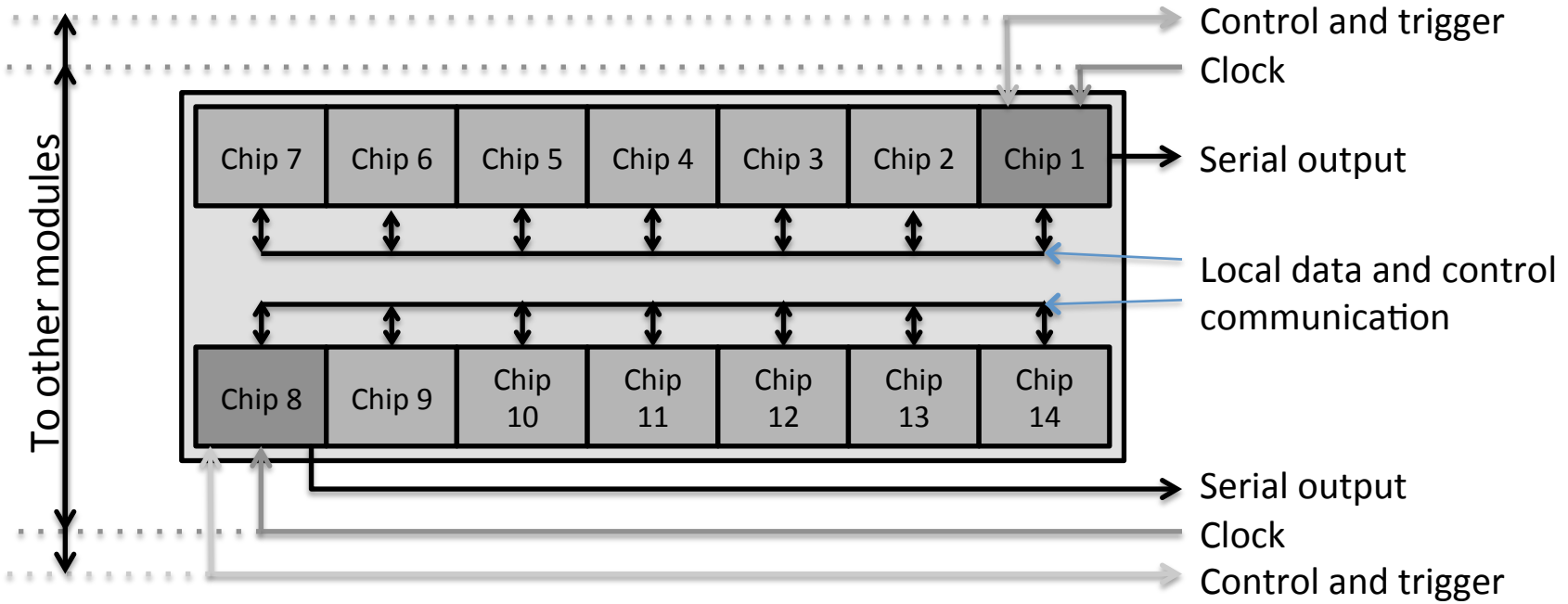
Readout – middle and outer layers



- 4 layers with 24, 30, 42 and 48 staves
- Radial positions (mm): 194, 247, 353, 405
- Layers 3 and 4 consist of 2 rows of 4 readout modules
- Layers 5 and 6 consist of 2 rows of 7 readout modules
- Staves consist of modules of 2x7 pixel chips

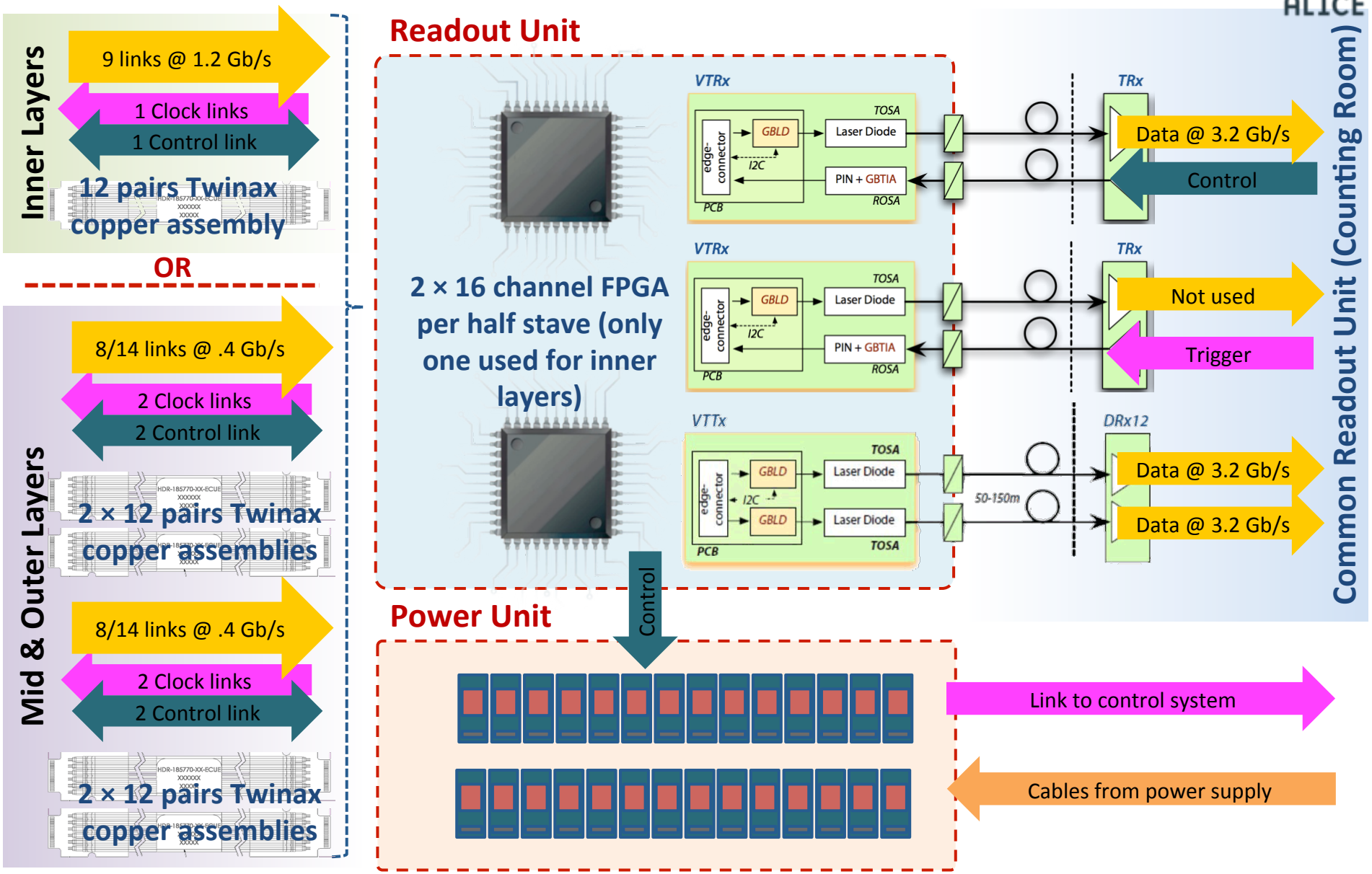


Outer barrel readout module



- Each module contains 2 half-modules (rows)
- Each half-module has one master chip responsible for communication with the Readout Unit
- Chips inside the half-module share the local bus to send out their data, the master chip serves as pass-through
- Control and clock lines are shared by all master chips in a row
- The output serial link is dedicated for a half-module, bandwidth is 400 Mbit/s (including 8b/10b encoding)

Readout Unit

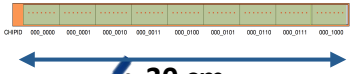


Readout – copper links

12 pairs Twinax copper assembly

Readout Unit

Inner layers (0, 1, 2) staves:



≈ 30 cm

1 assembly

≈ 5m

9 copper pairs, 1.2 Gb/s each, 1 clock, 1 control

16 copper pairs, 400 Mb/s each, 4 clock, 4 control

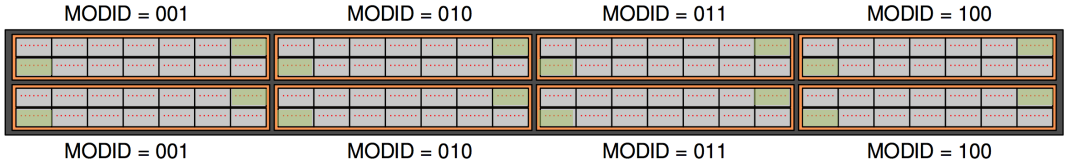
CRU

≈ 5m

2 or 4 assemblies

4 assemblies

Mid layers (3, 4) staves:

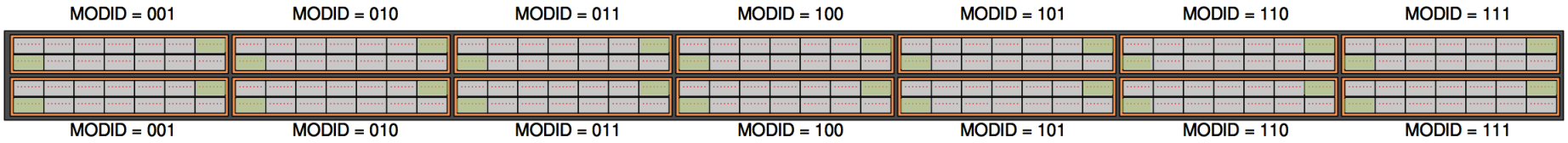


≈ 80 cm

28 copper pairs, 400 Mb/s each, 4 clock, 4 control

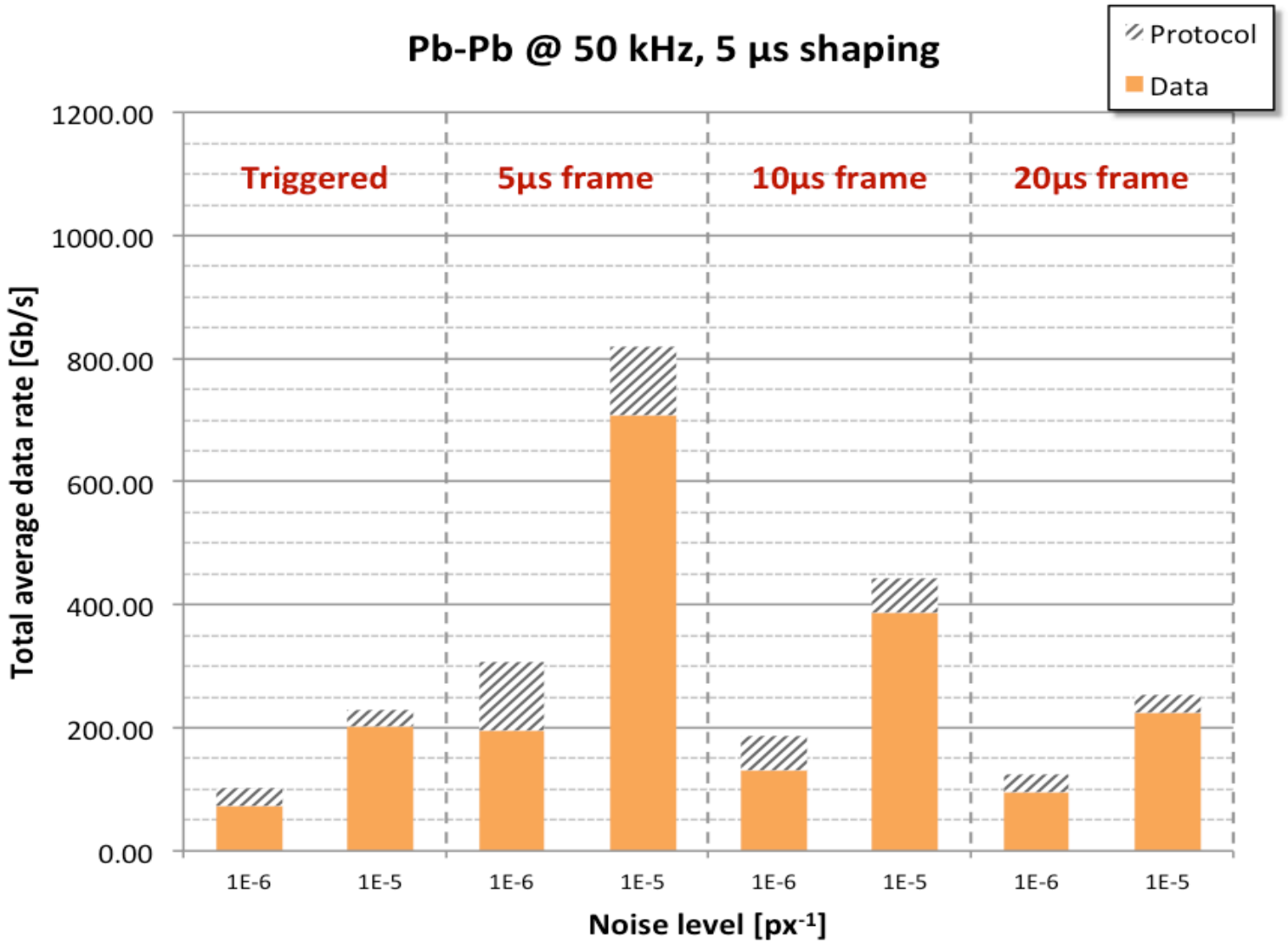
≈ 5m

Outer layers (5, 6) staves:

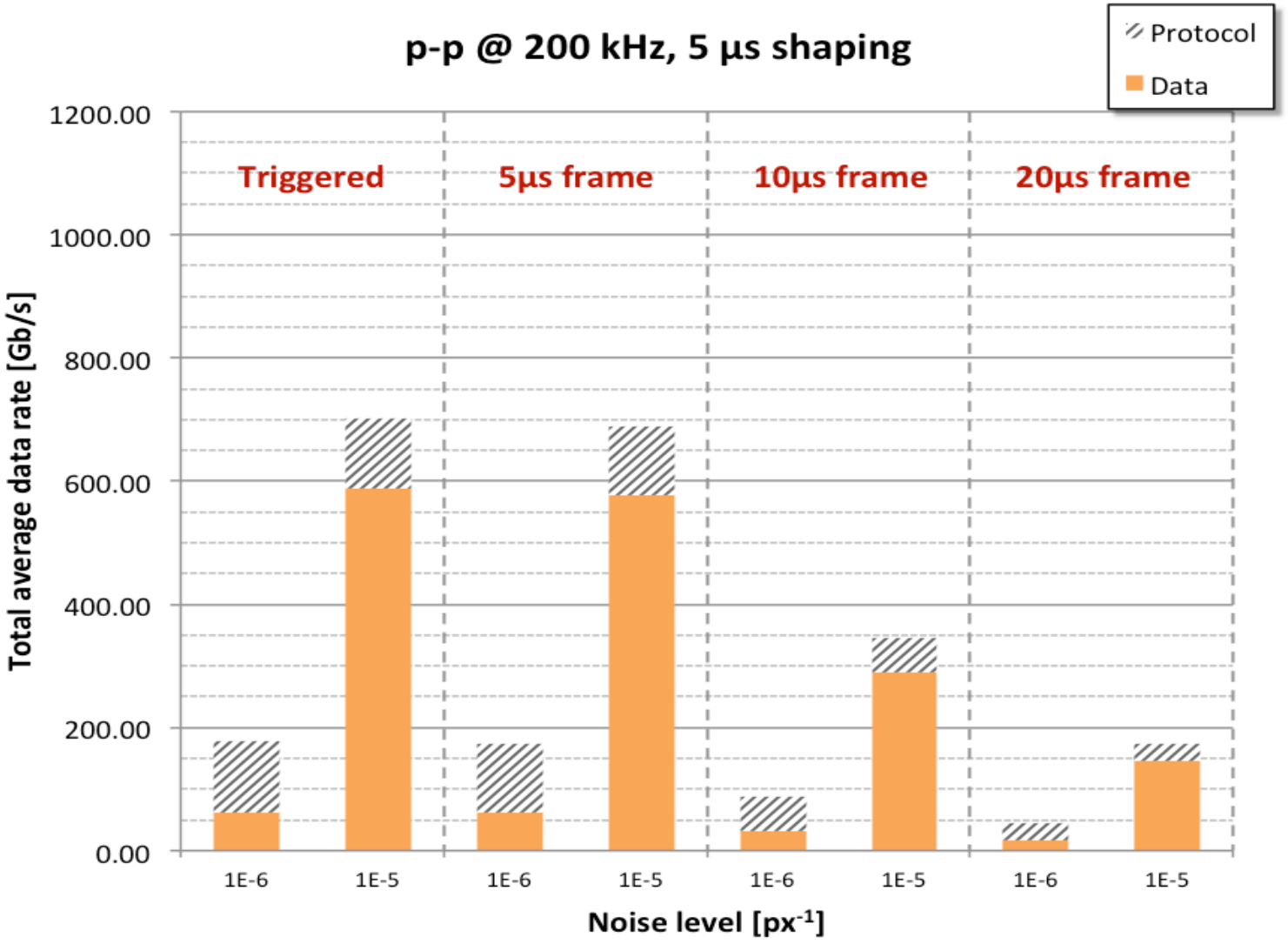


≈ 150 cm

Expected Pb-Pb data rates (50 kHz)



Expected pp data rates (200 kHz)



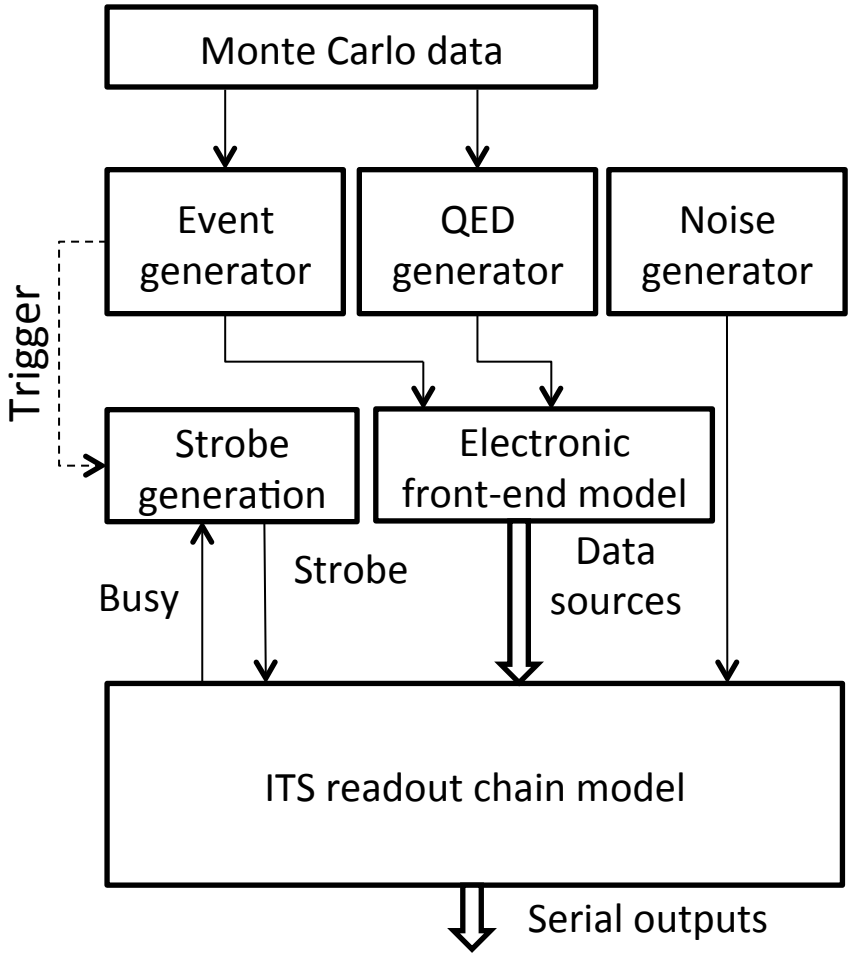
Summary and outlook

- Major upgrade aiming at installation during the Long Shutdown 2 (2018-2019)
- Fast readout of Pb-Pb events at >100 kHz in continuous and/or triggered mode
- New ITS layout using pixel detectors
- Two families of pixel chips:
  - ALPIDE – priority encoder readout
  - MISTRAL-O – rolling shutter
- Dedicated Readout Unit is under development for the ITS
- The R&D process of the components will continue until the end of 2015

Thank you

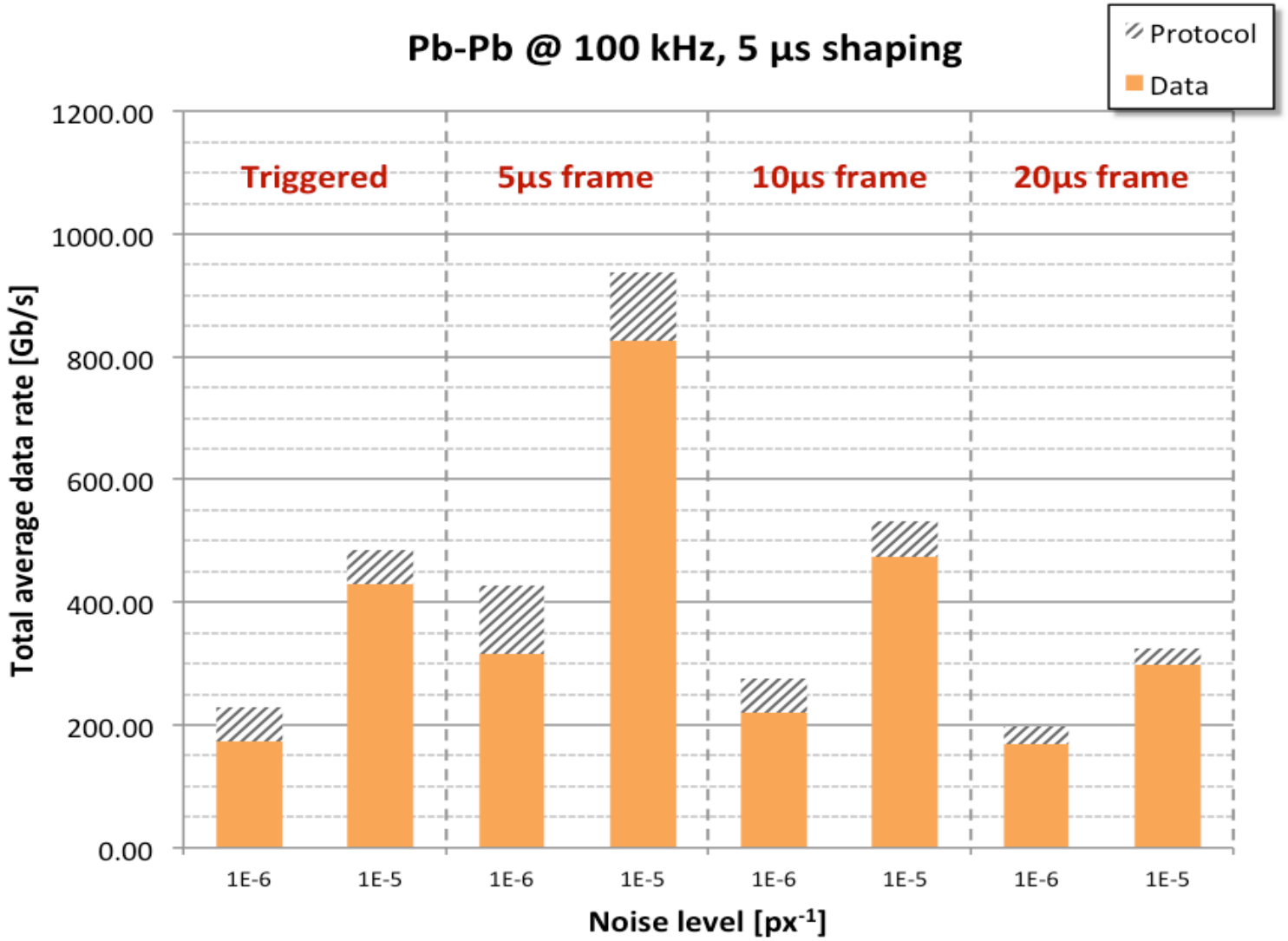
Backup slides

Performance simulations

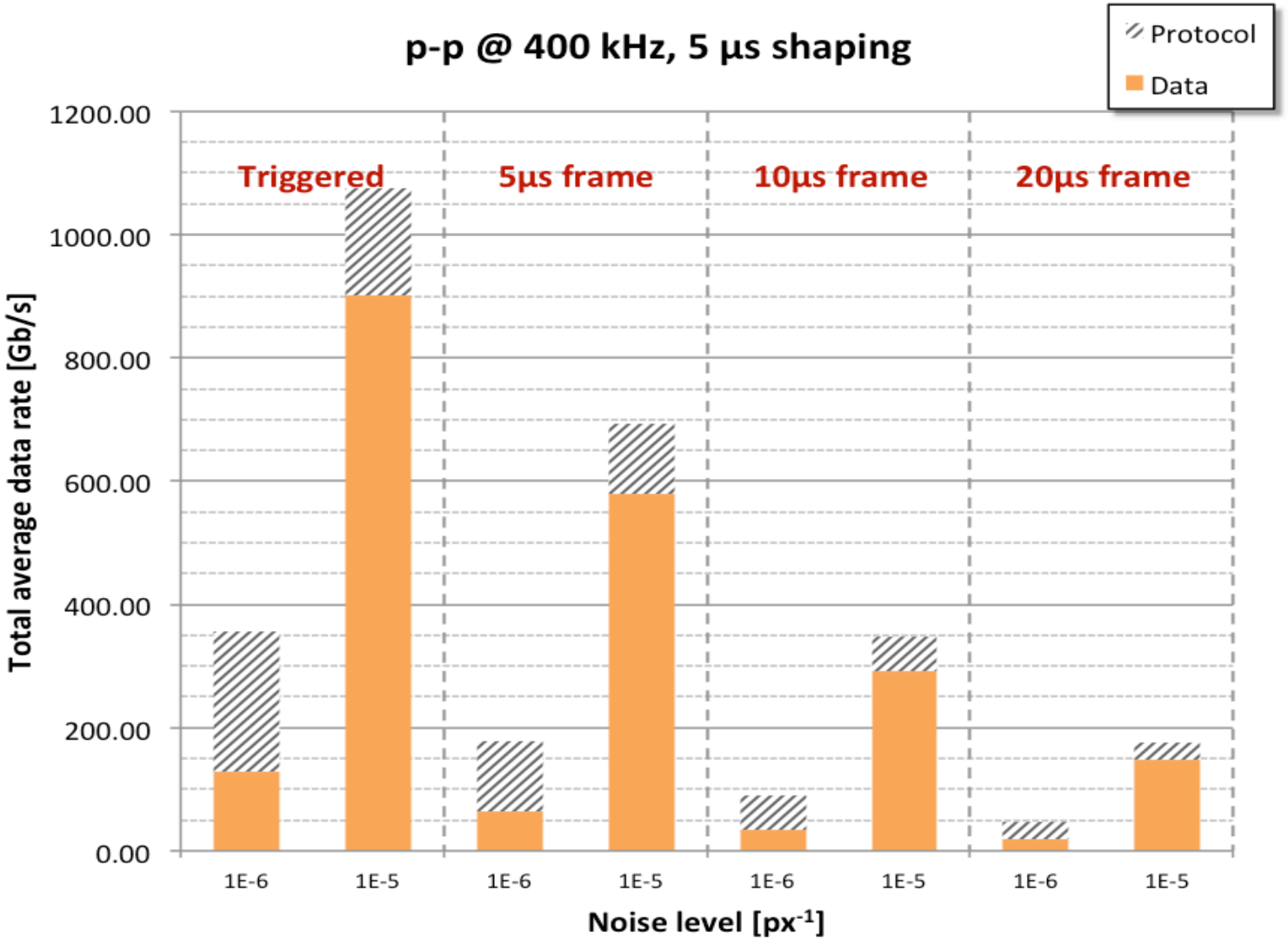


- Detailed model of data acquisition and readout chains
- Implementation uses SystemC library and simulator
- Pb-Pb, QED and pp Monte Carlo data is used as input
- Poisonnian event distribution
- Noise is discrete at strobe assertion

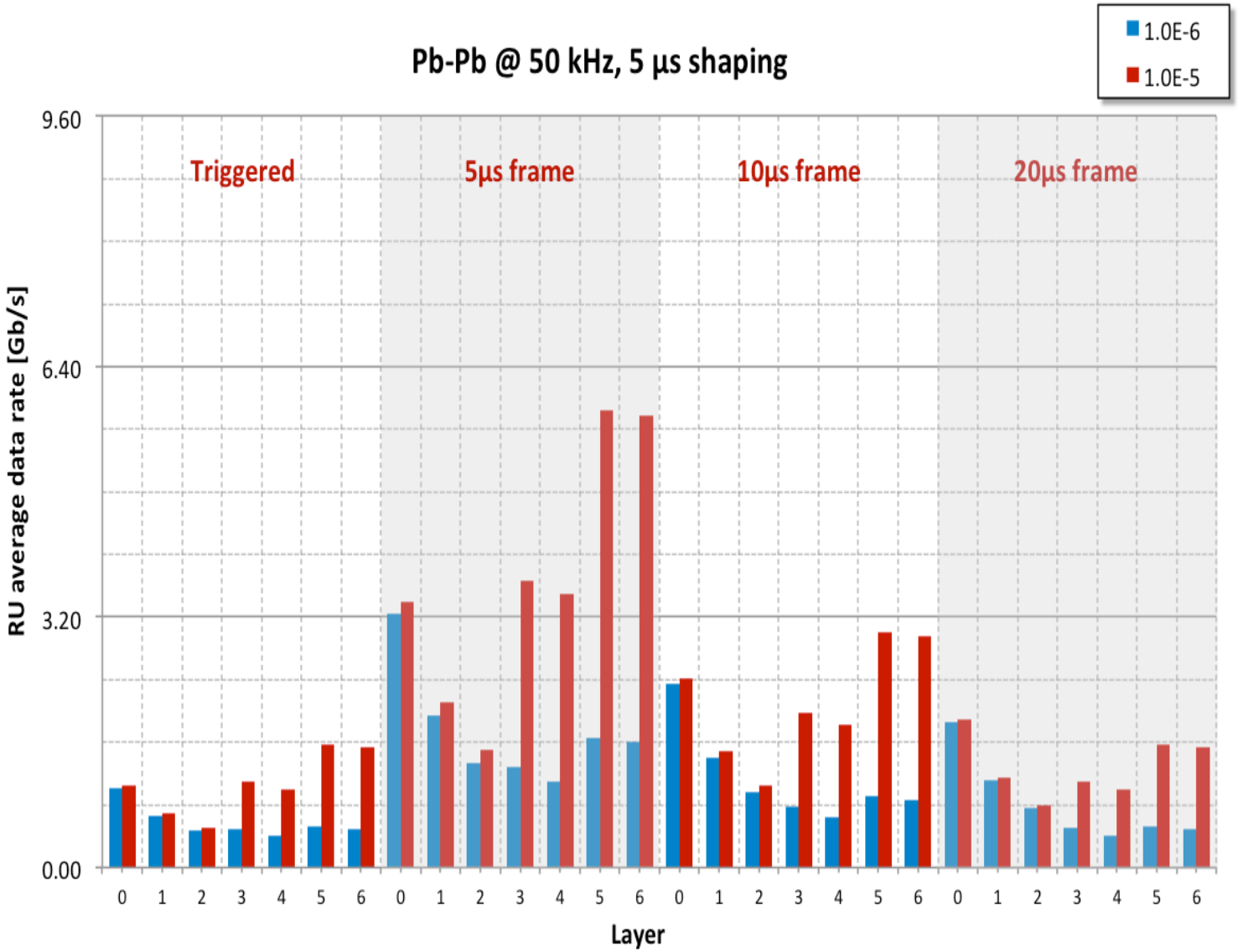
Expected Pb-Pb data rates (100 kHz)



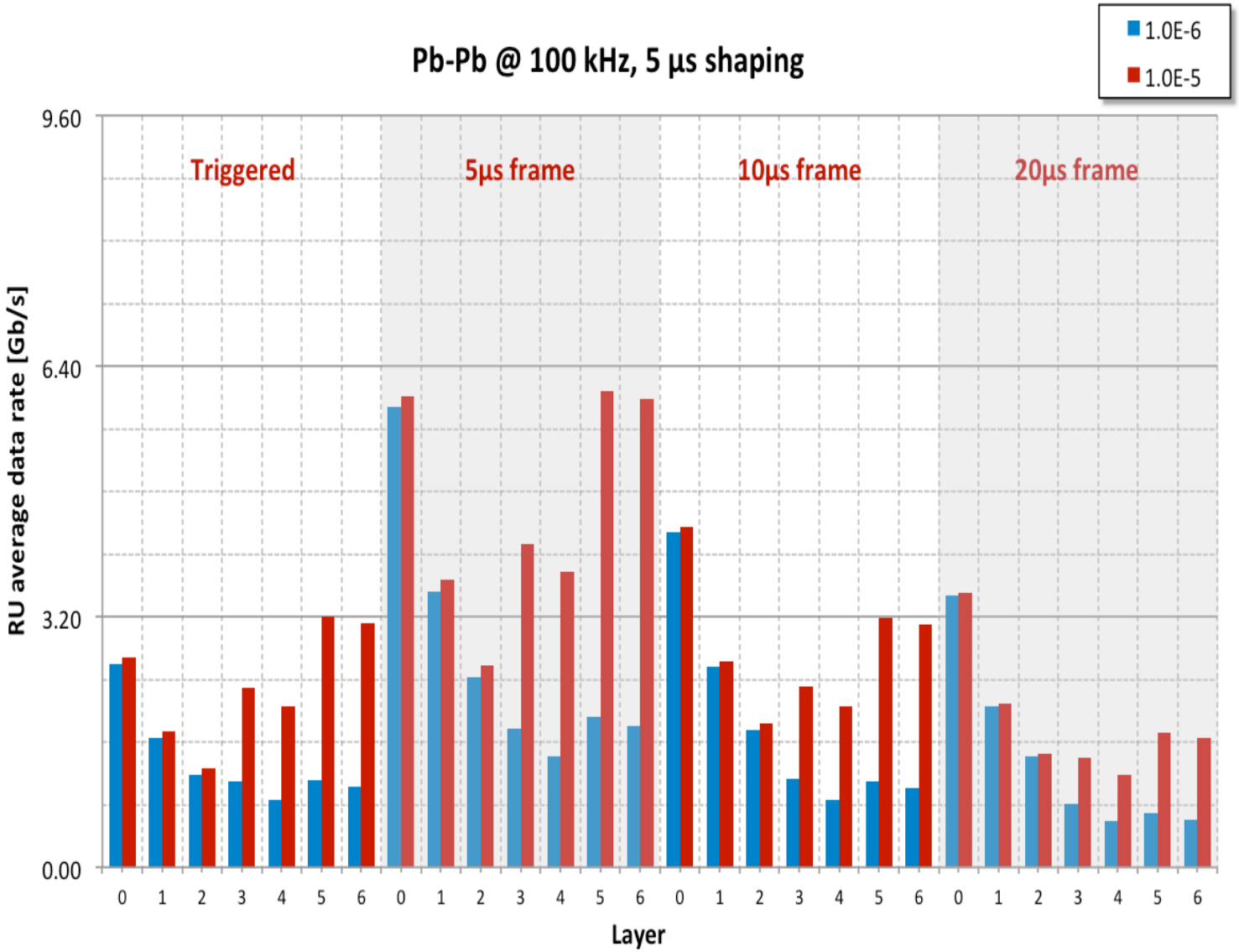
Expected pp data rates (400 kHz)



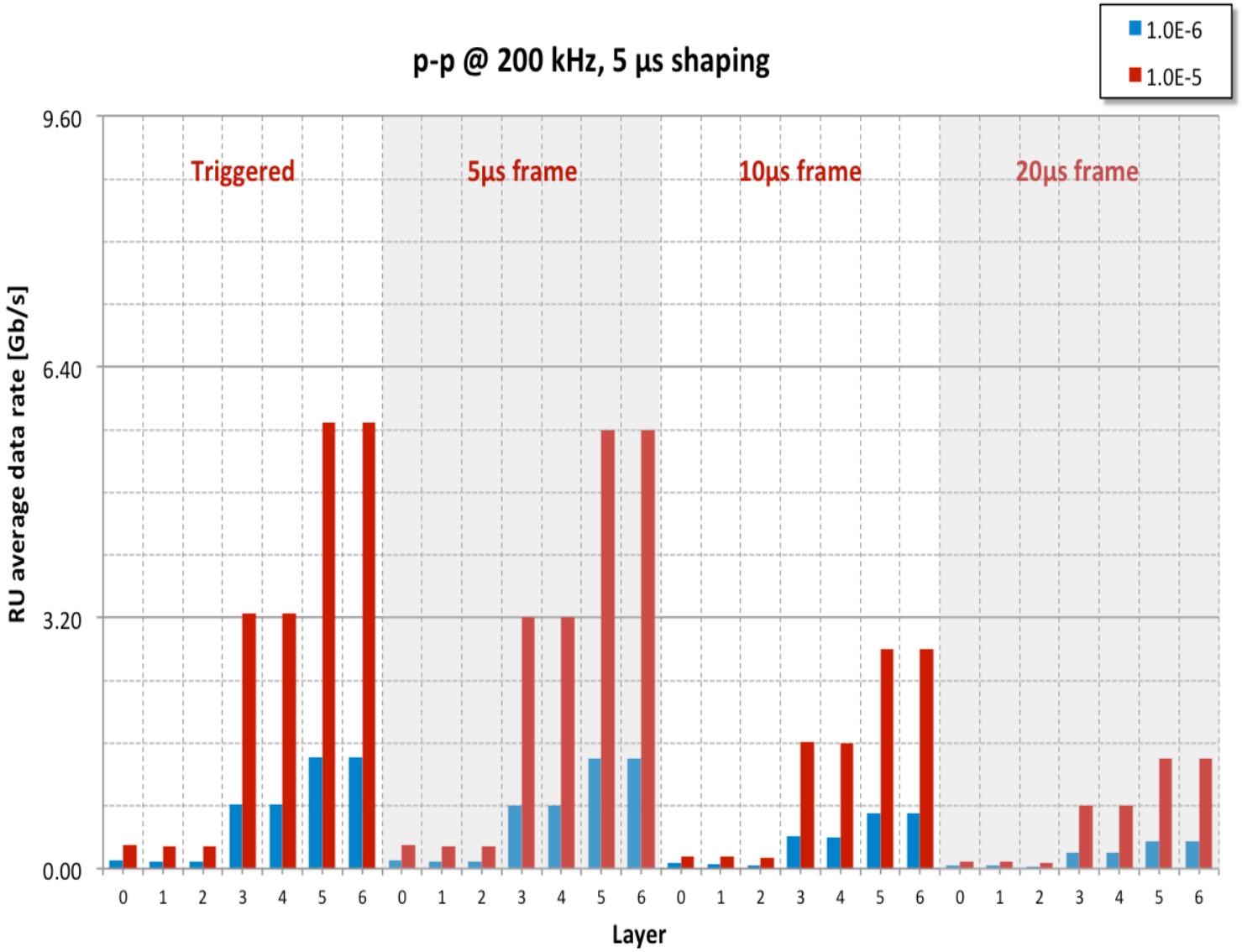
Expected Pb-Pb data rates, layer breakdown (50 kHz)



Expected Pb-Pb data rates, layer breakdown (100 kHz)



Expected pp data rates, layer breakdown (200 kHz)



Expected pp data rates, layer breakdown (400 kHz)