## FRONTIER DETECTORS FOR FRONTIER PHYSICS <br>> 13th Pisa Meeting on Advanced Detectors <br>>



Contribution ID: 288

Type: Poster

## Radiation testing campaign results for understanding the suitability of FPGAs in detector electronics

Thursday, 28 May 2015 17:42 (0 minutes)

SRAM based Field Programmable Gate Arrays (FPGAs) have been rarely used in High Energy Physics (HEP) due to their sensitivity to radiation. The last generation of commercial FPGAs based on 28 nm feature size and on Silicon On Insulator (SOI) technologies are more tolerant to radiation to the level that their use in front-end electronics is now feasible.

FPGAs provide re-programmability, high-speed computation and fast data transmission through the embedded serial transceivers. They could replace expensive custom application specific integrated circuits in front end electronics in locations with moderate radiation field. The use of a FPGA in HEP experiments is only limited by our ability to mitigate single event effects induced by the high energy hadrons present in the radiation field.

In this paper, we summarize results of a two-year study of Xilinx 7-series devices on their susceptibility to a HEP experiment radiation field. Experimental results from irradiation campaigns in the USA and Europe on ionizing dose studies up to 300 krad, and single event effects measurements performed with high-energy neutrons up to 1x10exp11 n/cm2 and protons up to 1x10exp13 p/cm2, will be presented.

After the proton exposure, the devices tested presented no permanent operational failure except for a 10% increase in the core-logic power consumption, well within the component specification.

To mitigate single event upsets we have implemented techniques such as Triple Module Redundancy (TMR) and soft error scrubbing. The effectiveness of these implementations will be presented in detail.

The paper also describes the various errors detected in the FPGA Multi Gigabit Transceivers (MGT). The estimated lane error rate suggests that the configurable logic that interfaces with the MGT is the most sensitive part of the FPGA. Proper application of mitigation methods, however, can significantly reduce this sensitivity. Future experiments are planned with improved TMR and scrubbing mitigation.

## Collaboration

Alessandra Camplani, Mauro Citterio, Chiara Meroni, Istituto Nazionale di Fisica Nucleare (INFN) Milano, Via G. Celoria 16, 20133 Milano, Italy

Matthew Cannon, Michael Wirthlin, NSF Center for High-Performance Reconfigurable Computing (CHREC), Department of Electrical and Computer Engineering, Brigham Young University, Provo, UT 84602, USA

Hucheng Chen, Kai Chen, James Kierstead, Helio Takai, Physics Department, Brookhaven National Laboratory, Upton, NY 11973-5000, USA

Binwei Deng, Chonghan Liu, Tiankuan Liu, Jingbo Ye, Southern Methodist University, Dallas, TX 75275-0100, USA

Primary author: Dr CITTERIO, Mauro (INFN Milano, Italy)

**Co-authors:** CAMPLANI, Alessandra (INFN Milano, Italy); Mr DENG, Binwei (SMU Dallas, USA); MERONI, Chiara (INFN Milano, Italy); LIU, Chonghan (SMU Dallas, USA); Dr TAKI, Helio (Brookhaven National Laboratory); Mr CHEN, Hucheng (Brookhaven National Laboratory); Mr KIERSTEAD, James (Brookhaven National Laboratory); Dr YE, Jingbo (SMU Dallas, USA); Mr CHEN, Kai (Brookhaven National Laboratory); Mr TIANKUAN, Liu (SMU Dallas, USA); Mr CANNON, Matthew (BYU, Provo, USA); Dr WIRTHLIN, Mike (BYU, Provo, USA)

Presenter: CAMPLANI, Alessandra (INFN Milano, Italy)

Session Classification: Front end, Trigger, DAQ and Data Management - Poster Session

Track Classification: S5 - Front End, Trigger, DAQ and Data Management