Radiation testing campaign results for understanding the suitability of FPGAs in detector electronics.

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Introduction

CRAM based Field Programmable Gate Arrays (FPGAs) have been rarely used in High Energy Physics (HEP) due to their sensitivity to radiation. The last generation of commercial FPGAs based on 28 nm feature size and on Silicon On Insulator (SOI) technologies are more tolerant to radiation than the level that their use in front-end electronics is now feasible. FPGAs provide re-programmability, high-speed computation and fast data transmission through the embedded serial transceivers. They could replace custom application specific integrated circuits in front end electronics in locations with moderate radiation field. The use of a FPGA in HEP experiments is only limited by our ability to mitigate single event effects induced by the high energy hadrons present in the radiation field.

Radiation environment in HEP experiments

Radiation background is due to a mixed-field of hadrons, electrons and photons. The expected background for the ATLAS liquid Argon (LAr) calorimeter electronics is shown in Figure 1 and in Table 1 for Phase II run.

Radiation induced failures on electronics are tested in facilities:
- With particle energy spectra similar to the expected HEP environment
- At high rates to find Single Event Effects (SEE) with small cross sections

Figure 2 shows the irradiation facilities used in the present study.

Electronic devices will be simultaneously effected by:
- Single event effects
- Total ionizing dose
- Displacement damage

FPGA Kintex 7

Our experiments evaluate Xilinx Kintex-7 KX732ST chip performance under radiation. FPGA Kintex 7 delivers high signal processing capability and low power consumption:
- 326K of logic cells
- 16 Mb of BRAM
- 40K User FFs
- 840 DSPs
- BRAM Built in Error Correcting Code (ECC)
- 1.2 V core voltage
- 16 TX transmitters
- Transmitters can operate at a range of 500 Mb/s - 1.2 Gb/s for a maximum operating bandwidth of 300 Gb/s.

Experiments performed using Kintex 7 Evaluation Board, Figure 3.

How to provide radiation hardness

FPGAs are sensitive to Single Event Upset (SEE):
- Non-destructive SEE
- Defined as a change in the logic state of a cell
- Mitigated using Triple Modular Redundancy (TMR) and scrubbing

TMR is implemented by (Figure 4):
- Tripling hardwares resources
- Using majority vote on hardware outputs
- TMR tolerant
- Single faults and many fault combinations
- Almost always is coupled with scrubbing
- A scrubbing architecture
- Performs fault repair
- Continuously monitor the configuration memory
- Repair SEU within the memory in real time

Parameters

Rad-hard techniques must prevent:
- Build up of configuration errors in CRAM
- Errors that "break" SEC/DED code in BRAM
- Corruption on transmitted data
- Transmitter/receiver de-synchronization

Parameters measured during the experiments are:
- FPGA Supply voltages and currents
- Configuration RAM (CRAM) crossing section
- Block RAM (BRAM) crossing section
- Data link failure rates
- Single Event Functional Interrupts (SEFI)
- Single Event Latch-up (SEU)

H4IRRAD results

H4IRRAD test area near the 4 MeV beam live at CERN:
- One of the few mixed-field (hadrons and neutrons) test area available
- Attenuated primary 400 GeV/c proton beam from CERN SPS or secondary beam of 280 GeV/c proton beam over Cu target (1 m long, 7.5 cm diameter)
- Large experimental area with difficult access to the Device Under Test (DUT), Figure 5.
- 50 hours of testing (1.8 x 10^15 hadrons)
- Large uncertainties on total particle fluence at DUT position
- Ionization dose deposited by hadrons not well known
- No current monitoring during the test

Estimated static cross section measurements results shown in Table 2.
- No test performed on MGTS.

Neutron results

Test performed at LANSCE - WHIRL (Los Alamos), max energy 800 MeV and at TSL (Uppsala), max energy 200 MeV.
- Wide neutrons spectrum similar to cosmic ray background.
- Over 30 hours of neutron testing (5.7 x 10^15 neutrons)

Parameters under test BRAM and CRAM. Results shown in Table 3.
- Mitigation strategies implemented on the DUT:
  - TMR
  - Multi-level (internal and external) scrubbing
  - No SEFI and no SEU observed during the experiment.

Some preliminary tests on MGTS data transmission:
- Two lanes tested at 5 Gbps
- Approximately 6 links failures observed
- Failures not correlated with error types

More details on MGTS failures studied with proton tests.

Proton results

Two different experiments performed at The Swedberg Laboratory (TSU) in Uppsala, Sweden, with 180 MeV protons, to:
- Re-measure the CRAM and BRAM cross section
- Evaluate the performance of the GTX transceivers of a Kintex 7 FPGAs

Proton beam is useful to simulate the complex radiation environment expected at the LHC accelerator. Protons deposit ionization dose and induce displacement damage.

In the first experiment, parameters under test were BRAM and CRAM. Results shown in Table 4 confirm the results obtained with neutrons.

Parameters measured during the experiments are:
- CRAM and BRAM cross sections
- MGTS crossing section
- FPGA Supply voltages and currents

In the second experiment 13 bidirectional lane were tested with configuration scrubbing without TMR, Figure 7.

Events of interest identified during the experiment are (Table 5):
- Configuration Error: due to the circuitry surrounding the MGT and not a problem with the actual MGT
- Lane Error: caused by a MGT failure
- DUT Error: caused all 13 lanes to fail simultaneously and suggests that some form of global failure or SEFI is occurring

Half of MGTS errors could probably be prevented by applying common mitigation techniques to the circuit, such as TMR.

Cross section comparison

The results presented summarize a two years long study which is still on going.

Permanent operational failures were never observed up to the level of radiation to which the FPGA was exposed.

CRAM and BRAM cross section results indicate that TMR plus multi-level scrubbing are essential to mitigate SEU in Kintex 7 FPGAs.

The estimated MGT lane error rate suggests that the configurable logic interfaces which MGTs is the most sensitive part of the FPGA. However application of mitigation methods, not applied during our tests, could significantly reduce this sensitivity. Based on the results obtained in these experiments, at the full scale ATLAS LAr calorimeter system we could estimate a lane failure every 6.5 minutes. Approximately, future experiments are planned with improved TMR and scrubbing mitigation strategies to further reduce the present error rates.

We are working towards also implementing a test board in ATLAS to gather more realistic data.

Conclusion and Outlook