

A Pattern Recognition Mezzanine based on Associative Memory and FPGA technology for L1 track triggering at HL-LHC

L. Alunni¹, N. Biesuz⁴, G.M. Bilei¹, S. Citraro⁴, F. Crescioli⁵, L. Fanò¹, G. Fedi⁴, D. Magalotti^{1,2}, G. Magazzù⁴, L. Servoli¹, L. Storchi¹, F. Palla⁴, P. Placidi^{1,3}, A. Papi¹, Y. Piadyk⁵, E. Rossi⁴

1. INFN – Sezione di Perugia
4. INFN – Sezione di Pisa



2. UNIMORE – Università di Modena e Reggio Emilia



3. DIEI – Università di Perugia

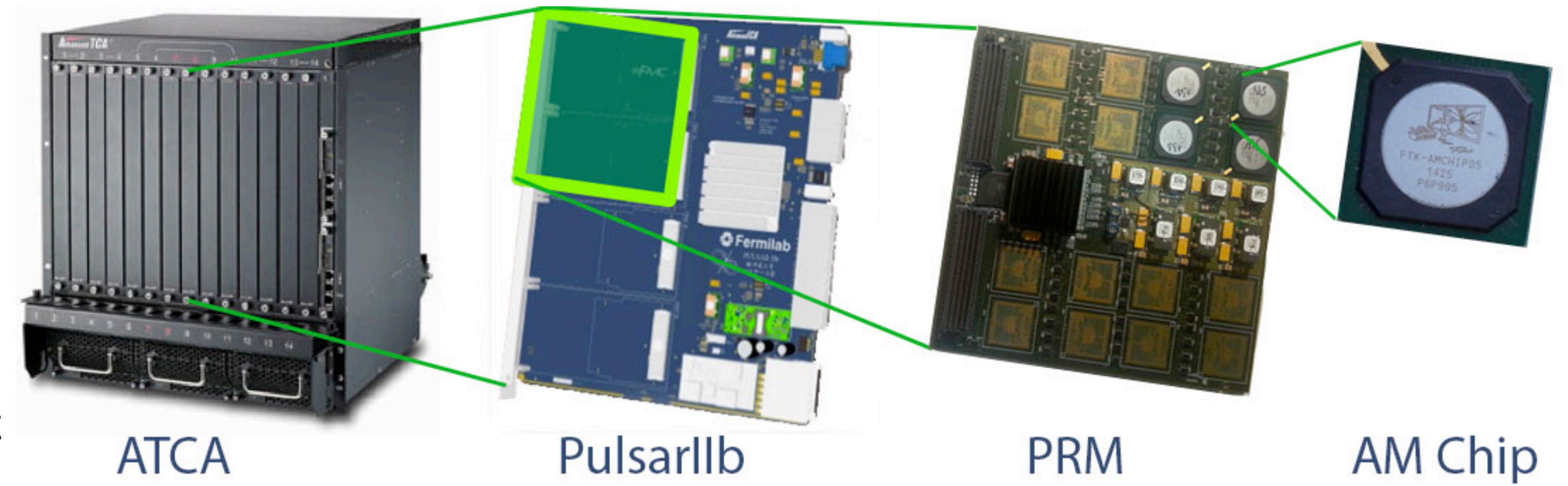


5. LPNHE Paris

INTRODUCTION

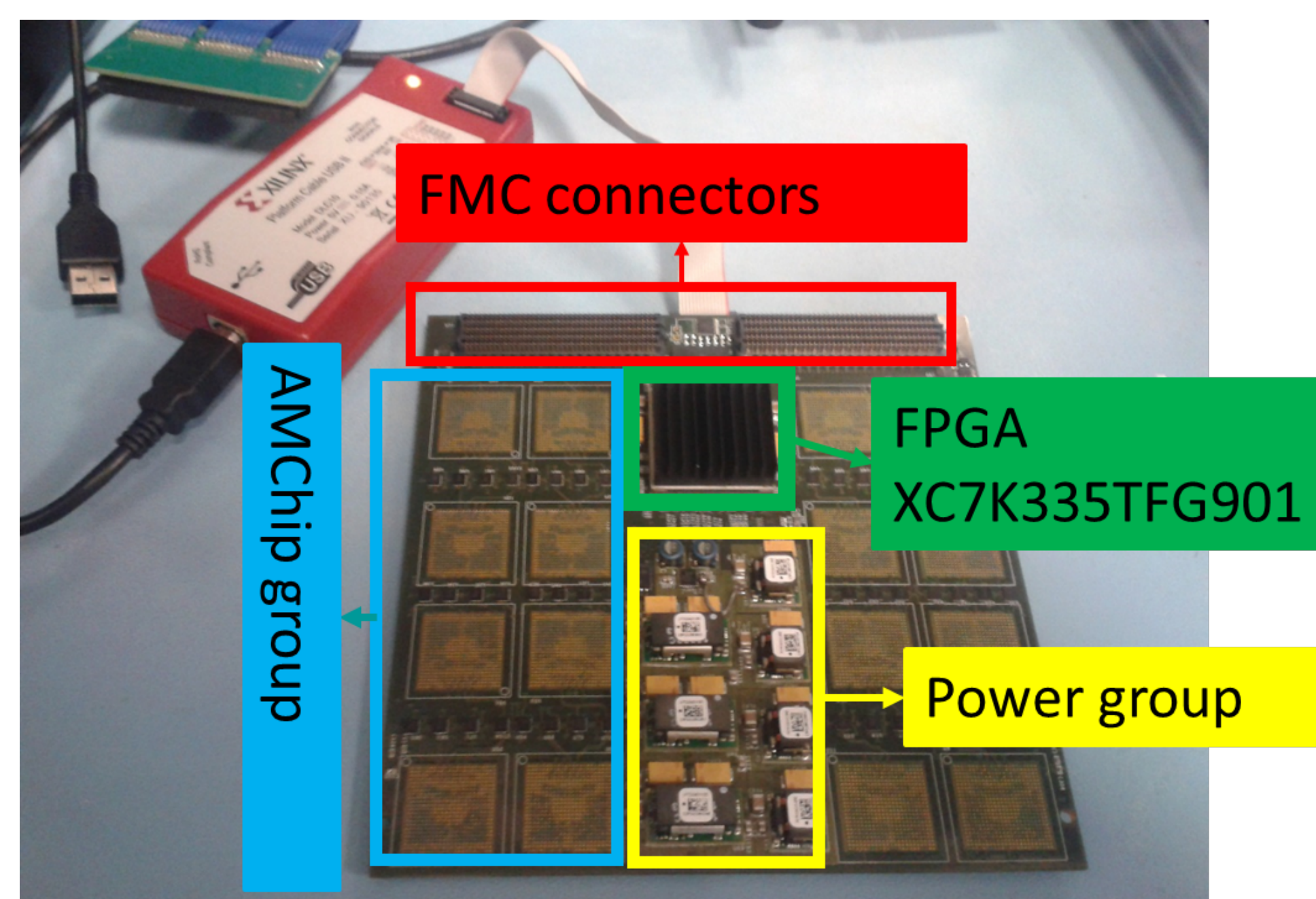
At high luminosity LHC ($5 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$), the number of interactions per bunch crossing will increase to 140 (and up to 200), and the trigger challenges due to the high pileup will be enormous.

- The silicon-based tracking information is the most effective way for pileup mitigation, if it can be made available to L1 trigger within the required latency (~5 microseconds)
- A dedicated hardware processor is hence the proposed solution to be used at L1 trigger to select interesting configurations at the 40 MHz bunch-crossing rate [1]
- The proposed CMS phase II L1 tracking trigger is conceptually organized in 48 trigger towers ($6 \eta \times 8 \phi$)
- Each tower is managed by a Advanced Telecom Computing Architecture (ATCA) crate. The basic card slot in each crate is the Pulsar II board [2]
- The Pattern Recognition Mezzanine (PRM) based on the Associative Memory and the FPGA technologies
- We aim to built a prototype of the system with the state of the art technology to show the feasibility of the project.



PATTERN RECOGNITION MEZZANINE ARCHITECTURE

The Pattern Recognition Mezzanine (PRM) is a $14.9 \times 14.9 \text{ cm}^2$ card hosting two High Pin Count connectors (FMC), a Xilinx FPGA (XC7K355T) and 16 AM chips. The FPGA will have the role of routing the hits coming from the tracker layers, collecting the candidate tracks and performing a track fitting operation.



The logic resources of the Pattern Recognition Mezzanine

- 16 Associative Memory Chips for a total amount of patterns:
 - PRM with AM05 $\rightarrow 2 \text{ kpatterns} \cdot 16 \text{ AM chips} = 32 \text{ kpatterns/PRM}$
 - PRM with AM06 $\rightarrow 128 \text{ kpatterns} \cdot 16 \text{ AM chips} = 2 \text{ Mpatterns/PRM}$

EXPERIMENTAL SETUP

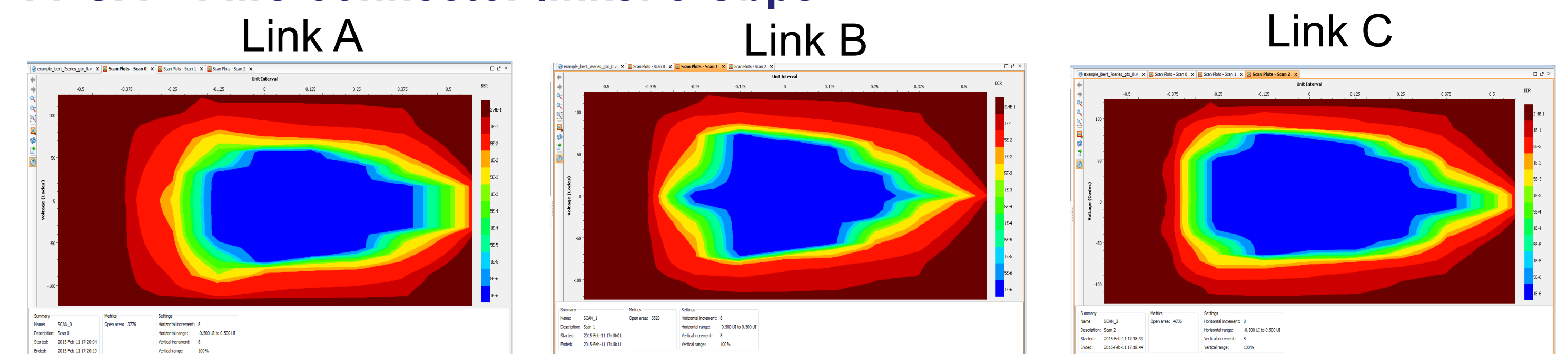


The experimental setup consists of:

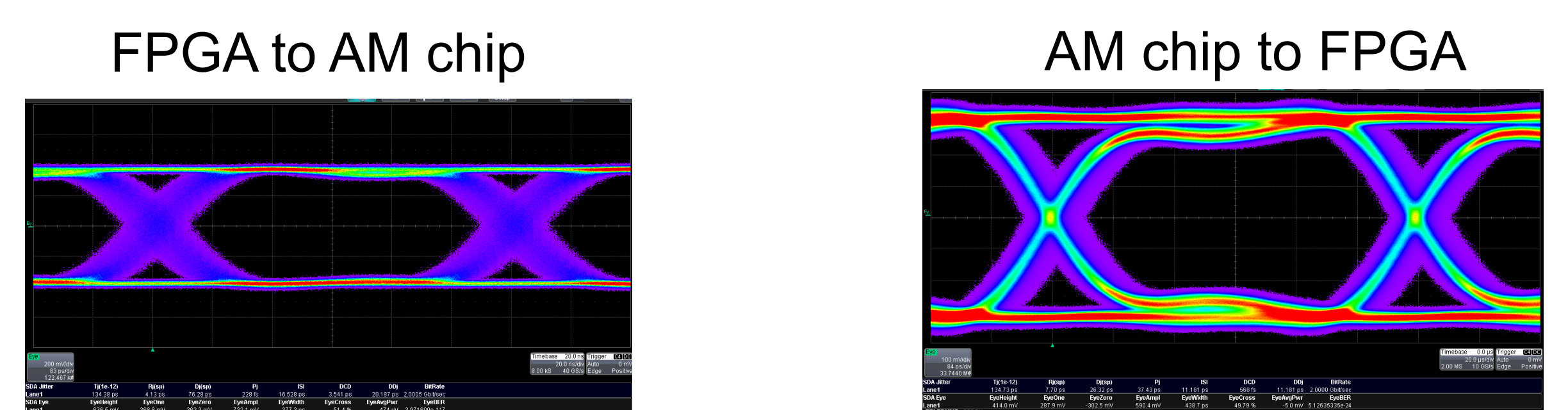
- loopback card providing the power and connects in loop the High Speed Serial I/O of the FMC connectors;
- the PRM board.

The eye diagram of the High Speed Serial links are tested with the IBERT core of the FPGA and a serial data analyzer.

FPGA – FMC connector links: 8 Gbps



FPGA – AM links: 2 Gbps (PRBS 7 sequence)



EVENT TRACK RECONSTRUCTION

Pattern Matching (AM approach)

The Associative Memory has a modular architecture in which each chip includes both the memory required for storing candidate tracks (patterns) and the logic needed for the actual comparison.

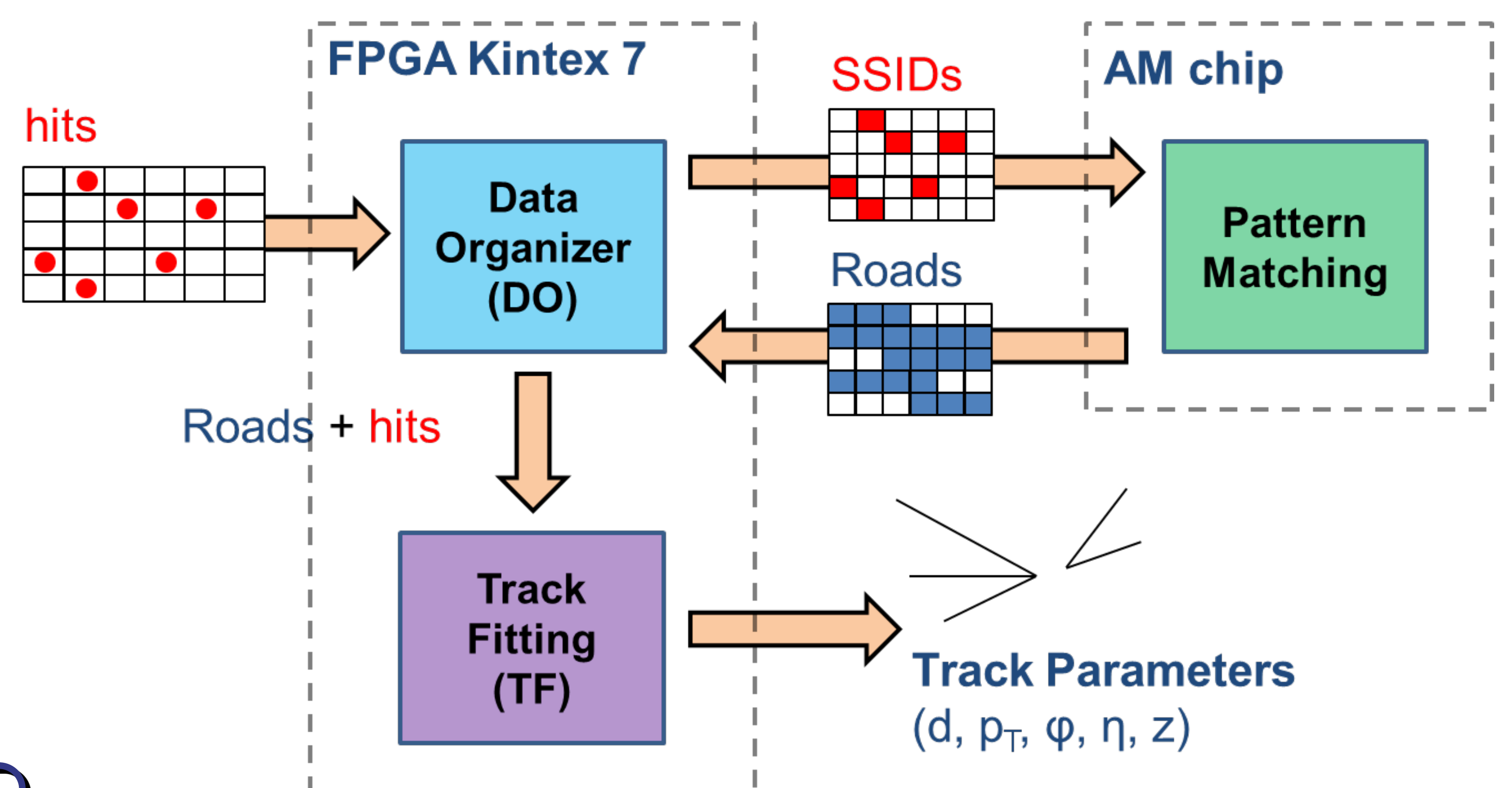
- The device compares the SuperStrips ID (SSID) with all the stored patterns.
- The device returns the addresses (Road ID) of the matching locations.

Data Organizer (FPGA logic and memories)

The Data Organizer (DO) implements a SmartDB containing the SuperStrip ID and the Road ID value according to the information written in the Associative Memory chip.

Track Fitting (FPGA logic)

A fit is done computing all combinations of hits across layers.



CONCLUSION

The proposed processor for the L1 track trigger provides high computation power combining the Associative Memory and the FPGA technologies. It implements also the Data Organizer and Track Fitter stages to minimize the latency of the whole processing chain.

REFERENCE

- [1] A. Annovi et al., *Associative Memory for L1 Track Triggering in LHC environment*, Nuclear Science, IEEE Transactions on, vol. 60, no. 5, pp. 3627–3632, Oct 2013
[2] J Olsen et al. *A full mesh ATCA-based general purpose data processing board*, 2014 JINST 9 C01041