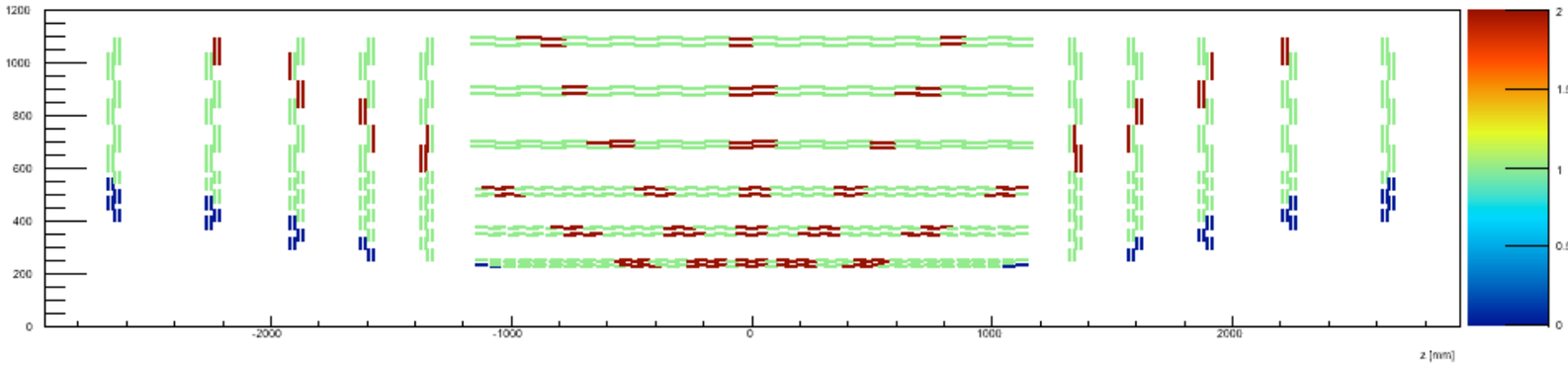
A Patter Recognition Mezzanine based on Associative Memory and FPGA technology for L1 track triggering at HL-LHC

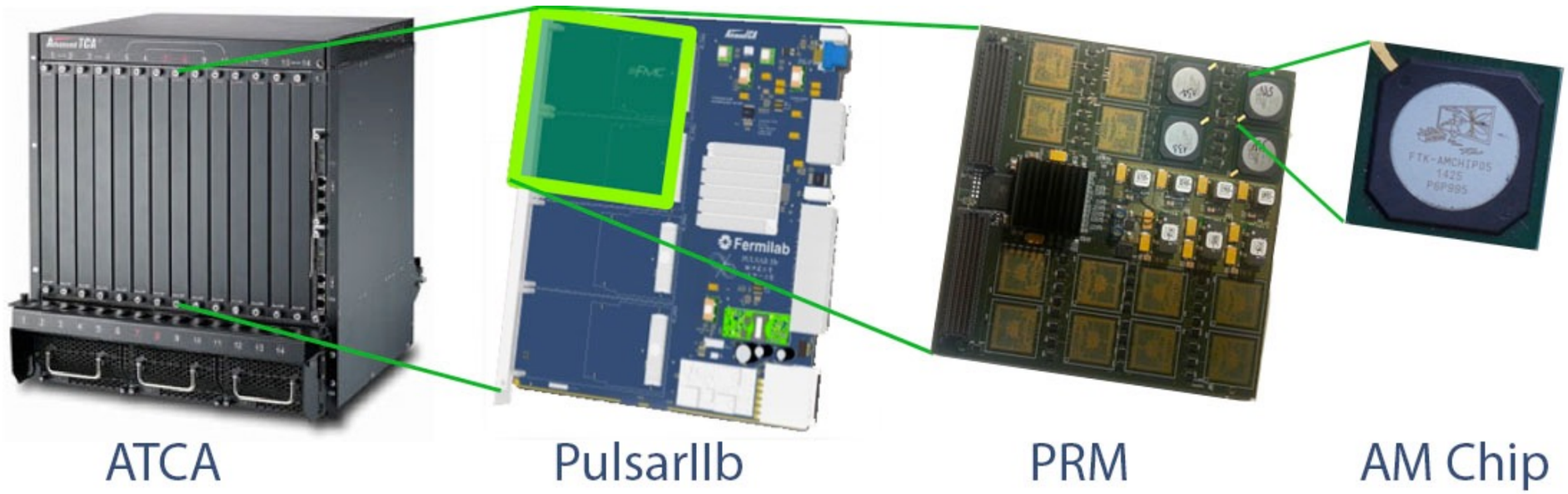
Giacomo Fedi

few hundred stubs/tower

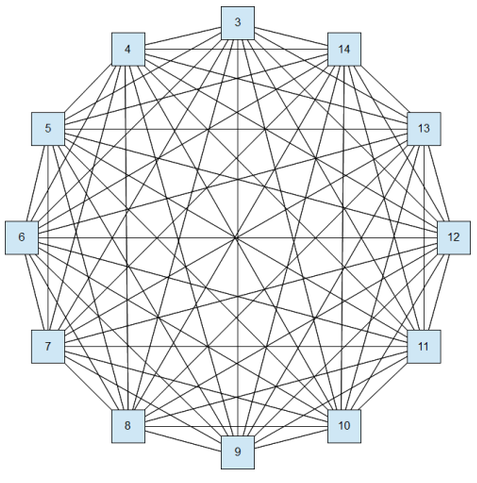
few hundred stubs/tower

CMS HL-LHC tracker



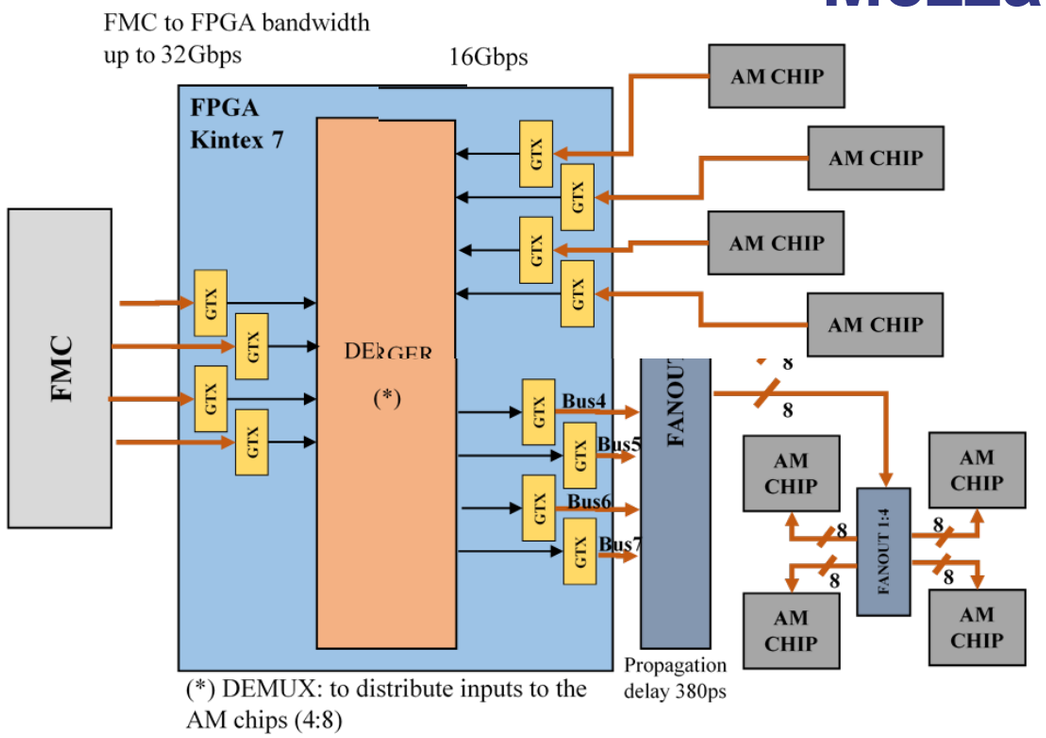


ATCA PulsarIIb PRM AM Chip



- Send data to Pattern Recognition Mezzanine in each ATCA blade
  - Data distributed to Pulsar boards in time multiplexed mode in round robin
  - Perform pattern recognition using several AM chips (120k Patterns/AM chip)
  - Track fit with FPGA inside the Mezzanine (~1 ns/fit)

Mezzanine testing



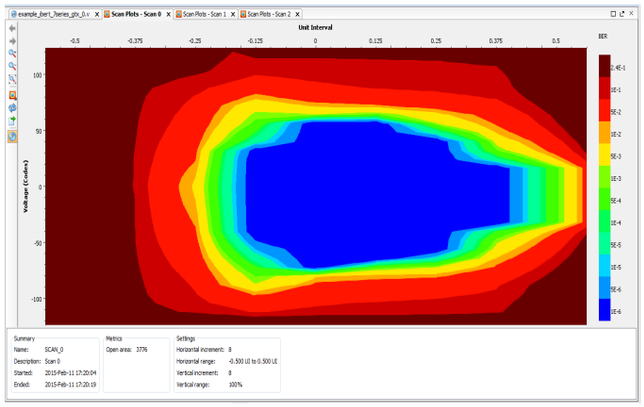
Input Super Strip (SSID) distribution

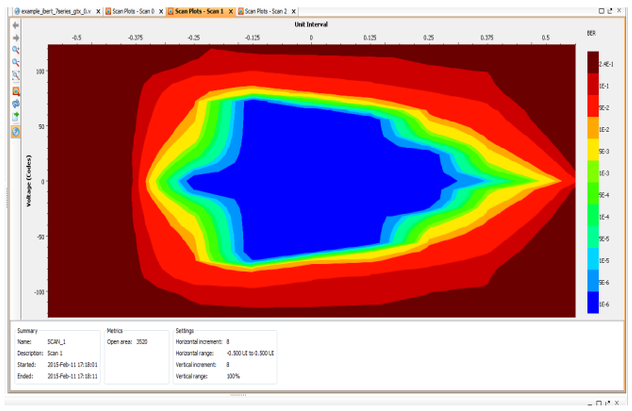
Dedicated transceiver for each of the 8 inputs of AM chip bus @ 2 Gb/s

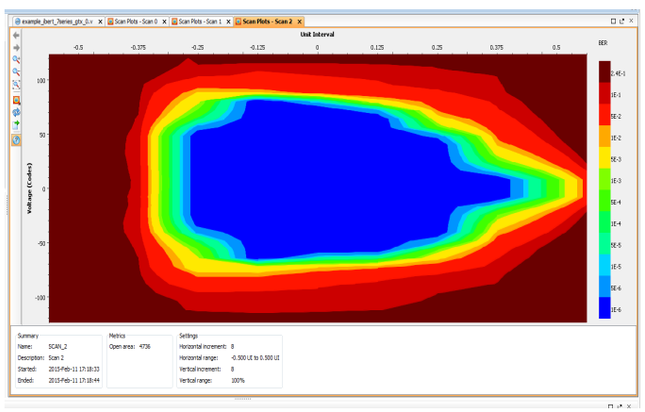
Matched roads output to Track fitter

"Star" connection of 8 individual AM chip outputs @ 2 Gb/s

FPGA – FMC connector links: 8 Gbps







FPGA – AM links: 2 Gbps (PRBS 7 sequence)