Characterization of Bandgap Reference Circuits designed for High Energy Physics Applications

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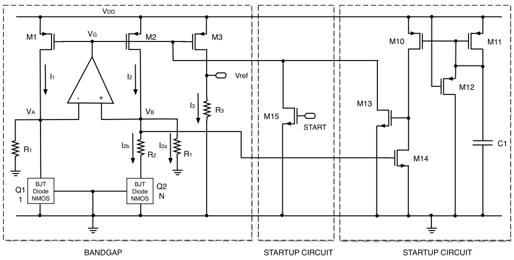
Introduction

Bandgap reference circuits (BGR) in a commercial 65nm CMOS technology were designed and fabricated in view of a potential use in high-energy physics (HEP) applications. Since in bandgaps radiation-susceptibility is mainly due to the bipolar devices or diodes, a version employing MOSFET transistors biased in weak inversion with standard and special layout techniques have been designed. Trimming techniques to adjust the reference voltage as a function of temperature are not included in the circuits.

Circuit description

Current mode bandgap voltage reference circuit



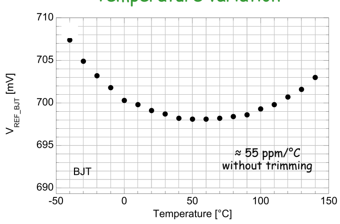
$$V_{REF} = \frac{R_3}{R_1}\left[V_{BE} + \frac{R_1}{R_2} V_T \ln(N)\right]$$

- I_{2a} decreases with temperature (CTAT)
- I_{2b} is proportional to the absolute temperature (PTAT)
- $dI_3/dT \approx 0 \implies V_{ref}$ has a very low temperature sensitivity

- Two different startup circuits were included
- Layout dimensions ≈ 250 μm x 110 μm
- Power consumption ≈ 50 μW

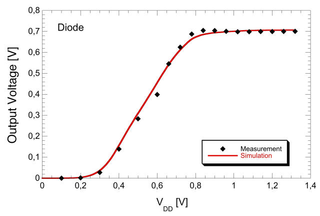
Circuit characterization

Temperature variation

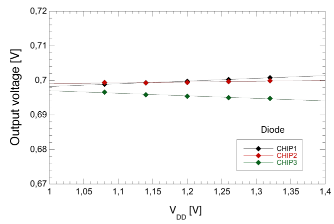


±3.4 mV over a temperature range of 170°C (-30°C to 140°C)

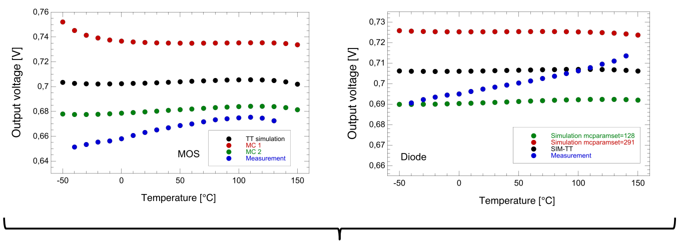
Voltage supply effect



Circuits correctly operate with supply voltages in the range from 1.32V down to 0.78V

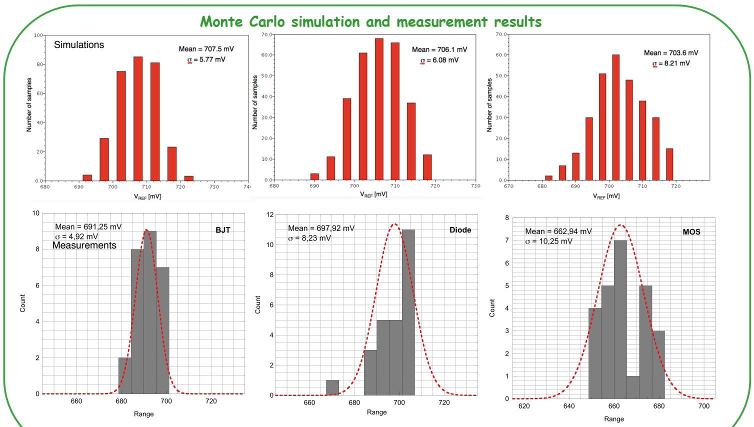


The measured **line regulation** at room temperature is about 1 %/V

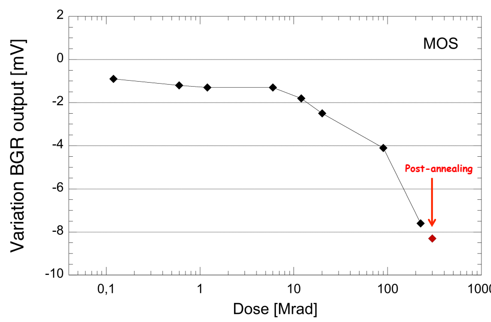


Comparison between worst case Monte Carlo simulations and measurements as a function of temperature. A trimming resistor is needed to change the slope of the CTAT voltage to the slope of the PTAT voltage in order to minimize the temperature coefficient of the reference voltage

Monte Carlo simulation and measurement results



Bandgap irradiated with X-rays (Legnaro), TID 230 Mrad



- **BGR based on BJT devices:** increase of the output voltage from 690 mV to 737mV: variation of 47mV. Recovers 6mV with annealing (7 days at room temperature)
- **BGR based on diode devices:** increase of the output voltage from 706mV to 756mV: variation of 50 mV. Recovers 6mV with annealing (7 days at room temperature)
- **BGR based on MOS in WI:** decrease of the output voltage from 674.8mV to 667,2 mV: variation of 7.6mV, degradation. Increase 0.7mV with annealing (7 days at room temperature)

Conclusion and future activity

- A reference voltage shift around 0.6% was measured after irradiation with 10keV X-rays up to about 100 Mrad (SiO_2)
- A new design with trimmable resistance in order to reduce the temperature coefficient was designed and fabricated
- A different bias point of the circuit, featuring higher static currents, has to be used in order to improve the radiation hardness up to 1 Grad

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