The Central Logic Board for the KM3NeT detector: design and production

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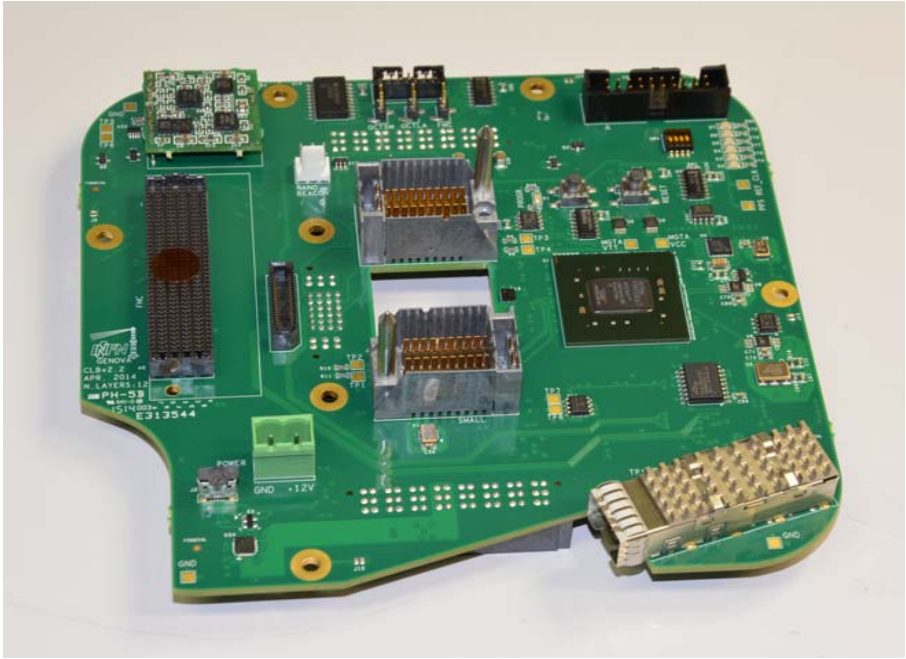
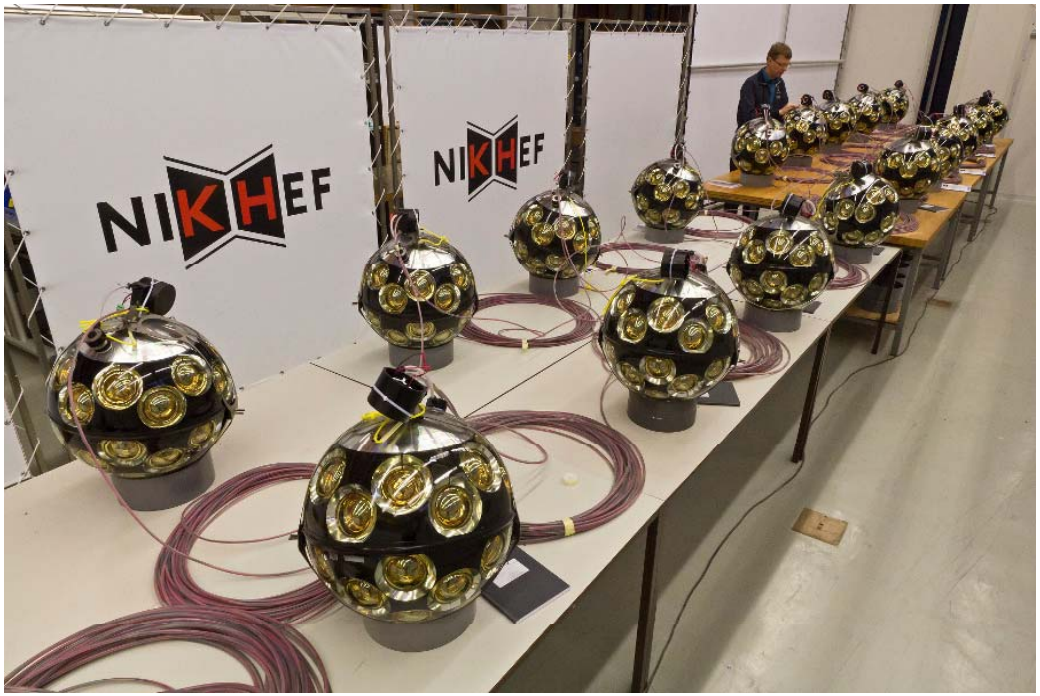
The Central Logic Board (CLB) has been developed to acquire timing and amplitude information from the PMT signals of the Optical Module (DOM), implementing time-to-digital conversion (TDC) with time over threshold (TOT) technique.
The board is also used to configure all the DOM subsystems, to assist in the DOM position and orientation, calibration and to monitor temperature and humidity in the DOM itself.
A large Field Programmable Gate Array (FPGA) has been adopted to implement all the specifications with the requested performances.



- Xilinx Kintex-7 FPGA (XC7K160TBG676) is the core of the board
- Two microprocessor systems based on LM32 soft processor are implemented:
  - White Rabbit Precision Time Protocol engine: implement 1 ns time synchronization and transfer data to shore station
  - Configuration and slow control: handles all the devices inside the DOM, manage housekeeping data and implement debug ports

- The 31 TDC channels measure the arrival time and the pulse width of the PMT discriminated signals with 1 ns resolution

- More than 200 tested CLBs have been delivered for DOM integration



Assembling the 1st Detection Unit (DU-1)