Contribution ID: **216** Type: **Poster**

Design and test of clock distribution circuits for the Macro Pixel ASIC

Thursday, 28 May 2015 17:56 (0 minutes)

The innermost part of the CMS outer tracker at the HL-LHC is based on a combination of pixelated and short strip sensors, the so-called Pixel-Strip module (PS). The pixelated layer is read out by means of the Macro Pixel ASIC (MPA), bump bonded to the sensor, as normally done in hybrid pixels. The MPA consists of a matrix of 16x120, 1500um x 100um pixels, and will be designed in a 65 nm CMOS technology. Clock distribution circuits account for a significant fraction of the power dissipation in the readout chip, mainly related to the dynamic power needed to drive the long lines running the clock signal through the wide area matrix. Moreover, the clock signal must be distributed all over the chip with minimum possible skew. A test chip including the clock distribution circuits of the MPA has been fabricated and tested. The prototype chip includes metal structures emulating the long clock lines that will be laid out in the final design of the MPA, and two versions of the drivers and the receivers suitable for operation in the readout chip. These versions are based on CMOS drivers supplied with a reduced supply voltage and on static reduced-swing drivers. Experimental results show that a power saving up to 60% can be obtained with a 0.8V chip supply voltage. The paper will present a summary of the experimental results relevant to the prototype chip, focusing particularly on the power and speed performance and will compare such results with those coming from circuit simulations.

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Session Classification: Front end, Trigger, DAQ and Data Management - Poster Session

Track Classification: S5 - Front End, Trigger, DAQ and Data Management