Design and test of clock distribution circuits for the Macro Pixel ASIC

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Introduction

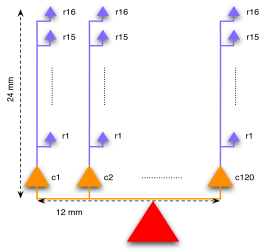
The innermost part of the **CMS tracker** at the HL-LHC is based on a combination of pixelated and short strip sensors, the so-called **Pixel-Strip module**. The short strip layer is read out as a classical strip detector by means of the Strip Sensor ASIC, while the pixelated layer is readout by means of the **Macro Pixel ASIC** (MPA), bump bonded to the sensor, as normally done in hybrid pixels. **Clock distribution** circuits account for a significant fraction of the **power dissipation** in the readout chip: the clock signal must indeed be distributed all over the chip with minimum possible skew. While keeping the skew at a minimum, clock distribution networks waste a significant amount of power.

A **65nm CMOS test chip,** including the clock distribution circuits of the MPA, has been fabricated and tested. The prototype chip includes metal structures emulating the long clock lines that will be laid out in the final design of the MPA, and two versions of the drivers and the receivers suitable for operation in the readout chip. A summary of the **simulation and experimental results**, focused on the power and speed performance, will be given in this work.

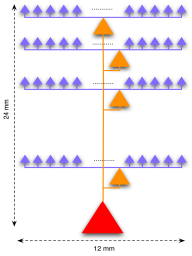
The Macro Pixel ASIC

MPA main characteristics

- 16x120 matrix featuring a pixel size of 1500 µm x 100 µm
- Designed in a 65 nm CMOS technology
- Limited power budget (~200 mW) available to carry out the complex functions integrated in the chip
- **40 MHz** clock operating frequency



Column distribution



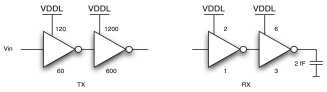
Row distribution

In the design phase of the prototype chip, two routing schemes for the clock distribution have been investigated: the **column distribution** (CD) and the **row distribution** (RD)

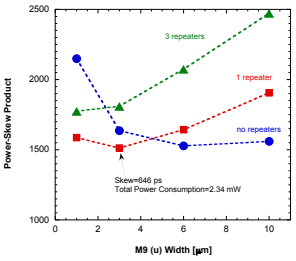
Investigated architectures and simulation results

- **CD scheme** for the MPA consumes a huge amount of power due to the large number of columns
- The integrated solution features an **RD architecture** where a central buffer column distributes the clock along the matrix and 1 clock line per row distributes the clock to the 120 pixel cells in the row
- A study of the optimum number and dimension of repeaters to be placed on the central column (laid out with ultrathick metal M9) has been carried out
- Two possible implementations have been investigated, based on CMOS buffers supplied with **reduced VDD** and on **reduced swing** drivers
- We evaluated each architecture in terms of **total power consumption** (including the contribution from row drivers, pixel receivers and column repeaters) and the maximum **skew** between pixels. A comparison with conventional full swing buffers (1.2 V) has been carried out.

Reduced supply voltage

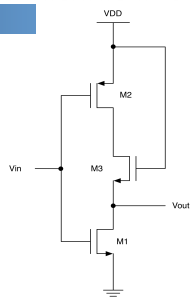


Standard CMOS buffers as TXs and RXs, supplied by VDDL=800 mV



Reduced-swing driver

The M3 nMOS transistor is inserted between the pMOS and nMOS transistors of a simple inverter to **decrease the output voltage swing**. An asymmetric inverter involving an LVT nMOS and a HVT pMOS can be used **as the receiver**.

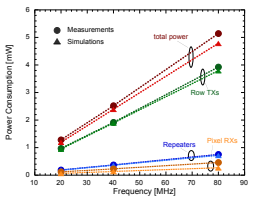


Simulations carried out for different number of buffers in the central column, for different column width

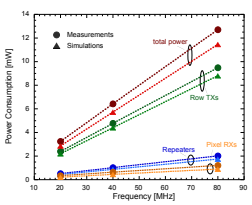
	Skew @ rising edge [ps]	Skew @ falling edge [ps]	Average Skew [ps]	Total Power Consumption [mW]	Power-Skew Product [fJ]
0.8V Solution	632	660	646	2.34	1512
Low-swing	489	636	562	4.34	2441
1.2V Solution	435	447	441	5.41	2386

Measurements results

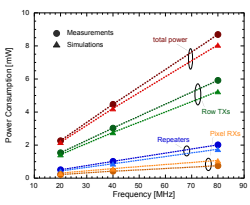
CMOS drivers @ 0.8 V



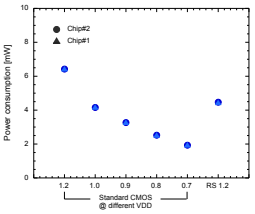
CMOS drivers @ 1.2 V



Reduced swing driver (RS) @ 1.2 V

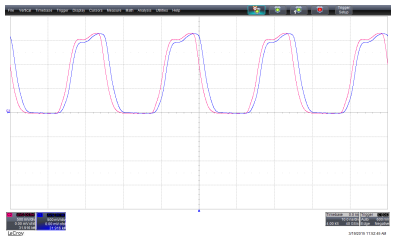


Chip-to-chip variations



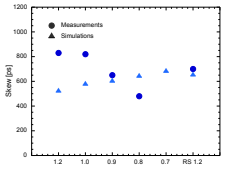
- **Total power consumption**, for a 40 MHz clock signal:
  - CMOS drivers @ 0.8V → 2.5 mW
  - CMOS drivers @1.2V → 6.4 mW
  - Reduced-swing drivers → 4.5 mW
- A **power saving** up to 60% can be obtained with a 0.8V chip supply voltage. A 30% gain is achieved with the RS solution, **not requiring a reduced supply voltage.**
- **Simulations and measurements** in good agreement. Main contribution to the total power consumption given by the row drivers.
- **Negligible** chip-to-chip variations.

Maximum skew between pixels, fclk= 40 MHz

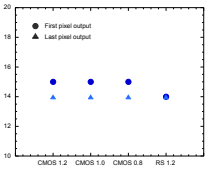


- **Skew** well below 1 ns for the investigated solutions. Differences between simulations and measurements (probably due to modeling of the chip output PADs)
- Very good performance in terms of **jitter** (close to 15 ps for the investigated solutions)

Skew



Jitter



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