Low-power architectures are required to meet the power budget constraint of the Macro Pixel ASIC, the readout chip for the so called Pixel-Strip module of the CMS tracker.

A 65nm CMOS test chip, including the clock distribution circuits for the MPA, has been fabricated and tested.

Two possible implementations have been investigated, based on CMOS buffers supplied with reduced VDD and on reduced swing drivers.

The proposed solution is based on a row clock distribution scheme.
Design and test of clock distribution circuits for the Macro Pixel ASIC

- **Standard CMOS buffers** as TXs and RXs, supplied by VDDL=800 mV
- **Reduced swing driver** supplied at VDD=1.2 V

**Maximum skew @ 40 MHz**

- Up to 60% power saving with a 0.8V chip supply voltage
- Max. skew < 1 ns