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An artificial retina processor for track reconstruction at the full LHC crossing rate

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The INFN-RETINA is an R&D project aimed at developing and implementing a parallel computational methodology allowing the reconstruction of events
with hundred of charged-particle tracks in pixel and silicon strip detectors at 40 MHz, thus suitable for processing LHC events at the full crossing frequency.
For this purpose we design and test a massively parallel pattern-recognition algorithm, inspired by studies of the processing of visual images by the brain
as it happens in nature. We find that high-quality tracking in large detectors is possible with sub-microseconds latencies when this algorithm is implemented
in modern, high-speed, high-bandwidth FPGA devices. This opens a possibility of making track reconstruction happen transparently as part of the detector readout.
The detailed geometry and charged-particle activity of a large already-built tracking detector are simulated and used to assess the performance of an artificial retina
processor prototype at the current available silicon readout frequency of 1MHz. TEL62 boards, equipped with 4 Altera Stratix III FPGAs providing the adequate
computing power, are used for the processing stage of the prototype. We report on the first results of such fast tracking device based on test with simulated and real
LHC events.

Collaboration

On behalf of the RETINA Collaboration. The RETINA project is funded by CSN5 of INFN. The members of the RETINA Collaboration are affiliated with Università di Milano, Politecnico di Milano, Università di Pisa, Scuola Normale Superiore di Pisa, Fermilab (USA) and INFN, Italy.

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