An "artificial retina" processor for track reconstruction at the full LHC crossing rate

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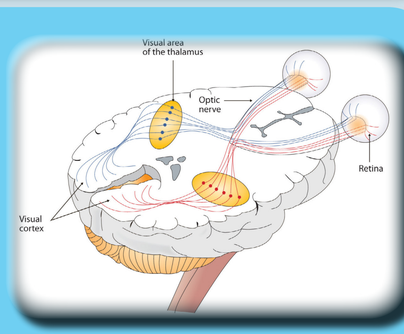
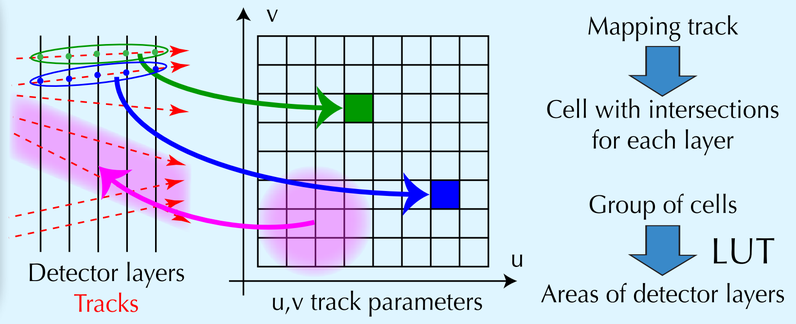
Problem: trigger efficiently hadronic events at very high luminosity (>10^{34} $cm^{-2}s^{-1}$)

The "Artificial Retina" algorithm[1]

- **Highly-parallel** algorithm inspired to quick detection of edges in mammals visual cortex
- **Continuous response** with limited number of pre-calculated patterns, which allows a coarser grid mapping of parameters
- Reconstruction of charged-particle trajectories (tracks) at LHC collisions frequency with **few μs latency**, which allows to trigger hadronic events

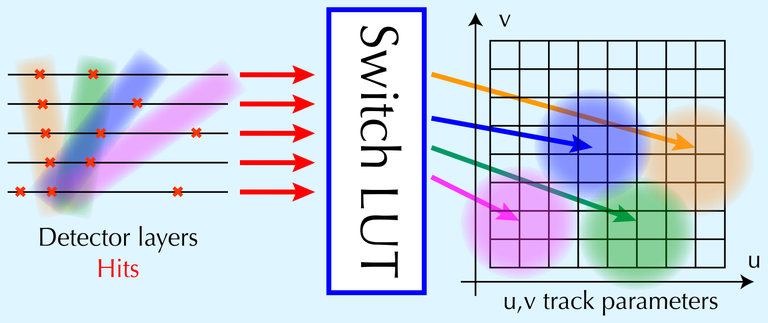


Phase A: Double mapping (PC simulation)

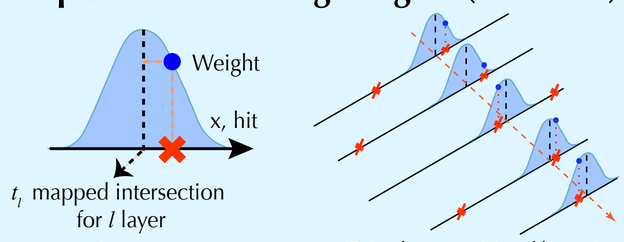


Phase B: Reconstruction (FPGA, Track Processing Unit TPU)

Step 1: Hits delivery through a switch



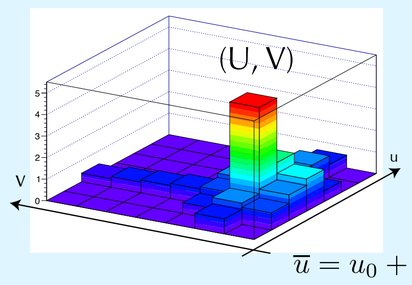
Step 2: Accumulating weights (each cell)

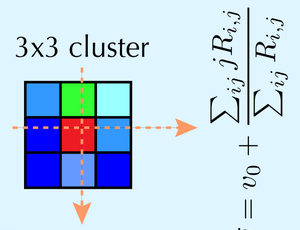


$$R = \sum^{\text{hits}} e^{-\frac{(x_l - t_l)^2}{2\sigma}}$$

R is close to N (# of layers) only if we have a set of hits near the mapped track

Step 3: Find the local maxima and compute centroid





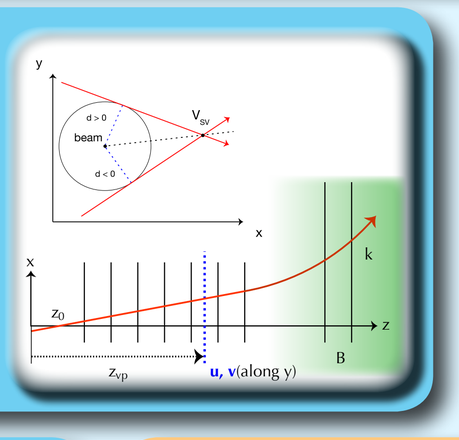
$$\overline{u} = u_0 + \frac{\sum_{ij} iR_{i,j}}{\sum_{ij} R_{i,j}} \quad \begin{matrix} i=U-1,U,U+1 \\ j=V-1,V,V+1 \end{matrix}$$

$$\overline{v} = v_0 + \frac{\sum_{ij} jR_{i,j}}{\sum_{ij} R_{i,j}}$$

Goal: reconstruct high quality tracks for events at 40 MHz, lab prototype at 1 MHz

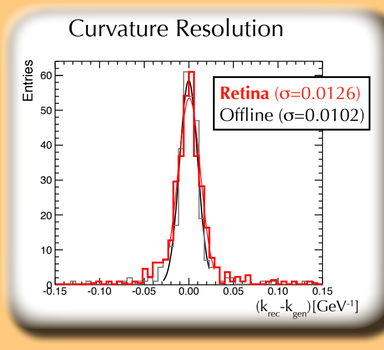
Study for a real-detector application[2]

- Forward spectrometer, **pixel silicon tracker** with fringe magnetic field, independent subset of LHCb tracker in 2020
- Track parameters: intersections u,v with virtual plane at z_{vp}
- Track origin shifts (z_0,d) and curvature (k) are included as perturbations
- Available testing events: single track, simulated using official LHCb simulation[3] with 2020 conditions after the upgrade



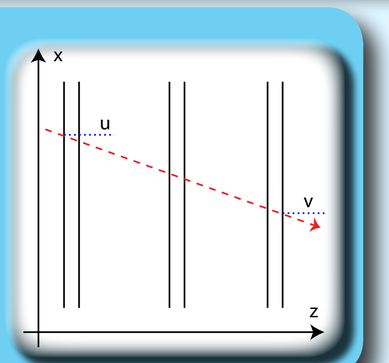
Study results[2]

- Using about 20k cells, **reconstruction performances equal to offline algorithms**
- Basic logic implementation in VHDL on **Altera Stratix V FPGA**, event processing time is about 150 clock cycles (**0.5 μs latency** @350MHz)
- 20k cells **fit into 32 Stratix V chips**



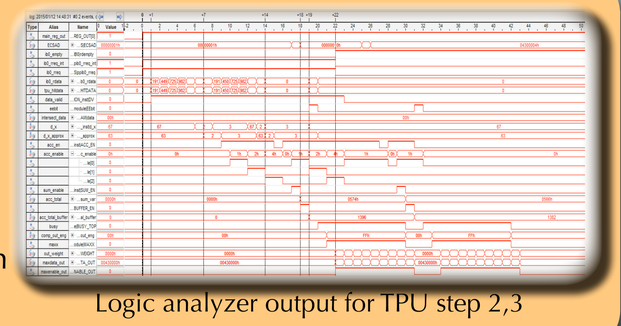
First prototype[4]

- Simplified tracker with 6 single-coordinate layers (x silicon strips)
- Track parameters: first and last layer coordinates (u,v)
- Available testing events: single track, simulated, **real data**



Prototype Results

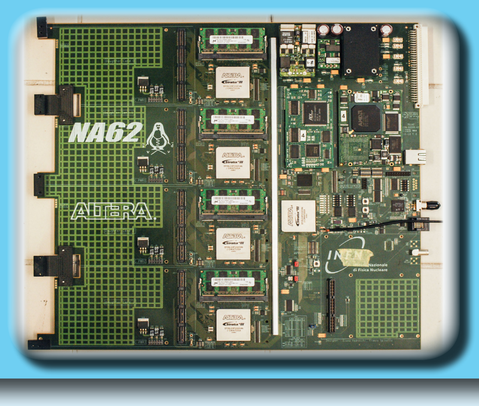
- Good reconstruction efficiency with about 3k cells, fit into 32 Stratix III chips
- TPU step 2,3: firmware designed and simulated[5]
- TPU step 2,3: firmware **fully working on the real board at 160 MHz**, including Ethernet output to PC
- Using detector occupancy from real data and switch simulation, **max event rate is 1.8 MHz**

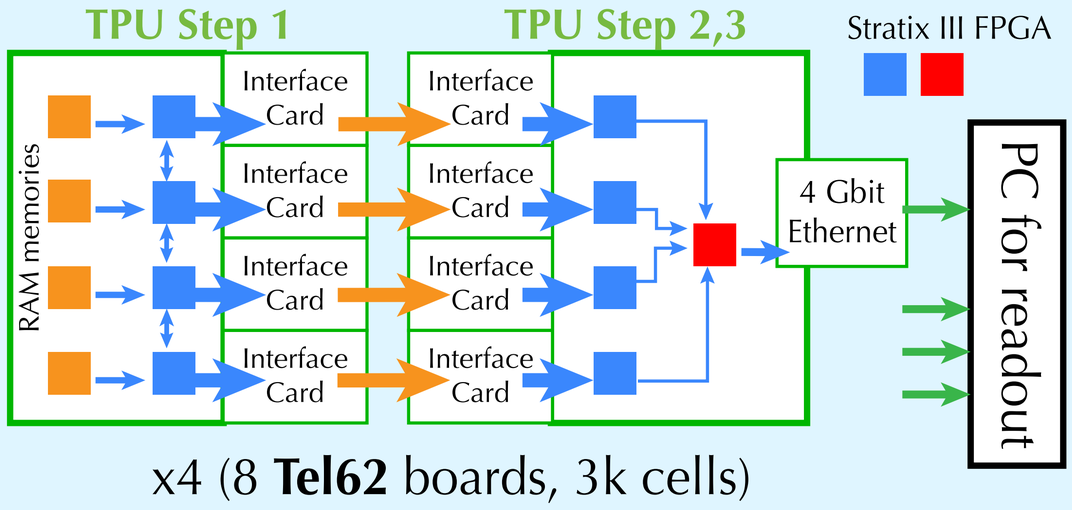


Logic analyzer output for TPU step 2,3

Prototype tech details[6]

- **Tel62** board developed by INFN for NA62
- FPGA **Altera Stratix III**: 4 processing unit (PP's) controlled by one master (SL)
- Clock: 40 MHz, 160 MHz inside FPGA's
- Memory: 4x2Gb DDR2, 64bit@640MHz
- I/O rate: 10 Gbit PP to SL, 5 Gbit on generic mezzanine slot (x4), 2.5 Gbit between PP's and SL to Ethernet card
- Slow control interface (embedded PC)





x4 (8 **Tel62** boards, 3k cells)

References:
[1] L. Ristori, *An artificial retina for fast track finding*, NIM A453 (2000) 425.
[2] A. Abba *et al.*, *A specialized track processor for the LHCb upgrade*, CERNa-LHCb-PUB-2014-026.
[3] M. Clemencic *et al.*, *The LHCb simulation application, Gauss: Design, evolution and experience*, J. Phys. Conf. Ser. 331, 032023 (2011).
[4] A. Piucci, *Reconstruction of tracks in real time at high luminosity environment at LHC*, Master thesis, https://etd.adm.unipi.it/theses/available/etd-06242014-055001/.
[5] D. Ninci, Real-time track reconstruction with FPGA at LHC, https://etd.adm.unipi.it/theses/available/etd-11302014-212637/.
[6] F. Spinella *et al.*, The TEL62: A real-time board for the NA62 Trigger and Data Acquisition. Data flow and firmware design, IEEE Nucl. Sci. Symp. Conf. Rec., 1 (2014).

Additional material can be found at: https://web2.infn.it/RETINA/index.php/en/

Results shown here have been achieved by "*Retina*", a 3-year project funded by INFN, Division of technological research experiments (CNS5)

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13th Pisa Meeting on Advanced Detectors, La Biodola (Italy), May 24-30, 2015