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VME Rear Transition Module with Backplane Data Access Capability for the ATLAS FTK Upgrade

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This paper describes a data processing board (AUX) designed for the ATLAS Fast Tracker (FTK), a system that does global track reconstruction in ~100 μs. The AUX processes silicon detector hits from 8 pixel and silicon strip layers, with typical data rates of 2 Gbps per layer. Each of 128 AUX boards will send hits to its adjacent pattern recognition board and receive back track roads, narrow regions containing track candidates. For each road, all combinations of 1 hit per layer are fit, a chi^2 cut is applied, and then duplicate tracks are removed. On average, 4 track candidates are fit on the board per nanosecond. The board is a VME Rear Transition Module (RTM) with six large FPGAs from the Altera Arria V family. In order to provide for configuration, setup and monitoring of these chips, a special VME data access feature was developed to provide backplane data transfers to and from the RTMs, while being in full compliance with the VME64xP Specifications. It employs the J2 user-defined feed-through pins to connect with the front module, allowing its slave interface to service FPGAs located both in the front and in the rear. As a result, a crate master, sees devices on this rear card as being part of the corresponding front module.

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