The WaveCatcher Digitizers: High-End Instrumentation for Advanced Fast Detectors

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1. Based on the SAMLONG Analog Memory ASIC
2. Sampling rate ranging between 400 MS/s and 3.2 GS/s.
3. 1024 channels/channel
4. 12 bits of dynamic range
5. Small signal bandwidth > 500 MHz
6. Sampling jitter < 5 ps rms at the system level
7. Up to 64+8-channel synchronous system
8. Advanced Oscilloscope-Like Software (Plug and Play)
9. Windows and Linux C-Library (control and readout)
10. Embedded feature extraction: Baseline, Peak, Charge, CFD (TDC-like mode) ...

Why Analog Memories

Modern high-end ADCs have broken the GS/s frontier but their implementation becomes difficult. Their companion FPGAs have to be high-end and the cost per channel explodes. The use of analog memories like SAMLONG makes it possible to perform high-quality digitizing at low cost and with a low power consumption.

The Sampling MATRIX

Our sampler chip is made of a matrix of E lines and C Columns of analog memory cells. Its main clock doesn’t exceed 200 MHz. It is virtually multiplied by 16 inside the chip thanks to the 64 vertical servo controlled delay line loops (DLL). The input signal is split in 16 branches, each housing a voltage buffer. The chip behaves like an analog circular buffer.

System Features

- Possibility to add as individual DC offset to each channel
- Individual trigger discriminators on each channel
- Programmable programmable bit rate counter on each channel
- External & internal trigger in different modes for coincidence triggering
- 2 extra memory channels for “signal” or “signal on 16-channel board” can be used as additional analog inputs
- Dedicated gate generator on each input
- External clock input for multi-board application (8, 16, 54-channel)
- Embedded USB, UDP and Gigabit optical interfaces (R, G & 64-channels)
- Possibility to upgrade the firmware via USB
- Enhanced charge extraction
- Embedded signal amplifiers and baseline correction
- Embedded digital CFD for time measurement

Trigger & Readout

- Several modes of triggering are available in the WaveCatcher boards and systems.

The 16-channel Board

- The Multi-layer Parallel Interface aims at simplifying the communication between FPgas located at different levels in the system.
- The same firmware decoding blocks are implemented in the FPgas independently of their hierarchy level in the system (same or different boards).
- USB and UDP/Gigabit interfaces are available
- A software library (Windows/Linux) has been developed to handle this communication protocol

Application Examples

- Comparison WaveCatcher vs LeCroy oscilloscope, LAL, France. The goal is to measure the time difference between the laser trigger and the Fasttronics 512-CH-PMT signal
- Characteristics and test bench for SPrinx, LAL, Orsay, France.
- Cell time INL extracted from CFD calibration and using sample INL: 0.15 μm rms

Summary

- AMS CMOS 0.35μm technology.
- Full Custom design
- 2 differential channels
- 1024 = 16/64 cells per channel
- Many modes configurable by a SPI-like serial link
- On-chip DAC’s for line-offset compensation
- “Built-in TDC” to 100,000 transitions, 11 mm2
- TQFP 100x14x14 package

The SAMLONG ASIC

- An analog memory array is running along a twisted delay line (DLL). It drives the recording of signals into analog memory cells.
- Principle of circular buffer: readout can target any memory cell, which can be any subset of the whole channel.