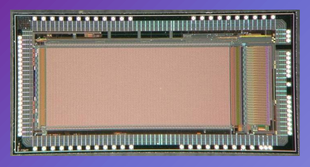

The WaveCatcher Digitizers:
High-End Instrumentation for Advanced Fast Detectors


1


2

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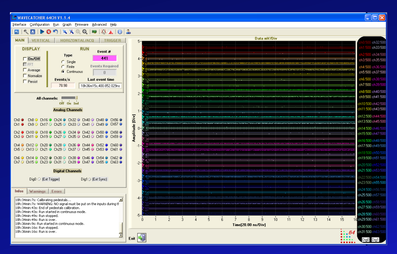
The family of WaveCatcher Digitizers :

2 to 64-channel 12-bit 3.2GS/s oscilloscope-like digitizers, close to the picosecond level in timing precision

- **Based on the SAMLONG Analog Memory ASIC**
- **Sampling rate ranging between 400 MS/s and 3.2GS/s.**
- **1024 samples/channel**
- **12 bits of dynamic range**
- **Small signal bandwidth > 500MHz**
- **Sampling jitter < 5 ps rms at the system level**
- **Up to 64+8-channel synchronous system**
- **Advanced Oscilloscope-Like Software (Plug and Play)**
- **Windows and Linux C-Library (control and readout)**
- **Embedded feature extraction: Baseline, Peak, Charge,CFD (TDC-like mode) …**



2 channels

8 channels

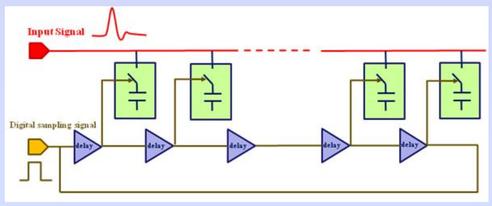
16 channels

64 channels

CAEN :
8 to 16 channels

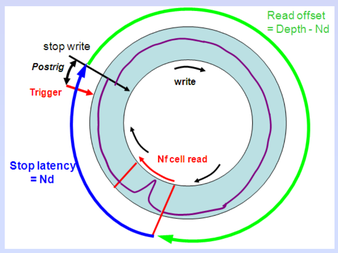
Why Analog Memories

Modern high-end ADCs have broken the GS/s frontier but their implementation becomes difficult. Their companion FPGAs have to be high end and the cost per channel explodes. The use of analog memories like **SAMLONG** makes it possible to perform high quality digitizing at low cost and with a low power consumption.



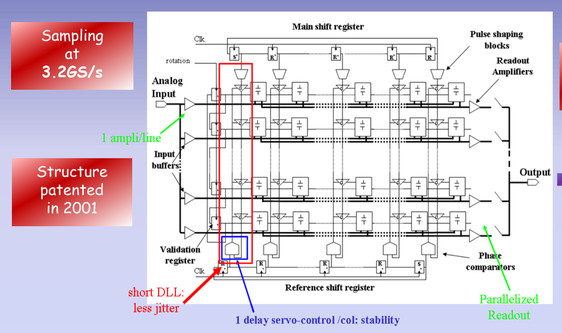
An analog memory: a write pulse is running along a folded delay line (DLL). It drives the recording of signal into analog memory cells.

Principle of circular buffer: readout can target an area of interest, which can be only a subset of the whole channel



The Sampling MATRIX

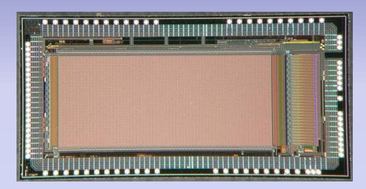
Our sampler chip is made of a matrix of **L lines** and **C Columns** of analog memory cells. Its main clock doesn't exceed 200 MHz. It is virtually multiplied by 16 inside the chip thanks to the 64 vertical **servo controlled** delay line loops (DLL). The input signal is split in 16 branches, each housing a voltage buffer. The chip behaves like an **analog circular buffer**.



Some advantages of the matrix structure:

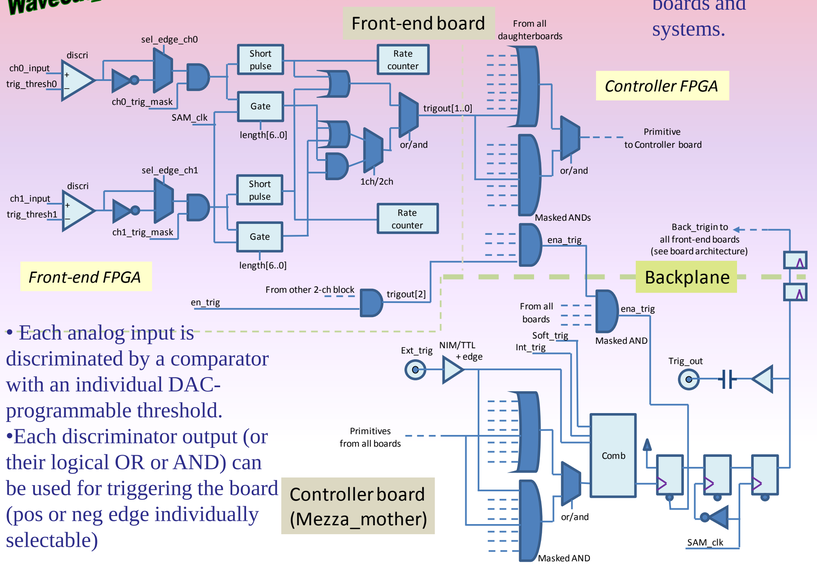
- Servo-controled DLLs permit **accurate timing**, stable with temperature.
- Input amplifier : stable **high input impedance**.
- 1 Amplifier/Line : better Bandwidth/ Consumption Factor Of Merit
- Channel information spread over numerous lines permits **fast readout**.

The SAMLONG ASIC



- AMS CMOS 0.35µm technology.
- Full Custom design
- 2 **differential** channels.
- **1024** = 16*64 cells per channel
- Many modes configurable by a SPI-like serial link.
- On-chip DACs for line-offset compensation
- **"Built-in TDC"**
- 100,000 transistors, 11 mm2
- TQFP 100 14x14 package

Trigger & Readout



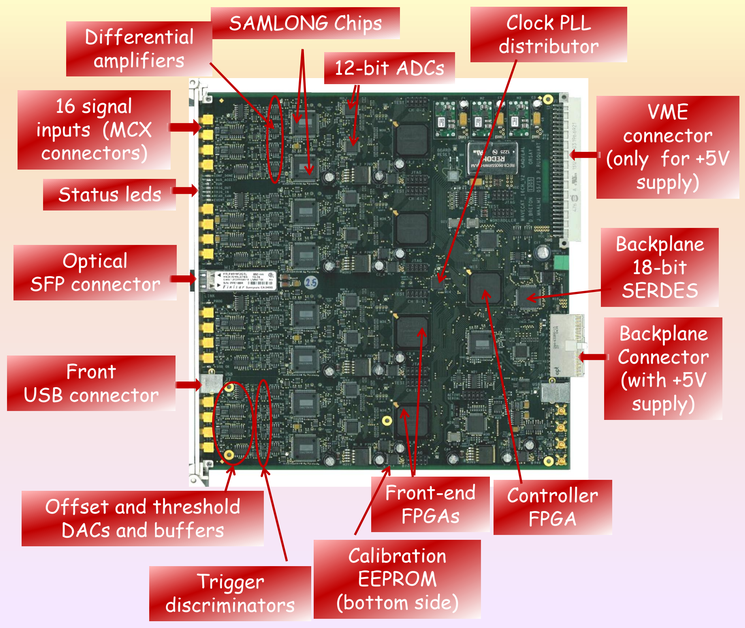
- Each analog input is discriminated by a comparator with an individual DAC-programmable threshold.
- Each discriminator output (or their logical OR or AND) can be used for triggering the board (pos or neg edge individually selectable)

- Several modes of triggering are available in the WaveCatcher boards and systems.

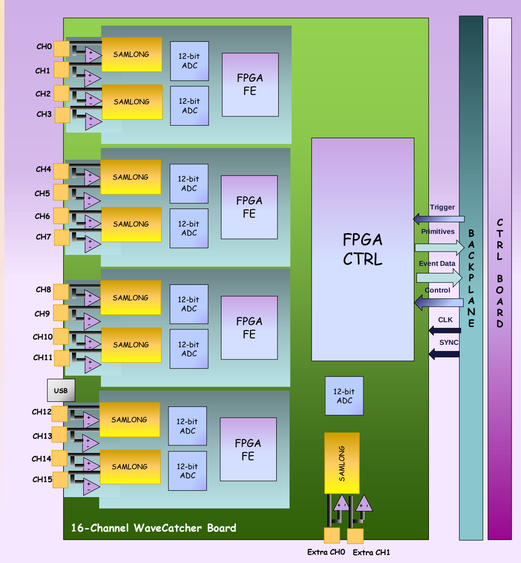
System Features

- Possibility to add an **individual DC offset** to each channel
- **Individual** trigger **discriminator** on each channel
- Integrated **programmable hit rate counter** on each channel
- **External** & internal trigger + different modes for **coïncidence** triggering
- 2 **extra** memory **channels** for « digital » signals on 16-channel board => can be used as additional analog inputs
- One **pulse generator** on each input
- External clock input for multi-board applications (8, 16 & 64-channel)
- Embedded USB, UDP and Gigabit optical interfaces (8, 16 & 64-channel)
- Possibility to upgrade the firmware via USB
- Embedded **charge** extraction
- Embedded signal **amplitude** and **baseline** extraction
- **Embedded digital CFD** for time measurement

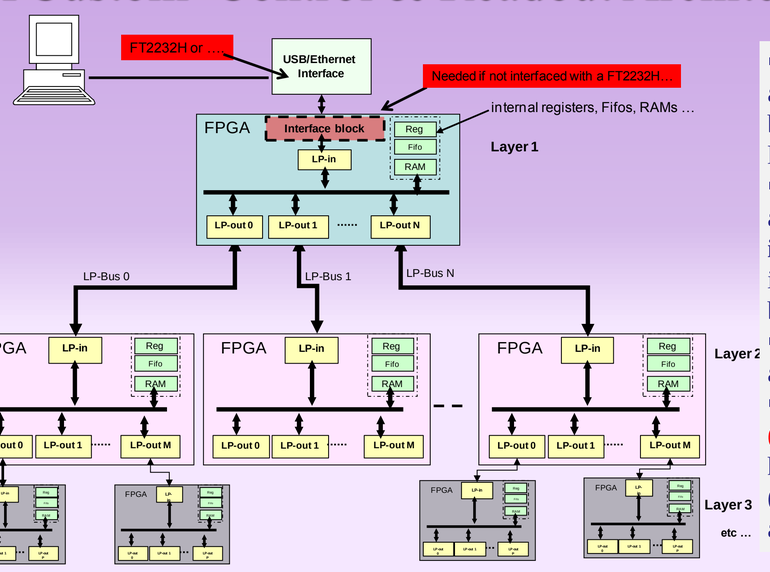
The 16-channel Board



Block Diagram of 16-channel Board



A Custom Control & Readout Architecture and Protocol

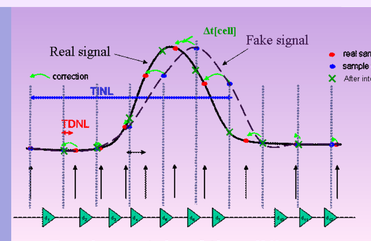


- The **Multi-layer Parallel Interface** aims at simplifying the communication between FPGAs located at different levels in the system.
- **The same firmware** decoding blocks are implemented in the FPGAs **independently of their hierarchy level** in the system (same or different boards).
- **USB and UDP** firmware interfaces are available
- A **Software Library (Usb/Udp_ML)** has been developed to handle this communication protocol (compatible with FT2xx components and the DP83865 Gigabit Phyter)

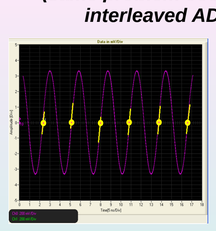
Summary

		Unit
SAMLONG ASIC technology	AMS CMOS 0.35µm	
System number of channels	2, 8, 16, 32, 48, 64	
Power consumption	2.5 (2-ch), 15 (8-ch), 23 (16-ch), 100 (64-ch)	W
Sampling depth	1024 / channel	Cells
Sampling speed	0.4 to 3.2	GS/s
Bandwidth	500	MHz
Range (unipolar)	± 1.25 (with full range individual channel offset)	V
ADC resolution	12	bits
Noise	0.75	mV rms
Dynamic range	11.5	bits rms
Readout time	11 to 66 (depends on number of cells read)	µs
Time precision before correction	< 20	ps rms
Time precision after time INL correction	< 5	ps rms

Time INL Calibration



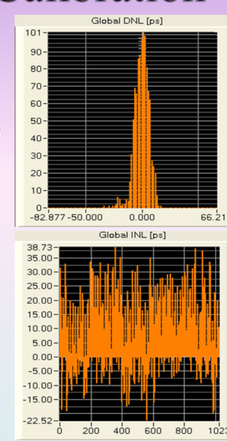
Fundamentals of time INL error (same problem occurs with interleaved ADCs)



Sinewave used for time INL calibration: zero-crossing segments are considered like straight lines

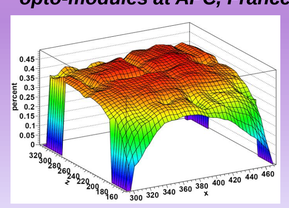
Cell time INL extracted from DNL calibration and used for sample correction: 0.75 ps rms

Time DNL distribution measured by calibration: 6.4 ps rms (based on segment length)

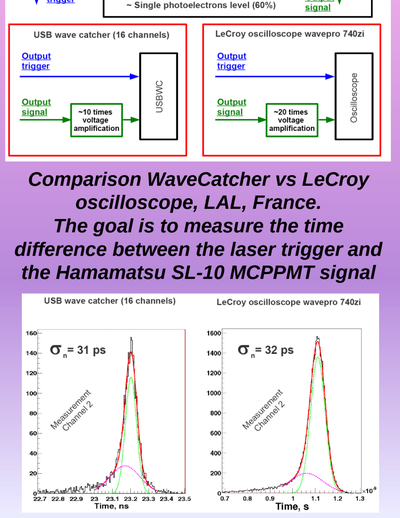


Application Examples

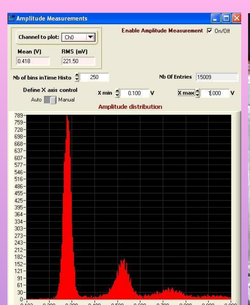
Calibration of ANTARES opto-modules at APC, France



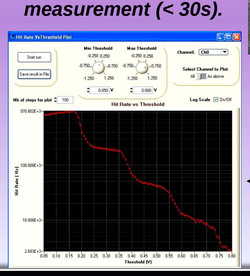
3D efficiency map with 3.10[8] events in less than 3 hours

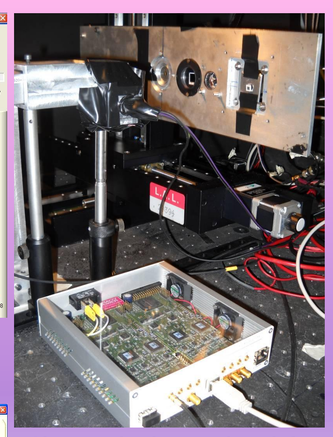


Comparison WaveCatcher vs LeCroy oscilloscope, LAL, France. The goal is to measure the time difference between the laser trigger and the Hamamatsu SL-10 MCPPMT signal



Amplitude distribution performed by firmware measurement (< 30s).





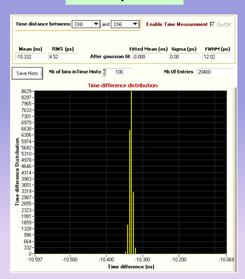
Characterization test bench for SiPMs, LAL Orsay, France. The 8-channel WaveCatcher can be seen on the picture

Result of a hit rate vs amplitude plot. This type of measurement is automatically performed by the software.

Time measurement results

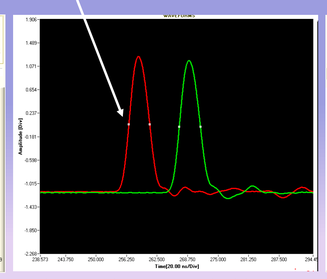
2 pulses, 2.5 ns risetime, 1.2V, Δt ~ 10 ns

4.52 ps rms



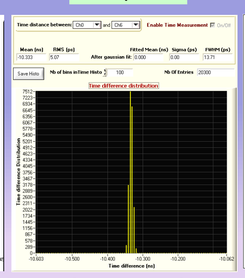
Δt measured by software

CFD points received from firmware



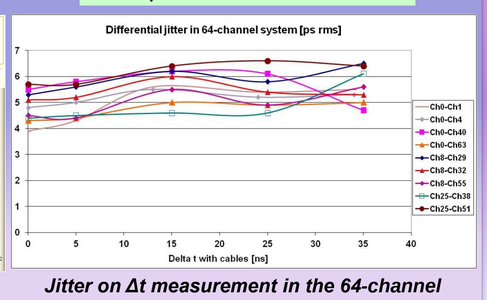
The 2 pulses recorded by the WaveCatcher board

5.07 ps rms



Δt measured by firmware

Differential jitter between channels: 4 to 7 ps rms, almost flat and independent on channel location



Jitter on Δt measurement in the 64-channel system, measured with cables

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