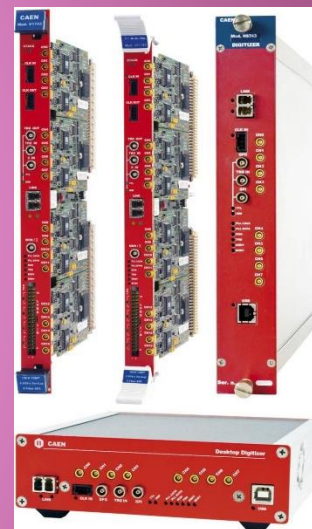
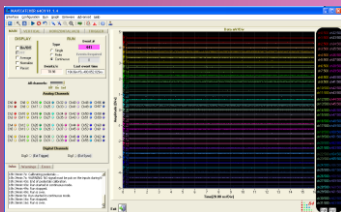


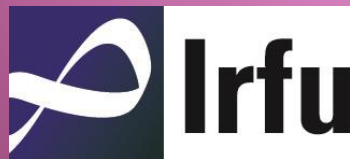


The WaveCatcher Digitizers

High End Instrumentation for characterization of Advanced Fast Detectors



Dominique Breton, Jihane Maalmi, Pascal Rusquart - CNRS/IN2P3/LAL (Orsay)
Eric Delagnes - CEA/IRFU (Saclay)



Frontier Detectors for Frontier Physics, 13th Pisa Meeting on Advanced Detectors, May 2015



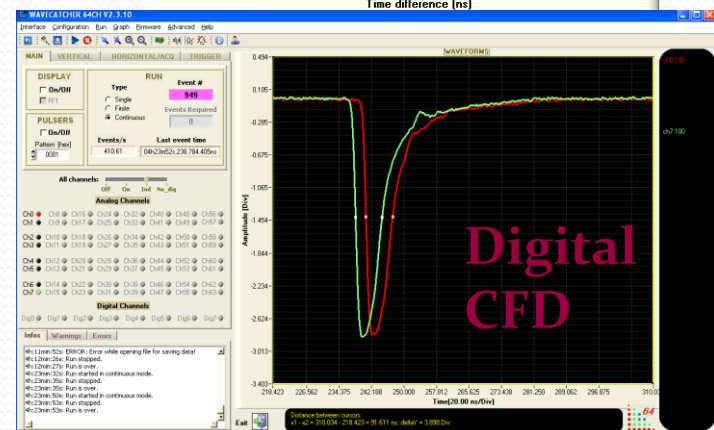
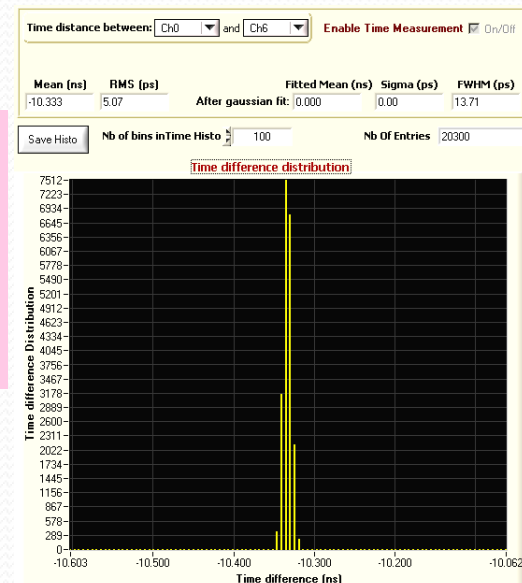
2 to 64-channel Oscilloscope-like Plug and Play Synchronous Systems

- Based on the **SAMLONG** Analog Memory ASIC
- Sampling rate ranging between

400 MS/s and 3.2GS/s.

- 1024 samples/channel
 - 12 bits of dynamic range
 - Sampling jitter **< 5 ps rms** at the system level!
 - Advanced Oscilloscope-Like Software (Plug and Play)
 - Advanced triggering options
 - Individual Rate counters
 - Embedded feature extraction :
- Baseline, Peak, Charge, Digital CFD (TDC-like mode)**

Example :
Jitter on a
 Δt of 10 ns
= 5 ps rms





You are welcome!

Even more if you are interested in:

- Waveform digitizers
- Fast Analog Memories
- Trigger Architecture
- Our custom Readout architecture and Protocol
- System optimisation
- Picosecond Time Measurements
- Detector Characterization

The WaveCatcher Digitizers:
High-End Instrumentation for Advanced Fast Detectors

Dominique Breton¹, Jihane Maalmi², Pascal Rusquart¹ - CNRS/IN2P3/LAL (Orsay)
Eric Delagnes¹ - CEA/DRF (Saclay)

The family of WaveCatcher Digitizers :
2 to 64-channel 12-bit 3.2GS/s oscilloscope-like digitizers, close to the picosecond level in timing precision

- Based on the **SAMLONG** Analog Memory ASIC
- Sampling rate ranging between 400 MS/s and 3.2GS/s
- 1024 samples/channel
- 12 bits of dynamic range
- Small signal bandwidth $> 800\text{MHz}$
- Sampling jitter $< 5\text{ps rms}$ at the system level
- Up to 64-channel **synchrotron** system
- Advanced Oscilloscope-Like Software (Plug and Play)
- Windows and Linux C-Library (control and readout)
- Embedded feature extraction: Baseline, Peak, Charge, CFD (TDC-like mode)

Why Analog Memories
Modern high-end ADCs have broken the OS's frontier but their implementation becomes difficult. Their companion FPGAs have to be high end and the cost per channel explodes. The use of analog memories like **SAMLONG** makes it possible to perform high quality digitizing at low cost and with a low power consumption.

The Sampling MATRIX
Our sampler chip is made of a matrix of 16 lines and 64 columns of analog memory cells. Its main clock doesn't exceed 200 MHz. It is virtually multiplied by 16 inside the chip thanks to the 64 vertical servo-controlled delay line loops (DLL). The input signal is split in 16 branches, each having a voltage buffer. The chip behaves like an analog circular buffer.

The SAMLONG ASIC
• AMS CMOS 0.35µm technology
• Full Custom design
• 2 differential channels
• 1024 = 16*64 cells per channel
• Many modes configurable by a SPI-like serial link
• On-chip DACs for line-off compensation
• "Built-in TDC"
• 100,000 transistors, 11mm²
• TQFP 100 14x14 package

Trigger & Readout
Trigger architecture (schematic diagram) showing the flow from input signals through various logic blocks to the readout system.

System Features
• External modes of triggering are available in the WaveCatcher board and system.
• Push buttons to add or subtract 100 ns to the delay line.
• Built-in trigger system to test on each channel.
• Integrated analog input line to test on each channel.
• External digital input line to test on each channel.
• External digital input line to test on each channel.
• External digital input line to test on each channel.
• External digital input line to test on each channel.

The 16-channel Board
Block diagram of the 16-channel board showing the internal components and their interconnections.

Block Diagram of 16-channel Board
Detailed block diagram of the 16-channel board showing the internal components and their interconnections.

A Custom Control & Readout Architecture and Protocol
Schematic diagram of the custom control and readout architecture and protocol.

Summary
Key performance indicators and system capabilities.

Time INL Calibration
Graphs showing time INL calibration results.

Application Examples
Examples of applications for the WaveCatcher digitizers.

Time measurement results
Graphs showing time measurement results.

Contact: breton@lal.in2p3.fr, eric.delagnes@cea.fr, jmaalmi@lal.in2p3.fr

FRONTIER DETECTORS FOR FRONTIER PHYSICS, 14th Plus Meeting on Advanced Detectors, May 2015