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The 40 MHz trigger-less DAQ system for the LHCb upgrade

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The LHCb experiment will undergo a major upgrade during the second long shutdown (2018 - 2019), aiming to let LHCb collect an order of magnitude more data with respect to run 1 and run 2.
The maximum readout rate of 1 MHz is the main bottleneck of the present LHCb trigger. The upgraded detector foresees apart from major detector upgrades, a full readout into the DAQ, running at the LHC bunch crossing frequency, using an entirely software based trigger.
A high-throughput PCIe Generation 3 based read-out board has been designed to read out the detector at 40MHz. The readout boards will allow a cost-effective implementation of the DAQ by means of high-speed PC network. The network-based DAQ system reads data fragments, performs the event building, and transport data to the High-Level software trigger at an estimated aggregate rate of ~32 Tbit/s. Possibile technologies candidates for high speed network under study are Infiniband and Gigabit Ethernet. Different architecture for the DAQ can be implemented, such as push, pull and traffic shaping with barrel-shifter.
In order the explore and find the best implementation we are performing tests on different platforms and technologies. The event builder evaluator is flexible, to be used on small size test beds and HPC scale facilities, and allows to explore different network protocols.
The architecture of DAQ system and up to date performance results will be presented.

Collaboration

This is collaboration between the INFN Bologna, CNAF and CERN Online Group aiming to develop the DAQ system for the LHCb Upgrade.

Summary

In this presentation we will describe the foreseen architecture for the LHCb DAQ upgrade. We will report about the performance of the PCIe40 interface board to be used to readout the whole detector at 40 MHz. We will present the results of the tests we are performing in order to evaluate the optimal technology and transport protocol for the event-builder. We developed on this purpose software tools, which allow us to easily compare the different industrial-standard protocols and architectures on small as well as large scale HPC infrastructure. We will present the up-to-date results available, achieved by emulating a realistic event-builder.

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