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SPAD Array Chips with Cluster Reconstruction and Fast Full Frame Readout

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We present two versions of single photon sensitive 2D camera chips containing 88 × 88 avalanche photo diodes.
The center-of-gravity of a photon cloud can be immediately reconstructed on-chip or full image frames can be read with up to 400.000 frames per second. The sensors have imaging areas of ≈ 5×5 mm2 covered by square pixels of 56.44×56.44 µm2 with a ≈ 55% fill factor in the latest chip generation. The chips contain a self triggering logic with selectable (column) multiplicities of up to ≥ 4 hits within an adjustable coincidence time window. The photon accumulation time window is programmable as well. First prototypes have demonstrated low dark count rates of < 50 kHz/mm2 (SPAD area) at 10°C for 10% masked pixels. A FPGA based readout board has been designed to allow for intelligent on-the-fly processing of the high data rate. The device could be used in various applications where fast, spatially resolved detection of single photons is required.

Collaboration

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Summary

Single Photon sensitive Avalanche photo Diodes (SPADs) can be included into CMOS chips to create single photon sensitive structures. Two dimensional arrays which deliver the number of fired SPADs per event are available since several years and are being used successfully for the readout of scintillating crystals, for instance for PET scanners or for calorimetry. The available devices offer no intrinisc spatial resolution because all SPADs are summed up. The aim
of our work is to design 2D SPAD array chips with more sophisticated readout concepts to extract more information from single scintillation events. In particular, a fast full frame readout of single scintillation events provides full information (at the price of a high digital data rate which must best be processed immediately).

We have therefore designed two versions of a 2-dimensional SPAD array using the 0.35 µm CMOS technology available at the Fraunhofer Institute for Microelectronic Circuits and Systems (Fraunhofer IMS) in Duisburg, Germany. The arrays have 88 × 88 pixels of (56.44 µm)2 size. The active SPAD region covers 38/55% of the pixels in the two chip versions, respectively. Each pixel further includes a hit discriminator, a local control bit to disable bad cells, a monostable with variable time width (some 10 ns) to generate a column-wise hit-OR signal, a second control bit to exclude noisy cells from the trigger (only in 1st chip version), a hit flipflop with variable gating time, a shift register for hit pattern readout and a digital hit injection for tests without SPAD involvment.
Hit in the 88 columns are flagged to the chip periphery where the number of hit columns is counted in a low-skew circuit. The coincidence time window can be set globally down to ≈ 10ns. Multiplicities up to ≥ 4 from this circuit can be used to open a global shutter time window during which hits in the pixels are accepted. When this accumulation elapses, the hit information is transferred to the pixel shift register flipflop so that the matrix is immediately ready for new events (hit pixels have higher dead times until the SPAD is recharged). The shift register is used to transfer the hit pattern to the periphery. In the full frame readout mode, every

pixel hit bit is sent serially off-chip. In the second chip iteration, this readout has been parallelized with 8 signals and double data rate signaling has been used to achieve a design frame rate of ≈ 400 kHz.
An alternative readout method assigns each pixel to one of four on-chip counters. The assignement pattern is fully programmable through a JTAG interface. The four counter values are buffered in a FIFO and sent off-chip on a single 8b-10b encoded link. By using an appropriate assignment pattern, the four counter signals can be used to reconstruct the center-of-gravity of the hit pattern.

As far as we have analyzed the fabricated first design, the main functionalities operate as expected. The dark count rate of the SPADs is at a fairly low level of of < 50 kHz/mm2 (SPAD area, measured at 10◦ C for 10% masked pixels) despite the dense integration of the SPADs with closeby digital circuitry. In the second design iteration, we have submitted various SPAD design variations to study layout effects on SPAD performance. Thanks to this low dark count rate and the multiplicity logic, the rate of coincidences ≥ 4 for a coincidence time window of ≈ 20ns is in the range of few Hertz only even at 30◦C, making self triggered operation easy with no dead time introduced by fake triggers. The device can be used to identify crystals in scintillator arrays. This has been done with high efficiency using a LYSO array with only 0.48 mm pitch (10 mm height), read out in self triggered mode at room temperature.

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