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An FPGA-based trigger for the MEG II experiment

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Frontier applications both in high energy and medical physics often require to develop custom electronic to be tailored to the specific detection technique being used, so as to accomplish either trigger or data acquisition (DAQ) tasks. For instance, this used to be the case of the first phase of the MEG experiment, where detector signals were split
to seperate trigger and digitizer VME modules. For the phase two of the experiment, we decided instead to develop a new, multi-purpose system, conceived to operate both functions on 3U Eurocard boards plugged to a custom backplane with point-to-point connection for data readout and command handshaking.

Here we focus on the on-line reconstruction of
detector signals and event selection at a trigger level. Basic algorithms are implemented on a Xilinx Spartan6 FPGA, hosted on the same board as the DRS Gigasampler. Detector signals are sampled by a slower digitizer, namely a 100 MHz, 14-bits FADC, to continuously feed the on-board FPGA. Data from different crates, each connected to a set of detector channels, are then
gathered by trigger concentrator boards (one per crate) and further processed by higher-level algorithms to issue a trigger, in the case of a candidate signal event, within 450 μs from event
occurrence. We describe the major features of the system and its performances in terms of selection efficiency and background rejection. We also discuss about possible extension of such a system to other applications than particle physics.

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