An FPGA-based trigger for the phase II of the MEG experiment

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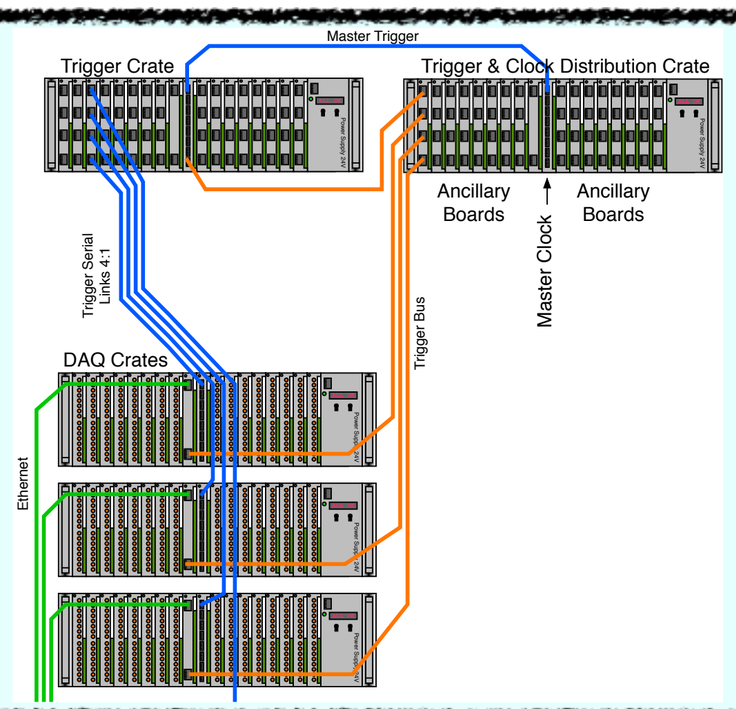
System overview

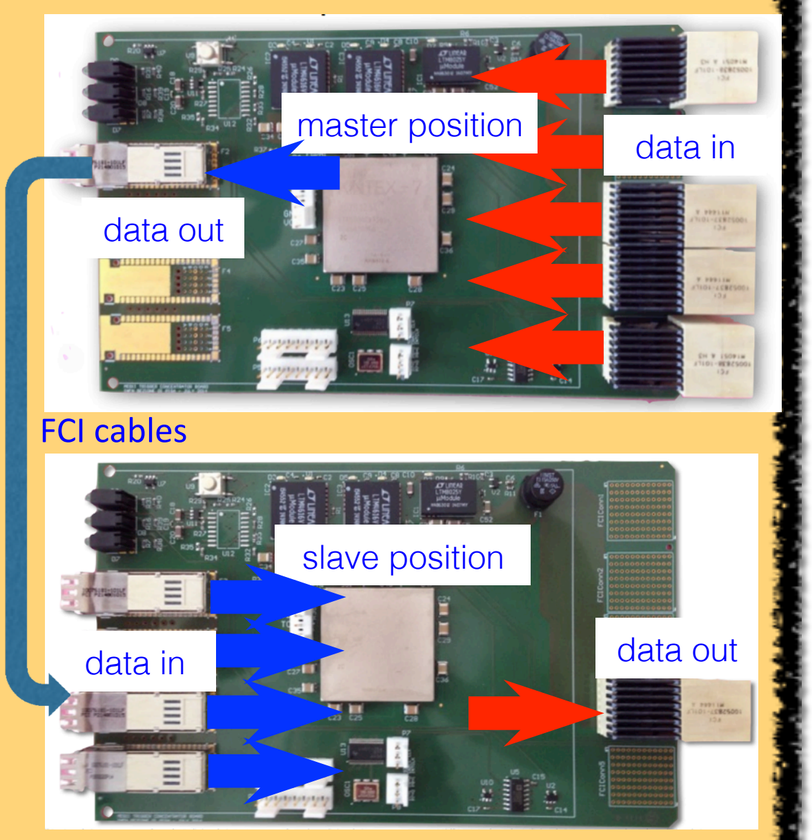
As in the case of phase I, the trigger task in MEG is accomplished by exploiting a fully digital approach[1][2]. Detector signals are sampled by commercial FADC (100 MHz sampling) and processed by means of reconstruction algorithms implemented on Xilinx FPGA, with the twofold objective of maximizing the background suppression (while taking the efficiency close to 1) and minimizing the latency to less than 450 ns (so as to fit with the memory depth of DRS4 chips running at ~2 GS/s).

FPGA are mounted on 3U custom boards arranged on a hierarchical structure. At the bottom stage, WaveDream Boards (WDB)[3] digitize detector signals and perform basic operations (pedestal subtraction, fast discrimination, gain compensation, etc.) implemented on Xilinx Spartan6 FPGA. Digital outputs are then serialized and transmitted by using the SERDES protocol to a Trigger Concentrator Board (TCB), via point-to-point LVDS connections with Gbit/s capability routed on a custom backplane of a DAQ crate. Pieces of information from individual crates are then gathered by higher level TCBs, hosted on the slots of a dedicated crate (the Trigger Crate), and further assembled to provide combined detector information to the master TCB, which is in charge of generating START and STOP to the whole system.



Trigger Concentrators (TCB)

In order to minimize design and production costs, we decided to use the same 12-layer layout for these boards, independent of the role each one plays in the trigger hierarchy.
TCBs diversify each from the others due to the firmware operating on an on-board Xilinx Kintex7 FPGA. Apart from reconstruction algorithms, which depend on individual subdetectors, other features might depend on the slot assignment. For instance, the direction of I/O data lines is set from the backplane to the FPGA if the TCB is located at the center of the crate (Master position in all the crates), while it is the other way round for higher level TCBs hosted in a Slave position in the Trigger Crate.

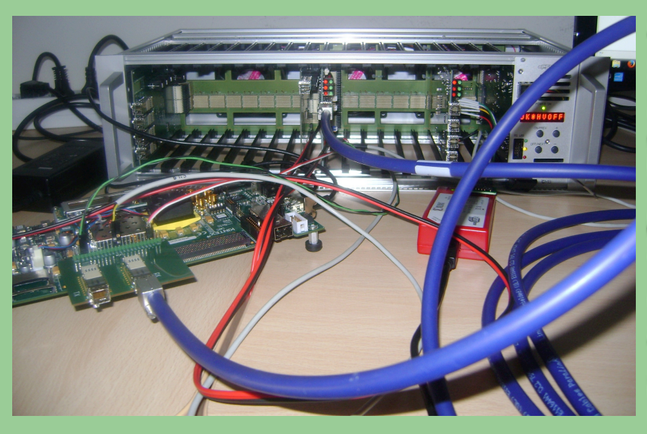


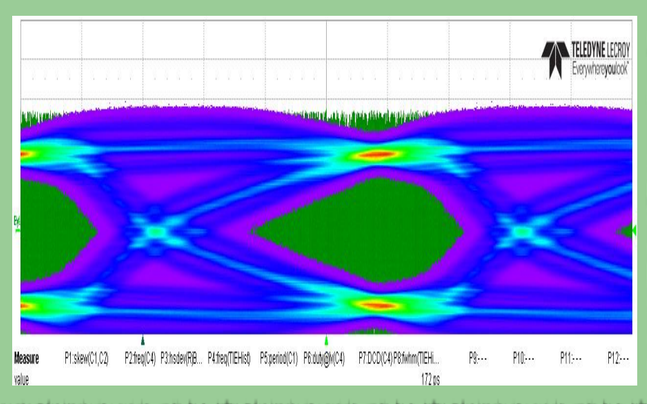
Event reconstruction

Event selection relies on an on-line reconstruction of decay product observables, like momenta, relative timing and direction. Logic equations are mapped in FPGA cells and implemented at 100 MHz so as to be synchronous with the FADC data flow.
An estimate of γ-energy is obtained by the linear sum of pedestal-substracted signal amplitudes of MPPC photosensors, each weighted according to their own gain, which is efficiently implemented by using DSP sheets in the FPGA. An increased ADC resolution (12 vs. 10 bits) coupled with an improved single photoelectron response of new sensors will allow us to achieve a resolution better than that of phase I (which used to be ~7% FWHM @ 52 MeV), the final resolution eventually depending on running conditions.
Concerning the relative $e^+ - \gamma$ timing, we will benefit from using WDB comparators coupled to each input signal (on both LXe and TC), whose latch time can be further refined by implementing look-up tables on the FPGA to correct for time-walk effects. Also in this case we expect the resolution to be significantly improved from the former 3 ns.
Moreover, enhanced imaging capability due to a finer detector segmentation (smaller LXe photosensors and TC tiles) will induce a stronger angular correlation of decay products to further constrain the decay kinematics.

TCB prototype tests

Prototypes of the TCB (and of the ancillary Clock distribution boards as well) were built to test crucial aspects of the new system, first of all data transmission. Serialization is in order to minimize the number of nets to be routed in the backplane. So the higher the serialization factor, the wider the information bit range to be transmitted to higher level boards, which implies better resolution and background rejection capability.
We successfully tested (bit error fraction < 10^{-12}) the eight TCB Slave-to-Master links up to 10:1 serialization factor (DDR SERDES protocol), for an overall 128 Gb/s data throughput to the TCB master. The test chain included a Kintex7 evaluation kit where to send and verify the proper transmission ofmaster output by means of a MicroBlaze μ-processor.





Trigger levels & background rates

- 1st level

Due to their prompt response, pieces of information coming from scintillation detectors (namely Liquid Xenon calorimeter and Timing Counter) are immediately available to the trigger. Within 450 ns since event occurrence, an L1 trigger is issued to STOP the DRS wave and start digitization of DRS analog cells. Conservative estimates of L1 rates (i.e., not taking into account reconstruction improvements yet) can be obtained by just scaling phase-I rates to almost doubled muon stop rate; therefore R(L1) ~ 30 Hz.

- 2nd level

Being related to tracking information, which is later by ~200 ns than other detectors due to electron drift time, the reconstruction of positron momentum is meant to be used only at a second trigger level. During DRS digitization (lasting O(10 μs)), positron patterns can be recognized by means of an associative memory instantiated in the FPGA of higher-level TCB: track segments can then be Kalman-filtered by the master TCB, which can issue an L2 to enable data readout and recording if any of these segment matches the stamp of a signal positron.

References

[1] L. Galli et al., JINST 8 (2013) P01008
[2] L. Galli et al., JINST 9 (2014) P04022
[3] S. Ritt et al., contribution to this conference