## FRONTIER DETECTORS FOR FRONTIER PHYSICS <br/> on Advanced Detectors <br/> or>



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## Advanced monolithic pixel sensors using SOI technology

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We are developing monolithic pixel detectors using 0.2 um FD-SOI pixel process. It aims at developing the next generation pixel detector for the future high energy physics experiment, space application, material science, medical application and so on. An SOI wafer is utilized for sensor and electronics. The top silicon is used for SOI-CMOS circuit, and the substrate is used for a radiation sensor. There is a buried oxide layer between two silicon materials, and these are connected each other through Tungsten via. SOI-CMOS circuit has smaller parasitic capacitance compared with bulk CMOS, and therefore high-speed, low noise and low power circuits can be fabricated. Since a bump bonding is not used, the sensors have high gain with smaller pixel size. SOI wafers are fabricated from two silicon wafers using Smart Cut™ by SOITEC. We have applied several types of wafers for the substrate, Czochralski (CZ), float-zone (n- and p- type FZ), and double SOI. KEK has performed the development project since 2005 and organizes Multi Project Wafer (MPW) runs once or twice a year and many universities and institution all over the world are participating. Several types of integration-type pixel sensor and counting-type pixel sensor have been developed with the pixel size of 8-64 microns. The characteristics of the detectors were investigated using radiation sources, X-rays and high-energy charged particles. In this presentation, recent progress and status of the development will be shown.

## Collaboration

The SOIPIX collaboration

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