Advanced monolithic pixel sensors using SOI technology

T. Miyoshi¹, Y. Arai¹, M. Asano², Y. Fujita¹, R. Hamasaki³, K. Hara², S. Honda², Y. Ikegami¹, I. Kurachi¹, S. Mitsui⁴, R. Nishimura³, K. Tauchi¹, N. Tobita², T. Tsuboyama¹, M. Yamada¹ and the SOIPIX collaboration

¹High Energy Accelerator Research Organization (KEK)
²Univ. Of Tsukuba, ³SOKENDAI, ⁴Kanazawa Univ.

http://rd.kek.jp/project/soi/
Outlines

SOI monolithic pixel sensors
KEK DAQ system and performance
Current issues and solutions
Sensor performance (Integration-type pixel sensors)
Future plan and summary

MX1655
(FY13-1)

MX1711
(FY13-2)

INTPIX7
(18 mm x 18 mm)

SPRiT
(SOI Portable Radiation imaging Terminal)

FPIXb
The features of SOI monolithic pixel sensor

- No mechanical bump bonding. Fabricated with semiconductor process only
- Fully depleted (thick & thin) sensing region with low sense node capacitance (~10 fF@17 μm pixel) → high sensor gain
- SOI-CMOS; Analog and digital circuit can be closer → smaller pixel size
- Wide temperature range (1-570K)
- Low single event cross section
- Technology based on industry standards; cost benefit

SOI Monolithic pixel sensor
SOI=Silicon on insulator

Insulator (SiO₂) →

Low R Si

High R Si

Targets
High-Energy Physics
X-ray astronomy
Material science
Non-destructive inspection
Medical application

SOI=Silicon on insulator

Targets
High-Energy Physics
X-ray astronomy
Material science
Non-destructive inspection
Medical application
Process Summary

- KEK organizes MPW runs once/twice a year
- Mask is shared to reduce cost of a design
- Including pixel detector chip and SOI-CMOS circuit chip

<table>
<thead>
<tr>
<th>Process (Lapis Semiconductor Co. Ltd.)</th>
<th>0.2μm Low-Leakage Fully-Depleted (FD) SOI CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 Poly, 5 Metal layers (MIM Capacitor and DMOS option)</td>
</tr>
<tr>
<td></td>
<td>Core (I/O) voltage : 1.8 (3.3) V</td>
</tr>
</tbody>
</table>

| SOI wafer (200 mm φ =8 inch)                     | Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick |
|                                                  | Buried Oxide: 200 nm thick |
|                                                  | Handle wafer thickness: 725 μm \(\rightarrow\) thinned up to 300 μm (Lapis) |
|                                                  | or ~50 μm (commercial process) |
|                                                  | Handle wafer type: NCZ, NFZ, PCZ, PFZ, double SOI |

| Backside process (2011~) | Mechanical Grind \(\rightarrow\) Chemical Etching \(\rightarrow\) Back side Implant \(\rightarrow\) Laser Annealing \(\rightarrow\) Al plating |
Sensor test and DAQ system

Detector board

On package < 6mm-sq

On circuit board > 6mm-sq

DAQ board

SEABAS1

SEABAS2

100Mbps

1Gbps
DAQ software & GUI

ROOT on linux
Single thread scheme (2008-)

ROOT+QT+OpenCV(+picojson)+MSVC
Multi-thread scheme (2014-)

NFZ-INTPPIX4(FY2009) @ 150V
17µm pixel size x 832x512
Pixel scan time 400 ns/pixel
Monochromatic
X-ray 33.3 keV

trimmer 65Hz, compressed
INTPIX4 still images with up-to-date system

INTPIX4+SEABAS2, 4ms x 2000fr, 150V, scan time 320ns/pixel
33.3keV monochromatic X-ray KEK Photon Factory BL-14C1

* INTPIX4 size ~14x9mm
Current issues

1. Additional pixel process
2. Improved SOI wafer
Various Implantation Options in Sensor part and Double SOI

Double SOI (DSOI) STEM image

Top SOI: SOI-CMOS

Middle SOI: Additional shield layer

p/n various doping density

Shield the back-gate effect / optimize charge collection efficiency

Nested-well process (Increase crosstalk?)
Current issues and solutions

1. **BPW process**: effective to analog circuit in a pixel
2. **Double SOI wafer**: effective to digital circuit in a pixel
3. **Additional process**: improve charge collection efficiency

**Buried P-Well (BPW)**

- **Electric Field**
- **Compensate charge accumulation**
- **Reduce coupling capacitance**

**Radiation Damage**

- **Hole Trap**

**Sensor-Circuit Cross Talk**

- **SiO₂**
- **another SOI layer**
Breakdown voltage: double SOI sensor I-V measurement

**Double SOI 1\textsuperscript{st} trial**

- double SOI INTPIX3g (T=23deg)
- 60V

**Double SOI 2\textsuperscript{nd} trial**

- MX1594-D1J-DSOI-3 INTPIXh2
- 160V

**3\textsuperscript{rd} & 4\textsuperscript{th}**

- MX1655D-1J-DSOI INTPIX7 ID#24
- RSTx=1.8V
- 110V

**5\textsuperscript{th}**

- MX1786D-1J-DSOI INTPIX8
- P-type sensor
- 2015(up-to-date)
- Almost the same as NCZ/NFZ cases

**Treatment of edge of SOI chip is incomplete.**

Recover breakdown voltages: Similar to the single SOI case
FET threshold shifts and compensation in DSOI

IV curves of an NMOS (2MGy irradiated) with Changing VDSOI2

Residual of Vth shifts of various FET types (FETs grouped into 3 in VSOI2 setting)

K. Hara et al., ”Initial Characteristics and Radiation Damage Compensation of Double Silicon-on-Insulator Pixel Device,”, PoS(VERTEX2014)033.
N-type Double SOI pixel sensor

Response to infrared laser of 1064 nm wavelength and 10 ns pulse duration.

The pixel images after 100 kGy could not obtain but recovered with VSOI2=-10V.

The average ADC count as function of the square root of the bias voltage for sensor.

- Obtained similar linearity and sensitivity to pre-irradiation with VSOI2=-10 V.

S. Honda et al., TIPP12014, 2-6 June 2014, Amsterdam
PIXEL2014 presentation by M. Yamada
SOI Pixel sensor with N-type, P-type (and double SOI wafers)

Spatial resolution study using NFZ-FPIXb
P-type sensor study using PFZ-INTPIX7 compared with NFZ-INTPIX7

NFZ-FPIXb
Front illumination

NFZ/PFZ-INTPIX7
Front illumination

KEK-PF monochromatic X-ray 16 keV

X-ray target (Cu)

sample

slit1
slit2

500mm
FPIXb

INTPIX7

Pixel size 8 um x 512 x 192 pixels

Pixel size 12 um x 1408 x 1408 pixels

4Tr.

~10Tr.
Spatial resolution

X-ray test chart + X-ray tube

• Cu 8keV, 20kV, 2mA, front illumination, bias 100V
• Ratio 16μm slit,

INTPIX4(17μm): 0.57, FPIXb(8μm): 0.83

INTPIX4

FPIXb

16μm zoom-in
Spatial resolution (2)

JIMA chart (RT RC-05)
Au thickness 1um (very thin!)

X-ray tube: Target Cu

NFZ-FPIXb
Cu 20kV 10ma
Backbias 100V
1ms x 2000fr.

8um slit can be seen
Energy resolution

- X-ray spectra Am241 at room temperature
- Energy resolution (FWHM) @13.9keV

**INTPIX4 CZN**: 1.87 keV (13.4%), **FPIXb FZN**: 0.80 keV (5.8%)
PFZ SOI sensor has high leakage current and low breakdown voltage. Modification of P-type wafer fabrication process is required.
Summary and future plan

SOI pixel sensor development since 2005
SOI pixel sensor system with Gbit Ethernet (SEABAS2) works fine

Current issues:
The back-gate effect will be suppressed by BPW process or double SOI
Radiation hardness can be improved with double SOI

Initial test of double SOI, N-type, P-type sensors was successful
All wafers need to be improved, especially p-type wafer

Future plan:
Crosstalk study must be done with counting-type pixel sensors
Charge collection issue must be solved using novel idea of p/n implantation
Thank you for your attention!
Supplement
SOI Wafer for monolithic sensor

Smart cut™ by Soitec

High Resistivity Silicon:
- N-type Czochralski, NCZ, 0.7 kOhm-cm, 300 μm-thick
- N-type Float Zone, NFZ, 2-7k Ohm-cm, 500 μm-thick
- P-type Czochralski, PCZ, 1k Ohm-cm, 300 μm-thick
- P-type Float Zone, PFZ, 2-40k Ohm-cm, 500 μm-thick
Double SOI (DSOI) pixel sensor

Double SOI N-type sensor (2011-2013) MPW11(MX1501), 12-1(MX1542), 12-2(MX1594)
Double SOI P-type sensor (2014-) MPW13-1(MX1655), MPW13-2(MX1711), MPW14(MX1786), MPW15-1(MX1850)