Real time tracking with a silicon telescope prototype using the “artificial retina” algorithm

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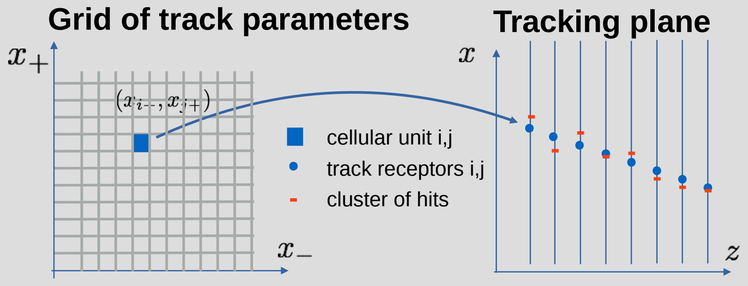
Abstract: we present the first prototype of a silicon tracker using the “artificial retina” for fast track finding. The algorithm, based on extensive parallelization, is implemented on commercial FPGAs and allows to reconstruct real time tracks with offline-like quality and <1μs latencies. The modularity permits to design a system able to operate at the 40MHz LHC crossing rate.

Retina Algorithm

- The “artificial retina” algorithm[1] is inspired from the neurobiological mechanism of recognition of edges in mammals visual cortex
- It is higly parallelized and a hardware implementation is possible using commercial FPGAs[2]
- A strongly pipelined architecture allows sub-μs latencies

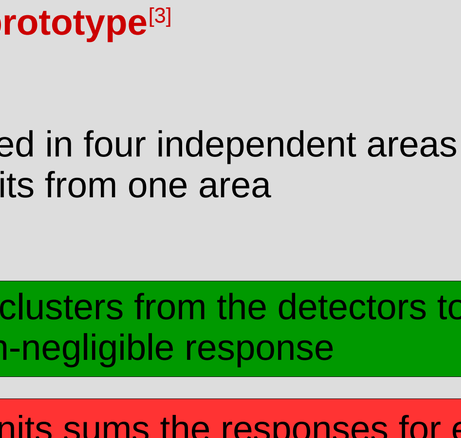
- A **grid of cellular units** covers the space of track parameters
- Each cell is associated with a set of **track receptors** in the tracking plane

Grid of track parameters **Tracking plane**



- The cells, **in parallel**, evaluate and sum the responses to the clusters → **“Weight function”**

Receptor response to cluster

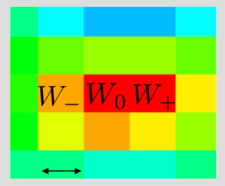


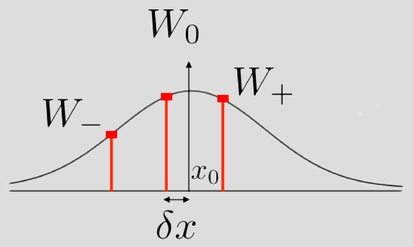
Excitation of the (i,j)-cellular unit

$$W_{ij} = \sum_k \exp\left(-\frac{s_{ijk}^2}{2\sigma^2}\right)$$

- **Local maxima** are found
- **Track parameters** are separately obtained **via interpolation** of the Weight function along the grid axes

Interpolation of the Weight function



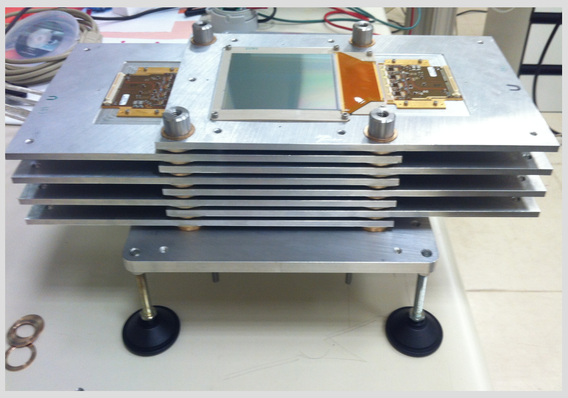


- The interpolation provides **offline-like quality tracks** even with a coarse grid

Silicon telescope

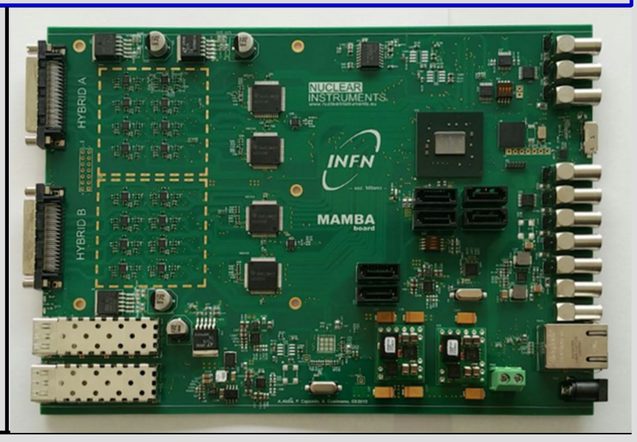
- 8 **single-sided** silicon strip sensors

- STM OB2 sensor:
  ~10x10cm² active area
  512 strips
  183μm pitch
  500μm thickness

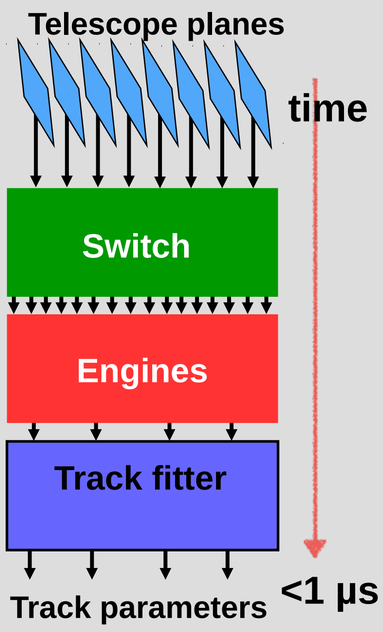


MAMBA board - DAQ+Retina

- **Custom board** designed and produced in Milano
- Based on **Xilinx Kintex 7 FPGA**
- 8 Beetle Chips (2 sensors) readout
  → **4 boards required**
- Readout rate limited at 1.1MHz by Beetle chips maximum trigger rate
- **On-board Retina algorithm**



“Artificial retina” architecture



First artificial retina tracking prototype[3]

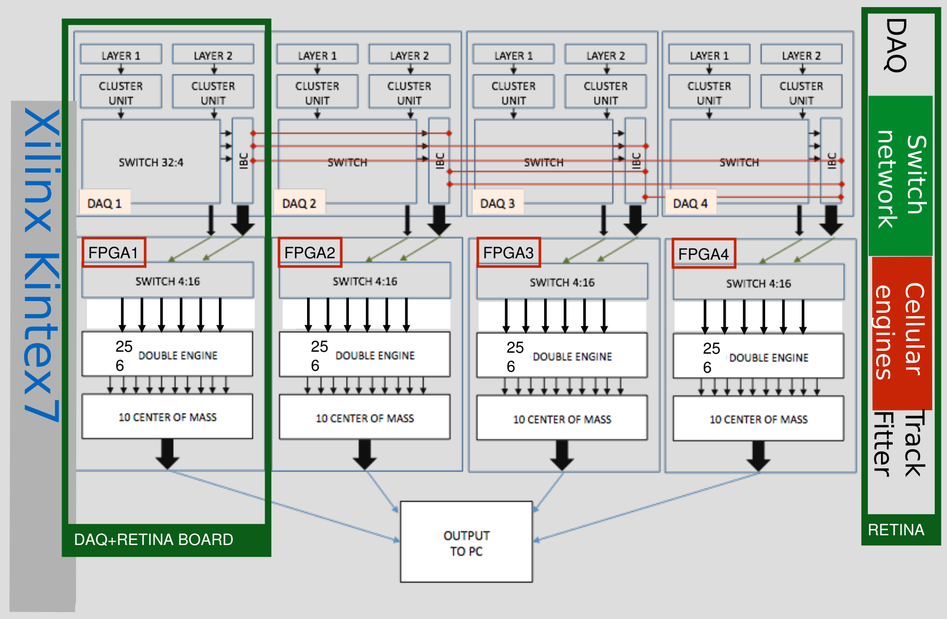
Modular system:
→the parameter space is divided in four independent areas
→each FPGA hosts cellular units from one area

Three main blocks:

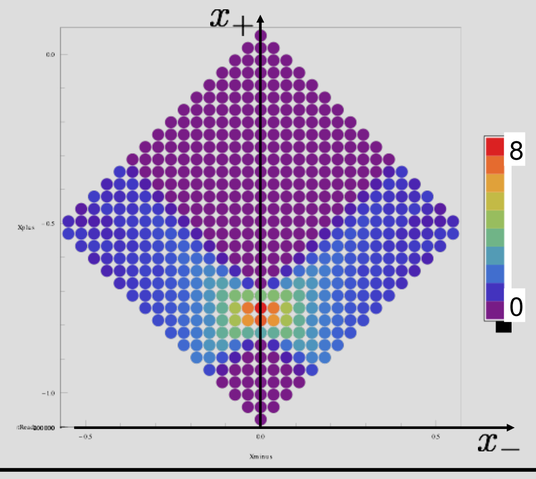
→**Switch**: delivers, in parallel, clusters from the detectors to cellular units with expected non-negligible response

→**Engines**: a pool of cellular units sums the responses for each incoming cluster.

→**Track fitter**: provides the track parameters via interpolation of adjacent cell Weight values near the found local maxima



Retina response



- **Typical Weight distribution** for a single track event
- Data from **FPGA simulation** of the “artificial retina” architecture
- Retina **resolutions are comparable to offline**-reconstruction resolutions

Results and future plans

- **Artificial retina algorithm implemented on custom DAQ+Retina boards, equipped with commercial FPGAs (Xilinx Kintex 7)**
- **Retina architecture succesfully tested up to 40 MHz track rate with low level FPGA simulation**
- **Full prototype functionalities to be tested on beam this summer**

References:
[1] L. Ristori, NIM A 453 (2000) 425-42
[2] A. Abba *et al*., LHCb-PUB-2014-026
[3] N. Neri *et al*., POS(TIPP2014)199

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