13th PISA Meeting on Advanced Detectors

Elba, 25-30.5.2015

Depleted CMOS Pixels
- for LHC – pp – Experiments

Norbert Wermes
University of Bonn

(representing ATLAS CMOS Pixel Collaboration)

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SiLAB
Silizium Labor Bonn

Outline

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Depleted CMOS Pixels

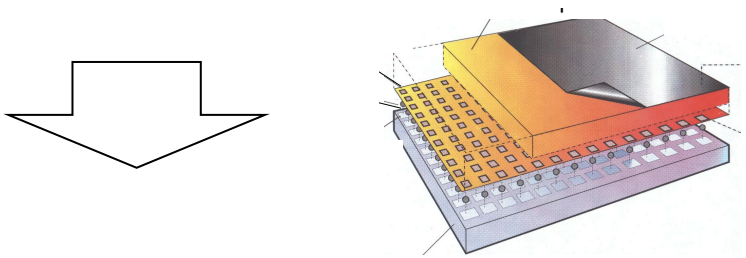
… why and how

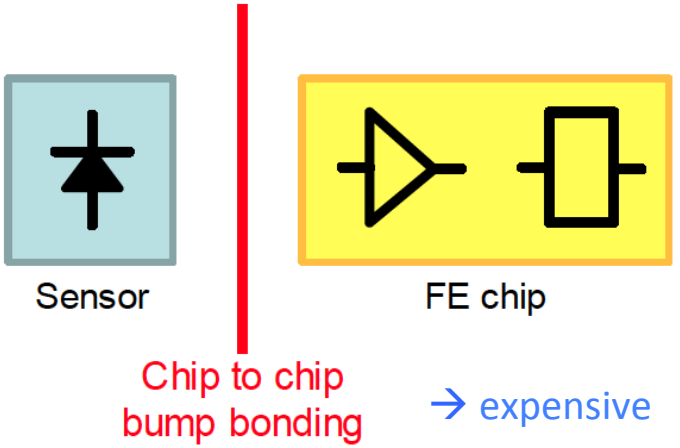
… technologies

… results from prototyping R&D

From LHC - HYBRID pixels → depleted CMOS pixels

- Standard HYBRID pixels
  - various sensors: planar-Si, 3D-Si, diamond
  - mixed signal R/O chip (FE-I3, FE-I4, ROC ...)





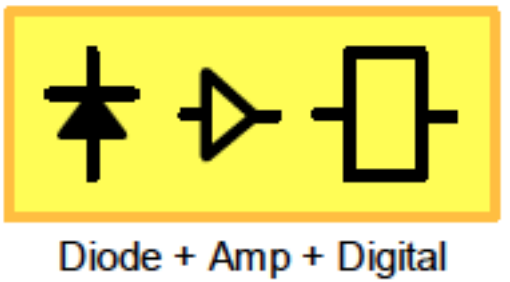
- Monolithic Active Pixel Sensors
  - **MAPS** using CMOS with Q-collection in epi-layer (largely by diffusion → recent advances)
  - Depleted **DMAPS** using **HR** substrate or **HV** process to create depletion region:

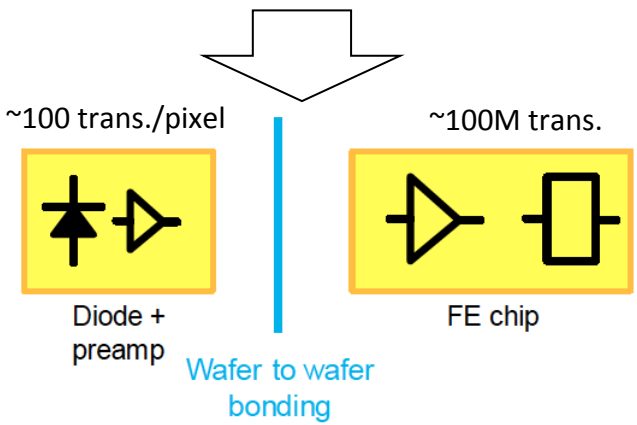
$$d \sim \sqrt{\rho \cdot V}$$

  - CMOS on **SOI**

- currently also: "smart" pixel matrix bonded to FE-chip: **CCPD**

this talk





Rate and radiation challenges for pixel detectors

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	BX time	Particle Rate	NIEL Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	Mrad per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	2×10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	25	10000	2×10^{16}	> 500
LHC Heavy Ions (6×10^{27} cm^{-2} s^{-1})	20.000	10	$>10^{13}$	0.7
RHIC (8×10^{27} cm^{-2}s^{-1})	110	3.8	few 10^{12}	0.2
SuperKEKB (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	0.4

assumed lifetimes:
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

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Monolithic Pixels

lower rates
lower radiation
smaller pixels
less material
better resolution

DEPFET: Belle II
MAPS: STAR@RHIC
and future
ALICE ITS

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focus in this talk (CMOS pixels for LHC-pp)

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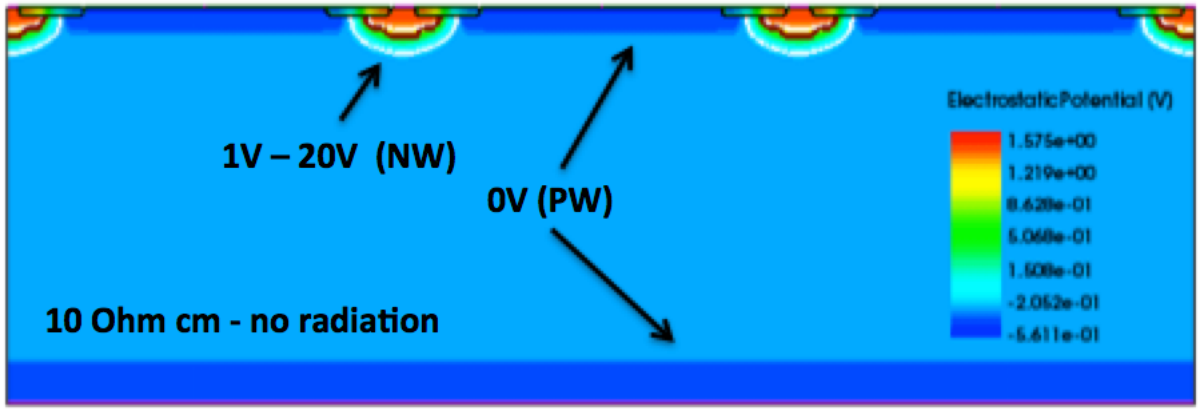
TCAD simulations: resistivity – voltage – fill factor



Substrate: 10 Ωcm – 2kΩ cm
Nwell: 1V – 20 V
Pwell: 0V

from Tomasz Hemperek

TCAD simulations: resistivity – voltage – fill factor

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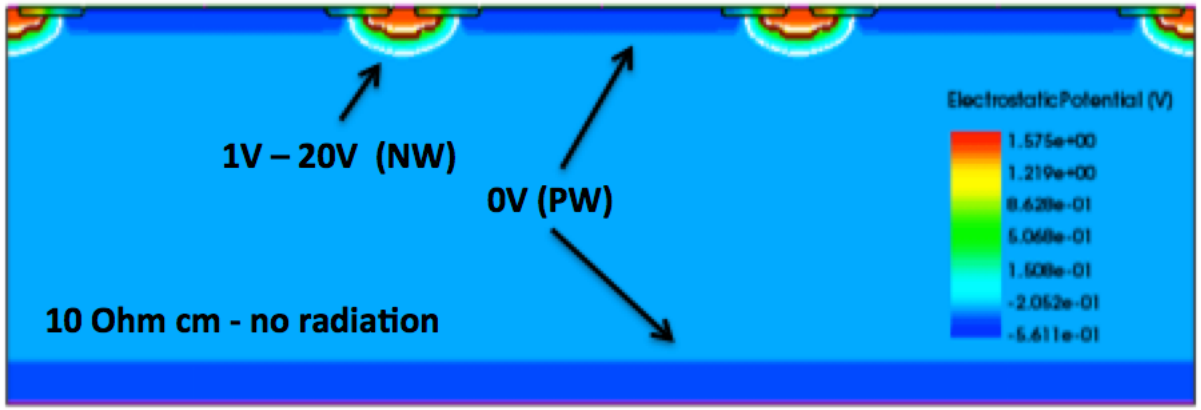

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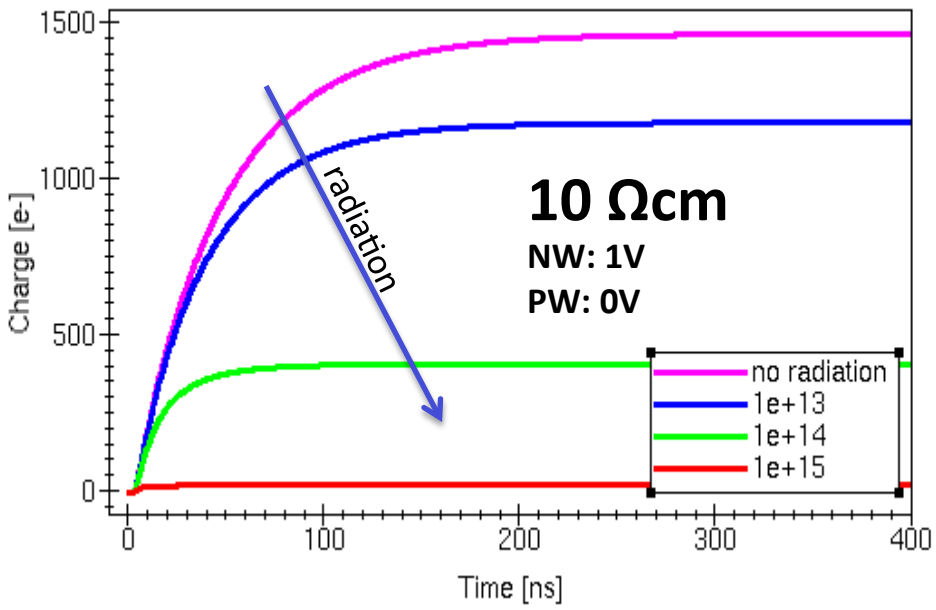
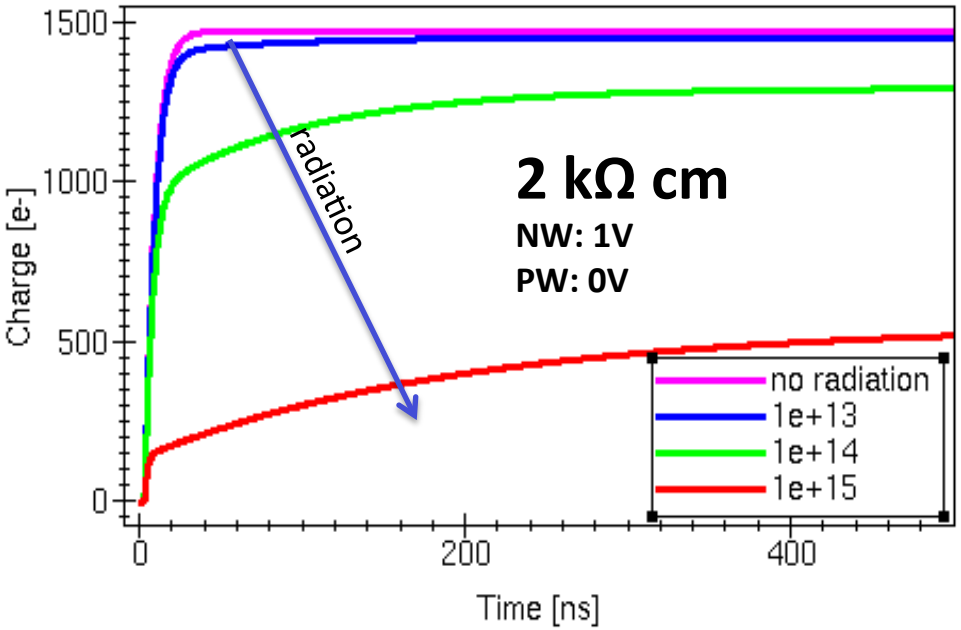
low resistivity



high resistivity



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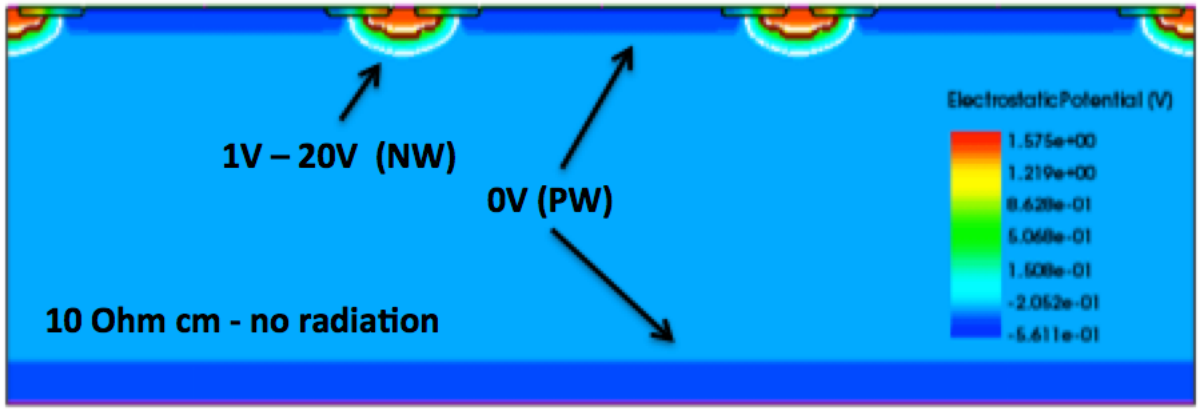

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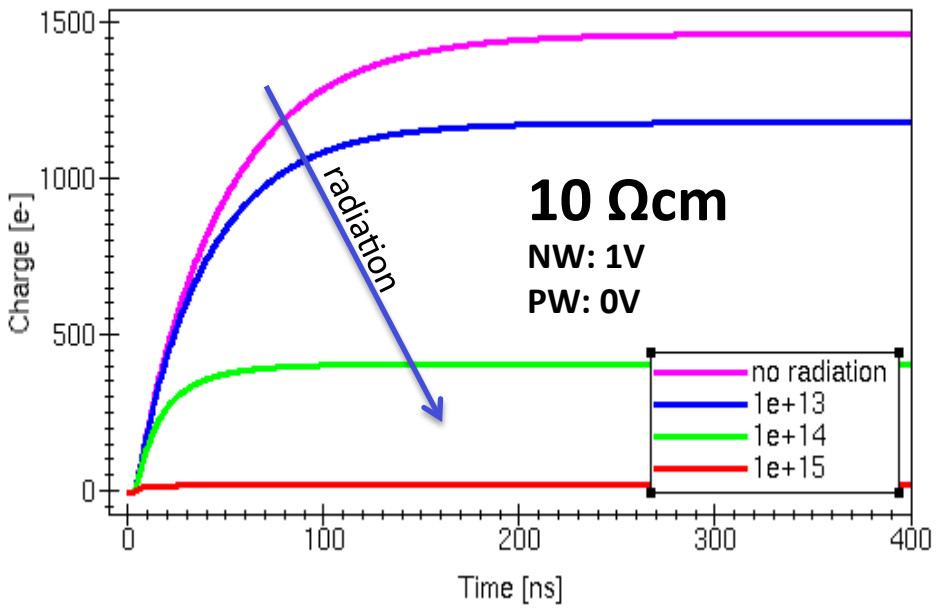
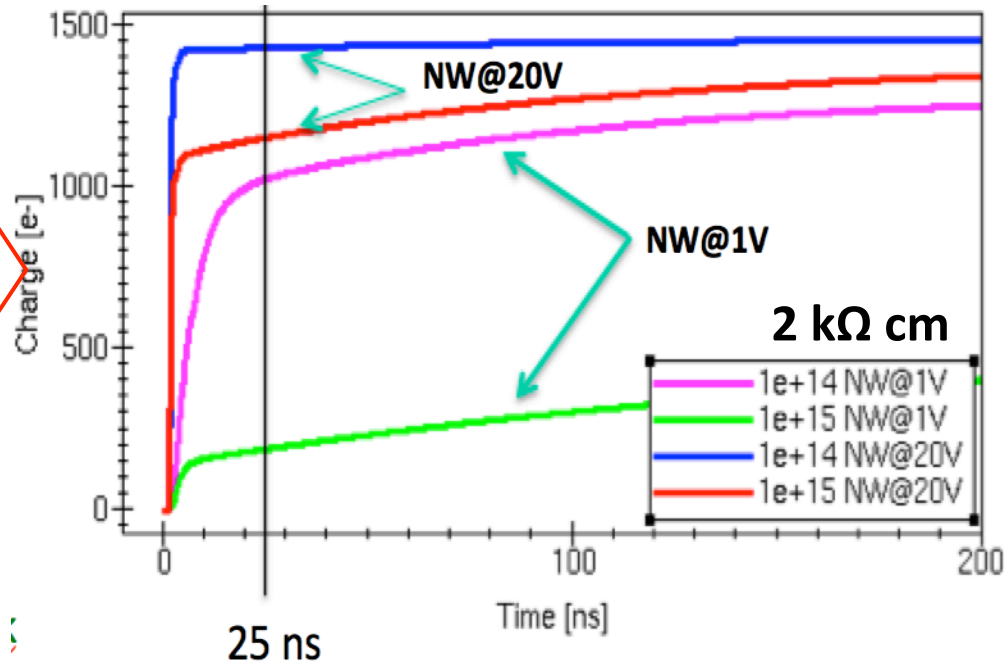


HR plus (high) voltage



Fill Factor influence: here at 10^{15} n_{eq}/cm^2

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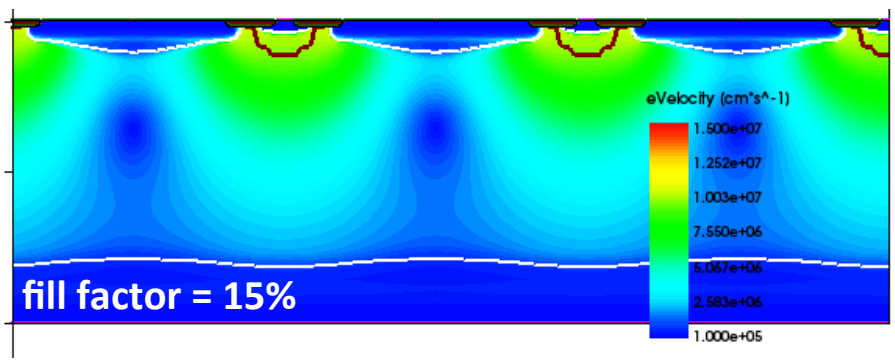
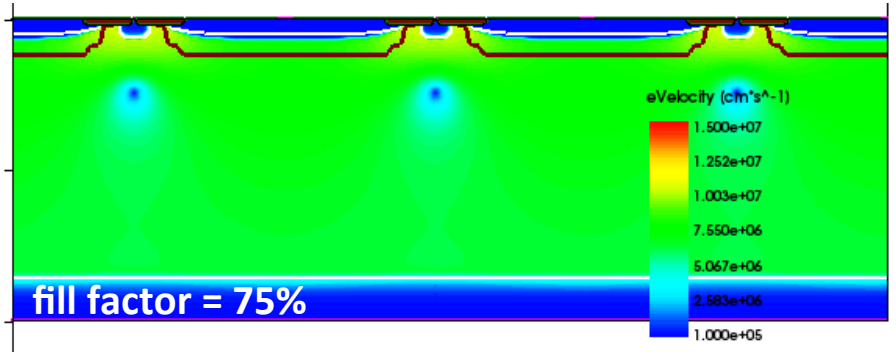
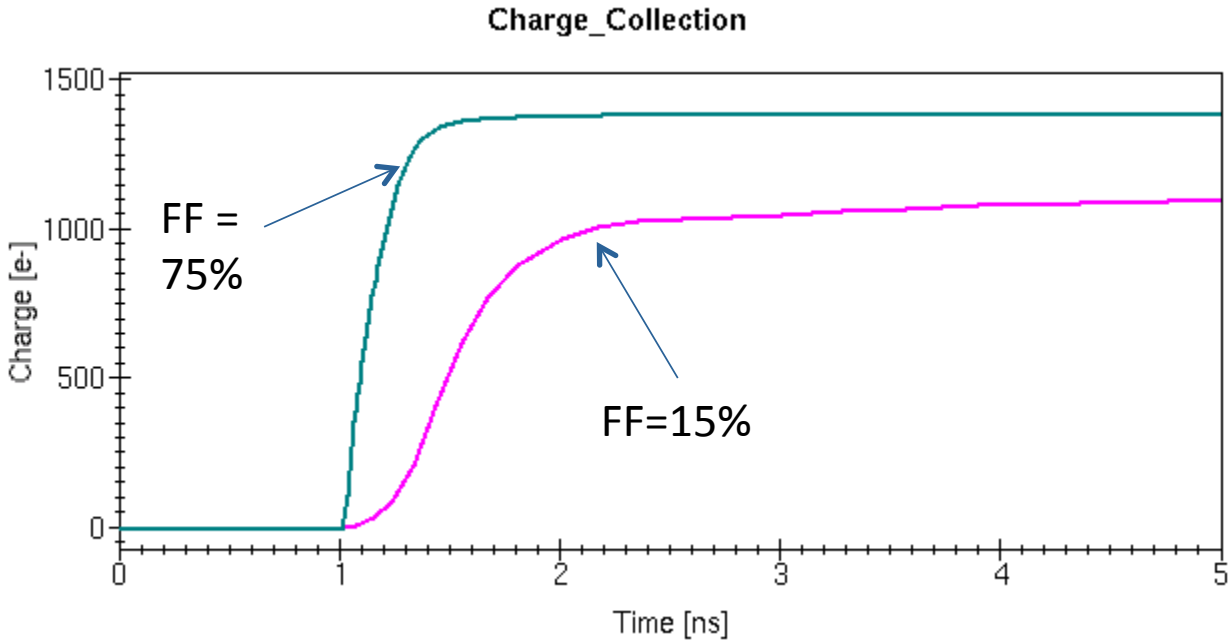
Electron Velocity







NW: 20V
PW: 0V
Substrate:2kΩ cm
Dose: 10^{15} n_{eq}/cm^2

Tomasz Hemperek

Summary: Resistivity, Voltage, Fill-Factor

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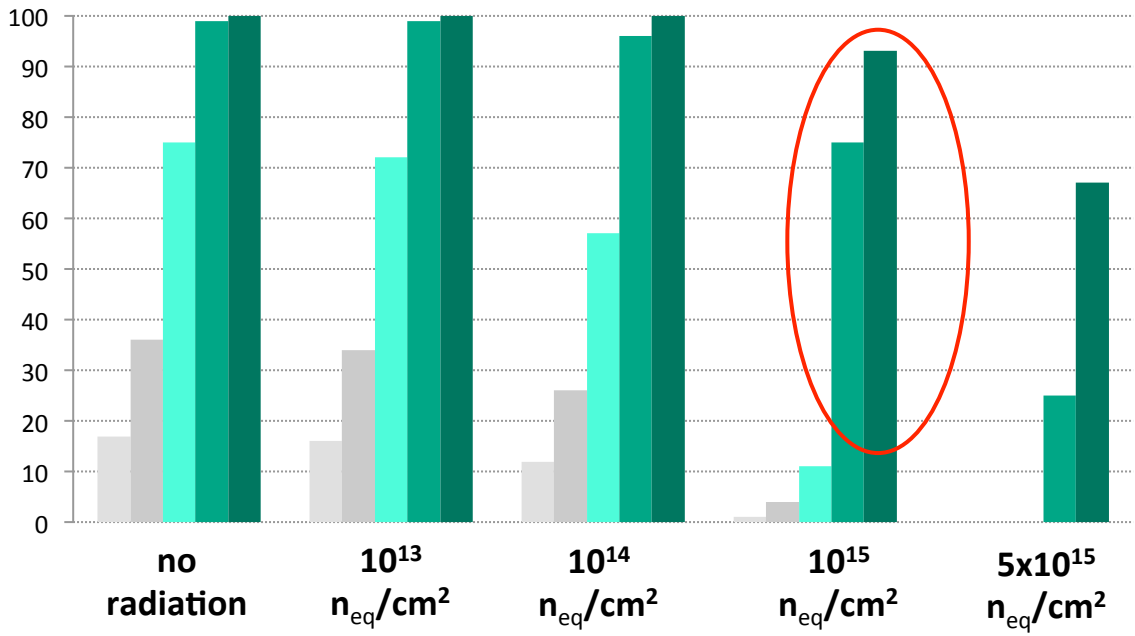
fraction of collected charge in first 10ns



	substrate resistivity [Ωcm]	Bias [V]	Fill Factor [%]
	10	1	15
	10	20	15
	2k	1	15
	2k	20	15
	2k	20	75

from Tomasz Hemperek

Enabling technologies

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"High" Voltage add-ons

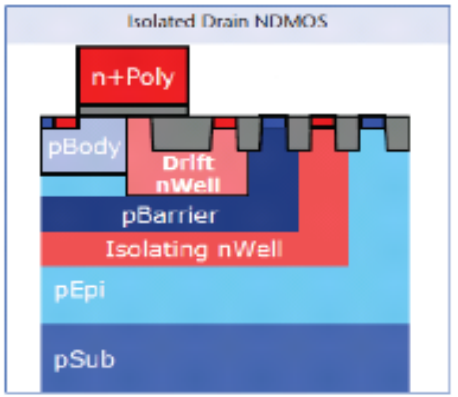
Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm).

"High" Resistive Wafers

8" hi/mid **resistivity** silicon wafers **accepted/qualified by the foundry**. Create depletion layer due the high resistivity.

Technology features (130-180 nm)

Radiation hard processes with **multiple nested wells**. Foundry must accept some process/DRC changes in order to optimize the design for HEP.



from: www.xfab.com

Backside Processing

Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing.

Interest in CMOS Pixels for LHC-pp => (D)MAPS

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- driven by the need/hope for
  - low cost large area detectors … more pixel layers in trackers …. commercial
  - less material … ? … possibly
  - smaller pixels … may be … may be not
  - less power … ? … not clear

- facing the challenges of HL-LHC

	inner layers (<6 cm)	outer layers (>25 cm)
• high rates	10 MHz/mm^2	1 MHz/mm^2
• radiation	> 1 Grad TID	50 Mrad
	2 x 10^{16} n_{eq}/cm^2	10^{15} n_{eq}/cm^2

note: at > 10^{15} n_{eq}/cm^2 trapping becomes the dominant radiation effect

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- **goal:** some (40 – 80 µm) depletion depth for …
  - a reasonably large signal ~4000 e-
  - fast charge collection (< 25ns "in-time" efficient)
  - not too large a travel distance to avoid trapping (rad hardness)

Current approaches (a classification)

HV - CMOS

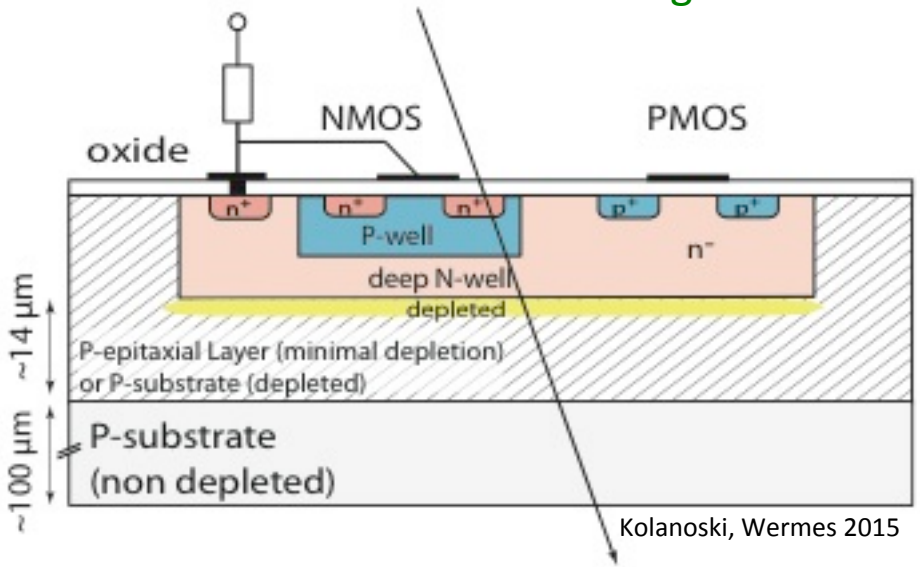
$$d \sim \sqrt{\rho \cdot V}$$

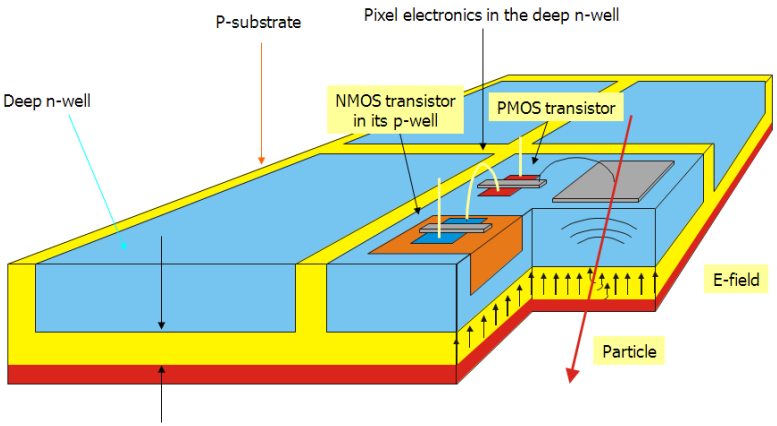
I. Peric et al.

Nucl.Instrum.Meth. A582 (2007) 876-885

Nucl.Instrum.Meth. A765 (2014) 172-176

e.g. AMS technology





- AMS 350 nm and 180 nm HV process (p-bulk) ... 60-100 V
- deep n-well to put nMOS (in extra p-well) and pMOS (limitation)
- ~10 - 15 µm depletion depth → 1-2 ke signal
- various pixel sizes (~20 x 20 to 50 x 125 µm^2)
- can also replace „sensor“ (amplified signal) in a „hybrid pixel“ bonding (bump, **glue**, other...) to FE-chip => **CCPD**

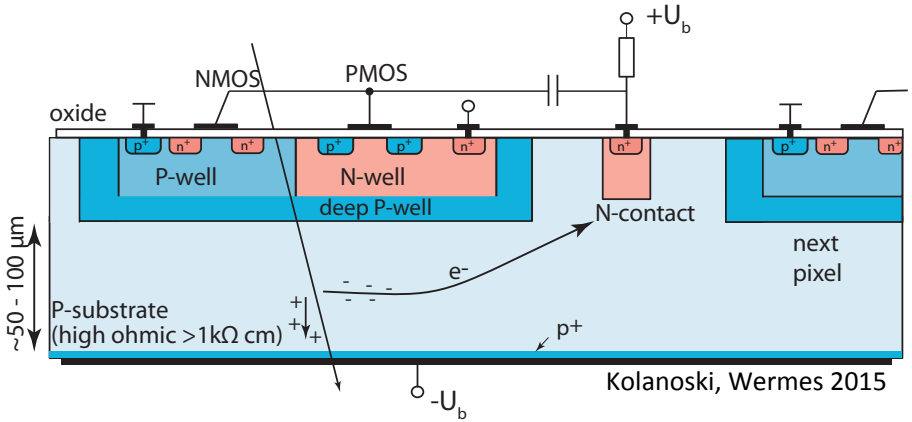
(see also Posters by Ivan Peric and by Heinz Pernegger)

Current approaches (a classification)

HR - CMOS

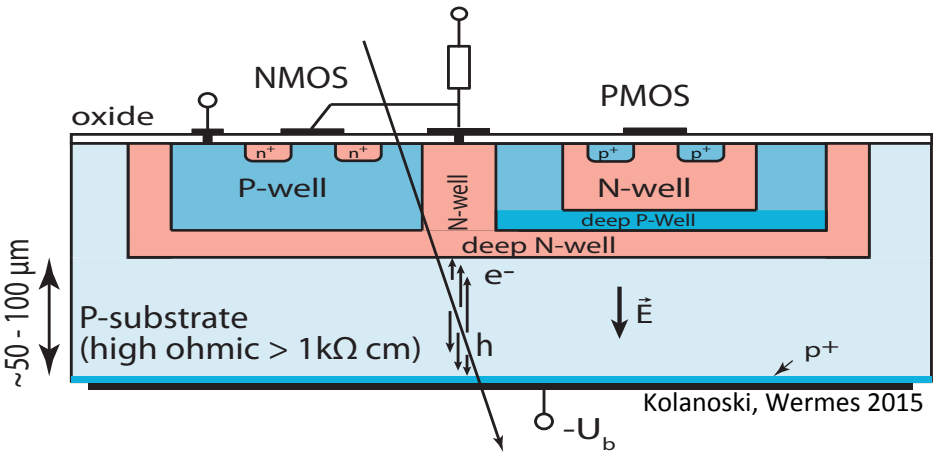
$$d \sim \sqrt{\rho \cdot V}$$

Havranek, Hemperek, Krüger et al.
JINST 10 (2015) 02, P02013



- (D)MAPS like configuration but w/ depleted bulk
- small collection node
- long drift path

=> **smaller C, more trapping**



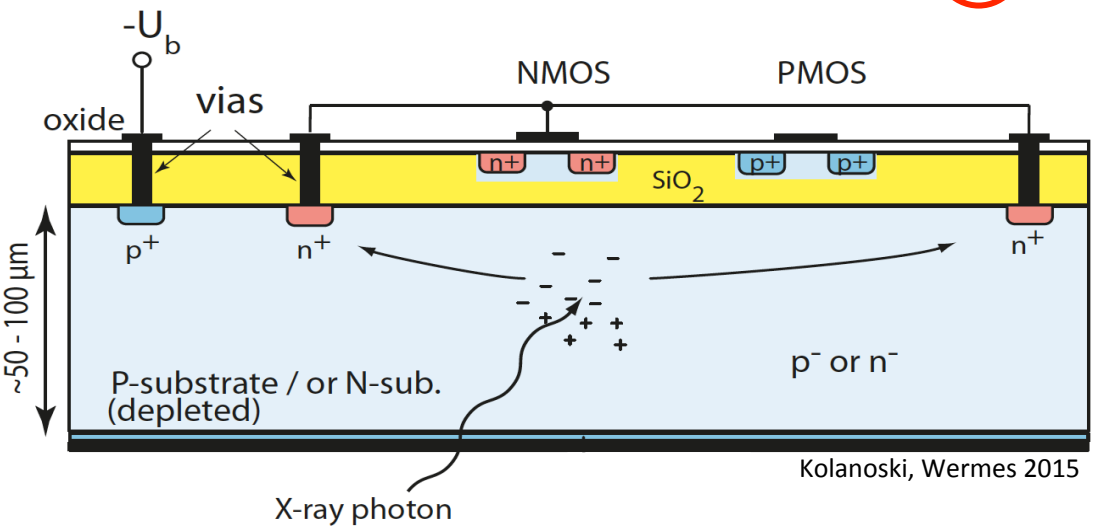
- deep n and deep p wells
- large collection node
- short drift path

=> **larger C, less trapping**

Current approaches (a classification)

CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$



Kolanoski, Wermes 2015

- **FD-SOI**
- OKI/LAPIS/KEK
  Y. Arai et al. (talk by T. Miyoshi)
- issues
  - back gate effect
  - radiation issues due to BOX
- cures invented in recent years
- but not suited for LHC - pp

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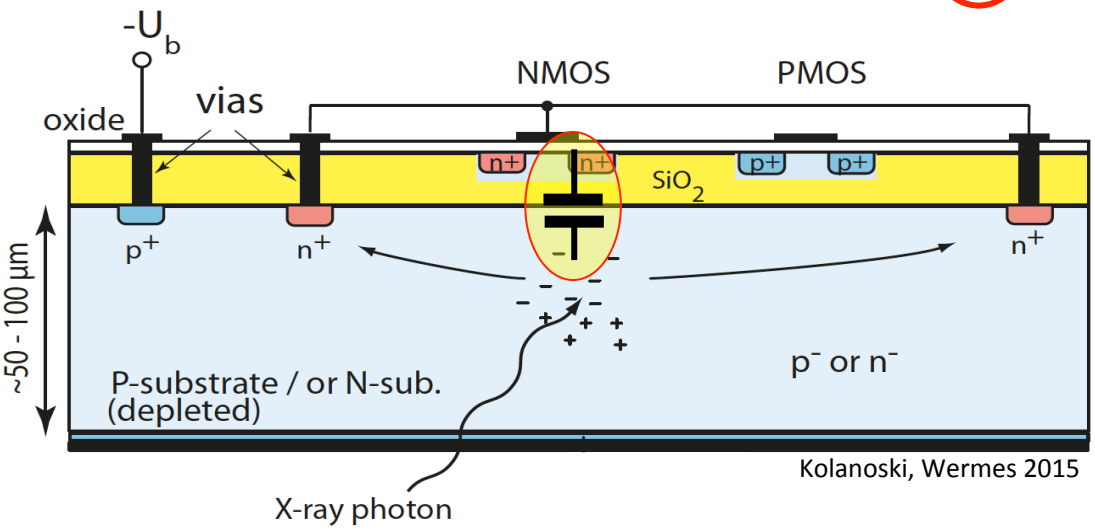

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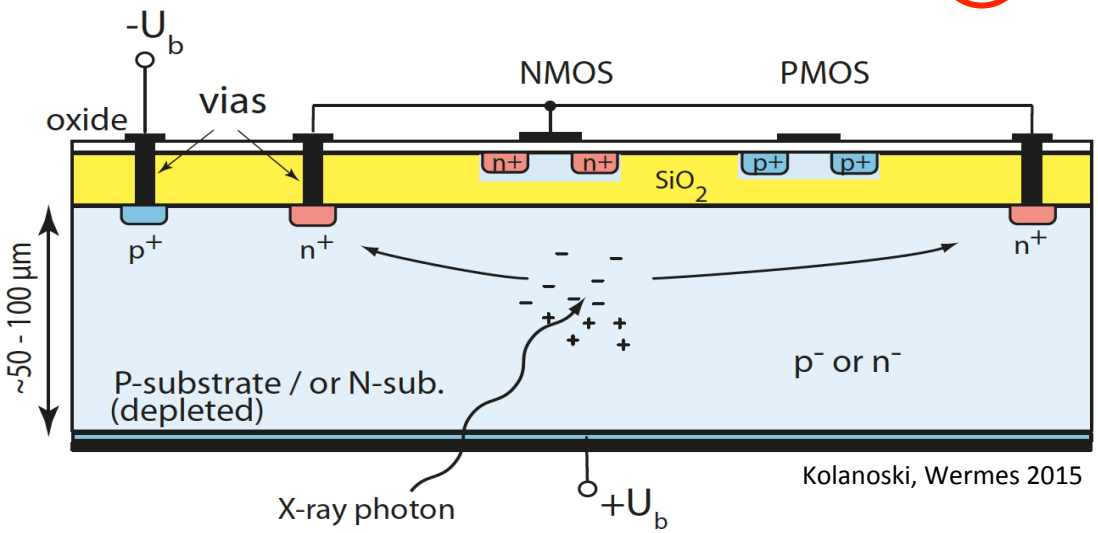

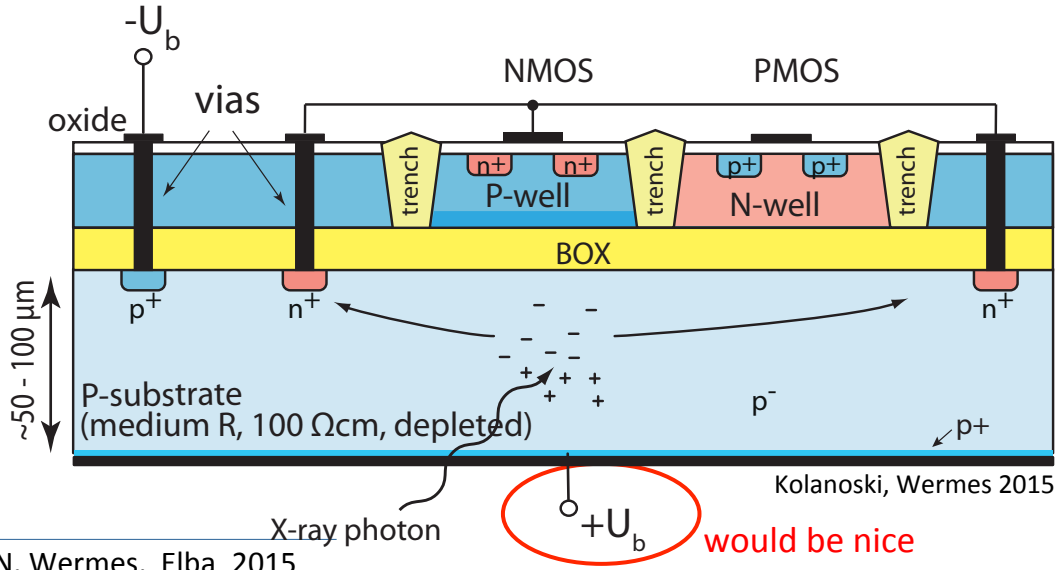

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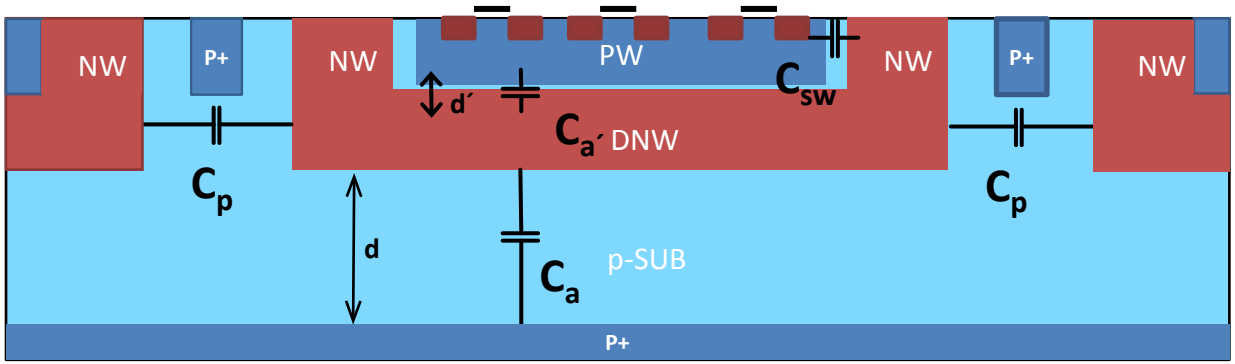
- **HV-SOI (thick film)**
- Hemperek, Kishishita, Krüger, NW
  doi:10.1016/j.nima.2015.02.052
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

The input capacitance to the CSA is crucial ...

- **noise** (ENC ~ C_{in}) increases with the input capacitance
- **speed** also depends on C_{in} => the smaller the better
- for active CMOS pixels there are additional capacitance contributions (H. Krüger)
  - C between deep N-well and P-well is dominant
  - C_{in} does not scale (down) with area



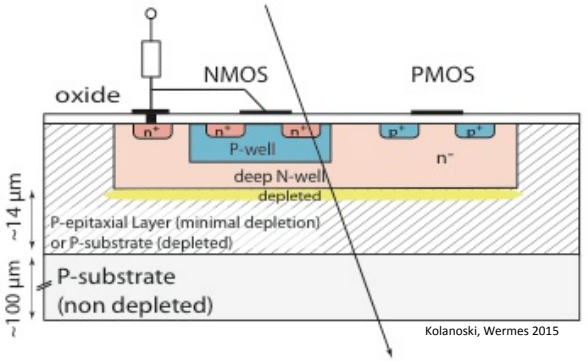
- hybrid planar pixels (e.g. ATLAS IBL, 50×250×200 µm^3): **C_{in} = 109 fF** (Havranek et al, NIMA 714 (2013) 83-89
- CMOS pixel extrapolation: **C_{in} ≈ 200 fF**

Prototype results

bonded to FE-I4 pixel chip (CCPD)
and stand alone (for DMAPS performance characterization)

- **HV CMOS** (see also Posters by Ivan Peric and by Heinz Pernegger)
- **HR CMOS** (see also Poster by Tetsuishi Kishishita)
- **SOI CMOS** (see also Poster by Heinz Pernegger)

HV-CMOS (AMS H18 180 nm)



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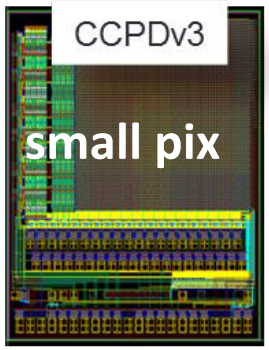
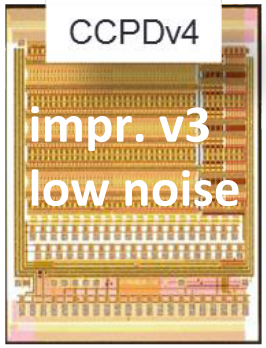
Karlsruhe (design&test)
Geneva, CCPM, CERN,
Bonn (char&tests)

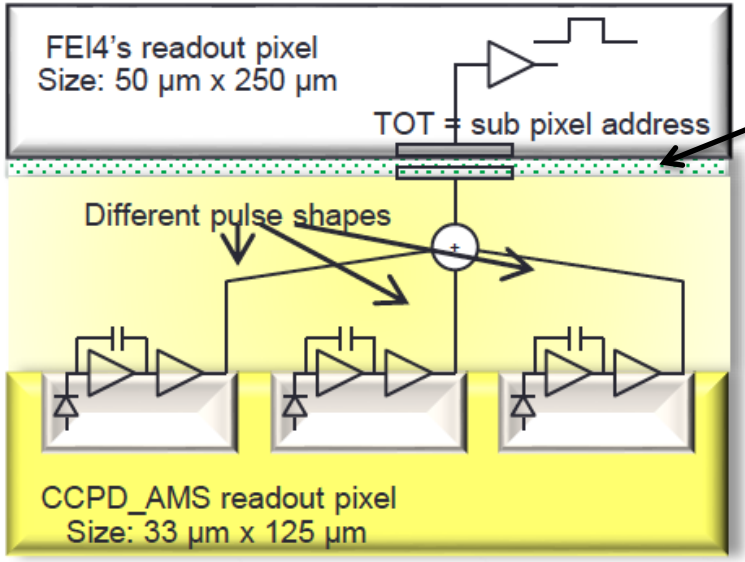
4 versions since 2011





specs

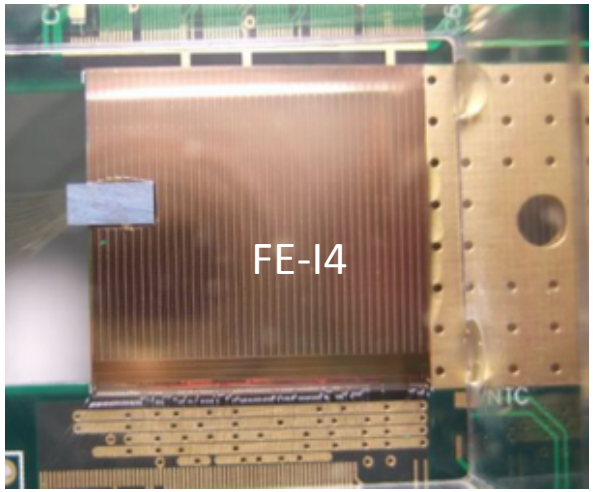
- ρ = 10 Ωcm
- bias 60 – 100 V
- depletion depth ~10 µm or more
- Q (theoretical) ~1000 e- by drift
- R/O via ATLAS pixel chip FE-I4 capacitively coupled
- design ported also to **GF & LF** (CPPM/KIT)



glue

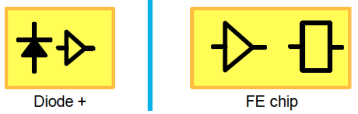
sub-pixel decoding
through pulse shape
(TOT => sub-address)

50 × 250 µm² => 33 × 125 µm²
effectively



I. Peric et al., NIM A765 (2014) 172-176 (see also poster by Ivan Peric)

AMS 180 nm (bonded to FE-I4)



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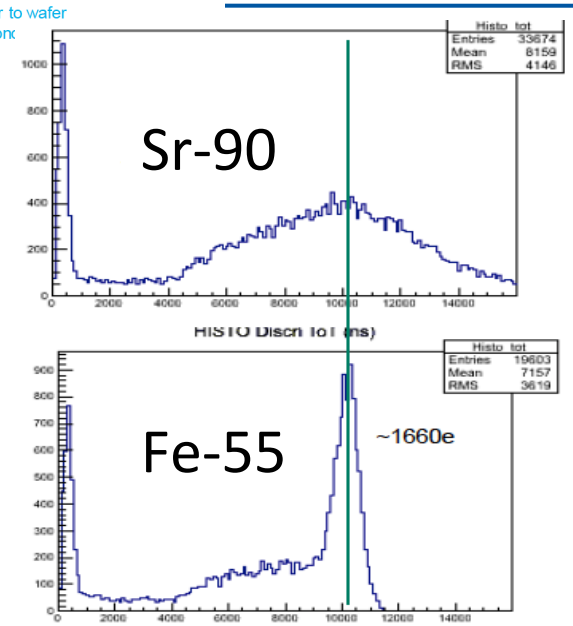
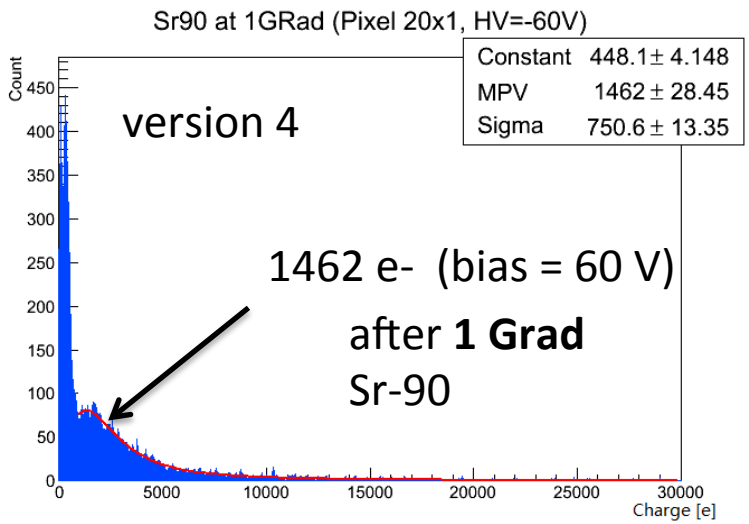
some encouraging results

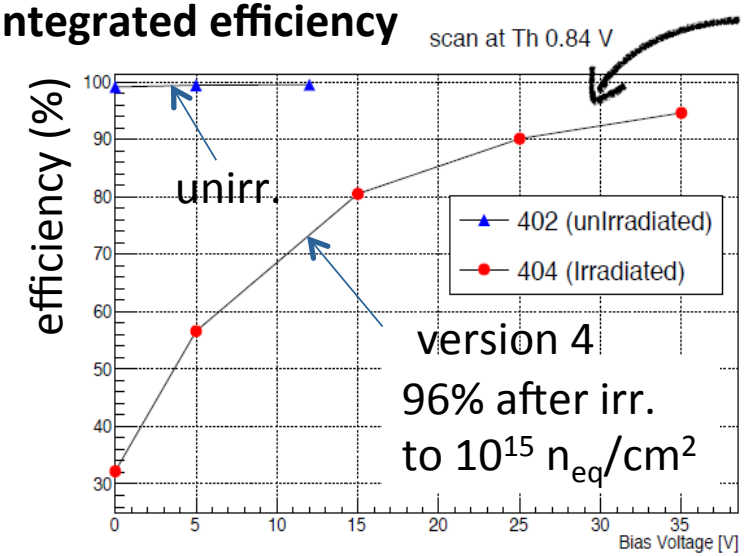
- **capacitive coupling** seems to work in principle, whether it is competitive in terms of reliability and price is unclear
- chips stand **TIDs** up to **1 Grad**
- proton irradiation 10^{15} n_{eq}/cm^2 performed
- efficiency (time integrated): 99% -> **96%**
- **in-time efficiency** not yet met (τ_{rise}~100 ns)
- signal ~1500 e ; SNR ~ 25



version 2
before
irradiation



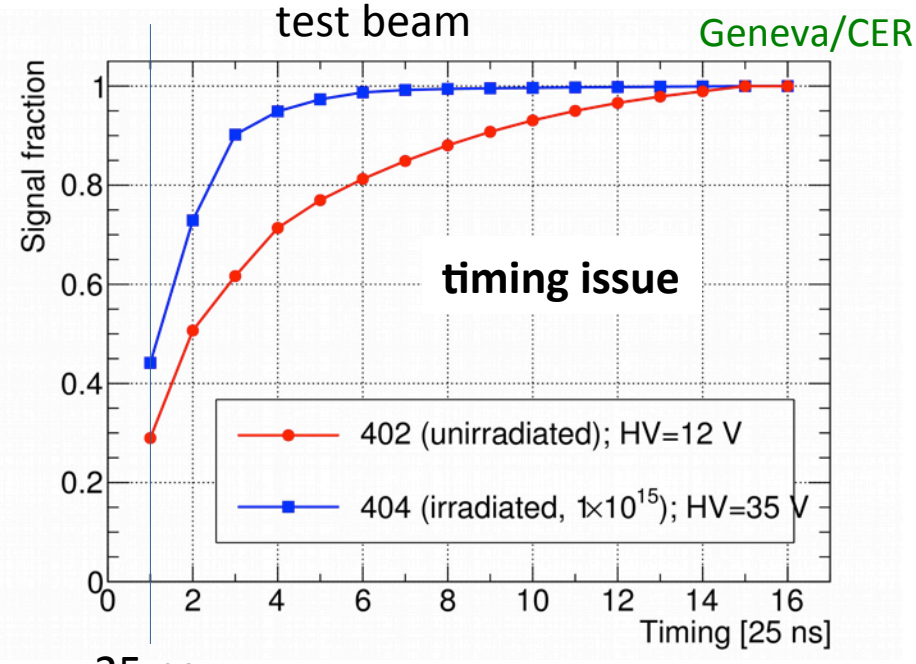
time integrated efficiency



AMS 180 nm version4 (bonded to FE-I4)

The only CMOS sensor which has seen >> 10^{15} neutrons / cm^2 (up to 2 x 10^{16} n/cm^2, i.e. HL-LHC)

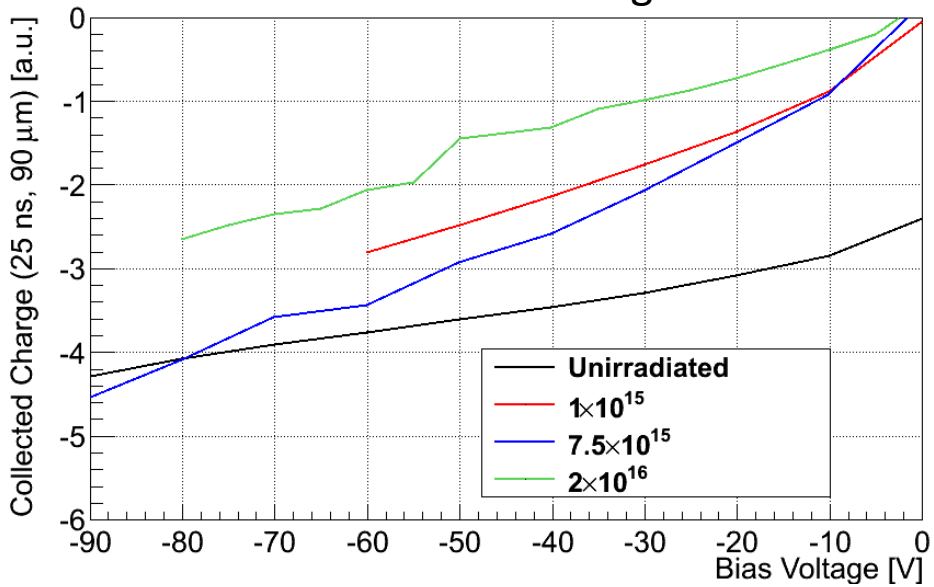
test beam



25 ns

Geneva/CERN characterizations

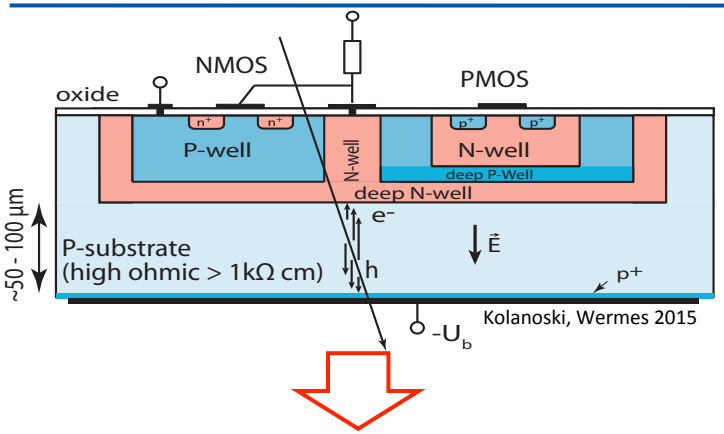
edge TCT

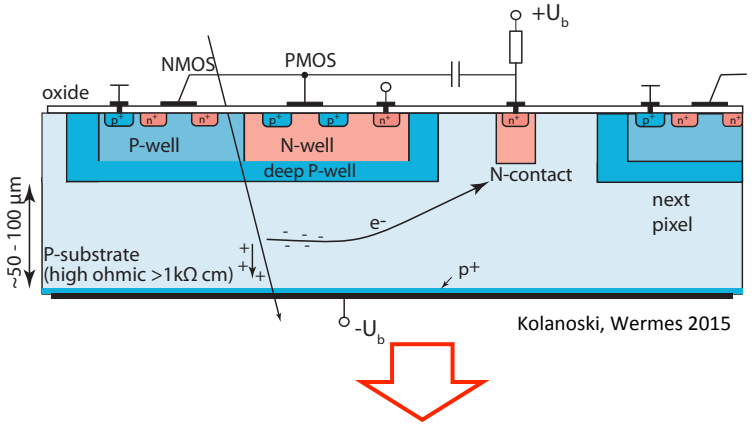


see also
poster by Heinz Pernegger

Intime signal fraction increases with irradiation, probably due to acceptor removal and larger fraction of charge collected by drift **also depletion depth** increases to ~20 µm @ -80V

HR-CMOS: LFoundry and ESPROS prototypes

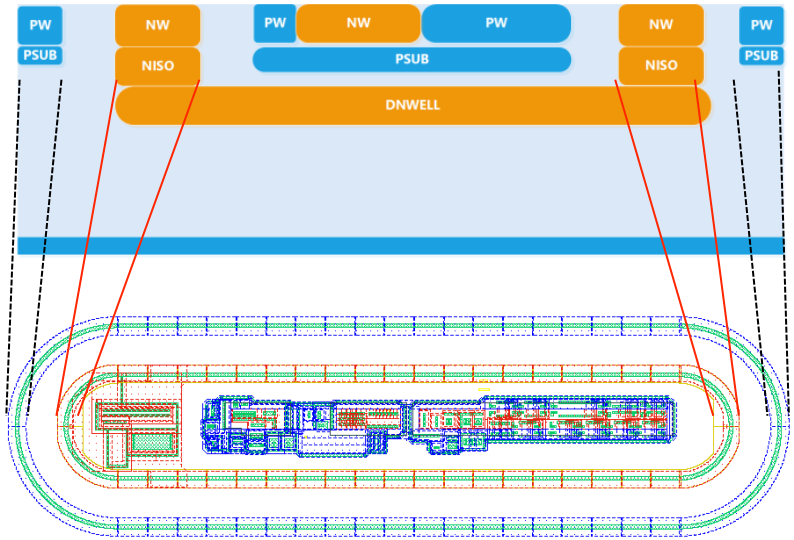




LF: Electronics inside collection well

- ❑ Large fill factor for high CCE and rad-hardness
- ❑ Full CMOS, isolation via deep p-well (PSUB)
- ❑ HR substrate **(2 kΩ cm)**, p bulk
- ❑ 150 nm process

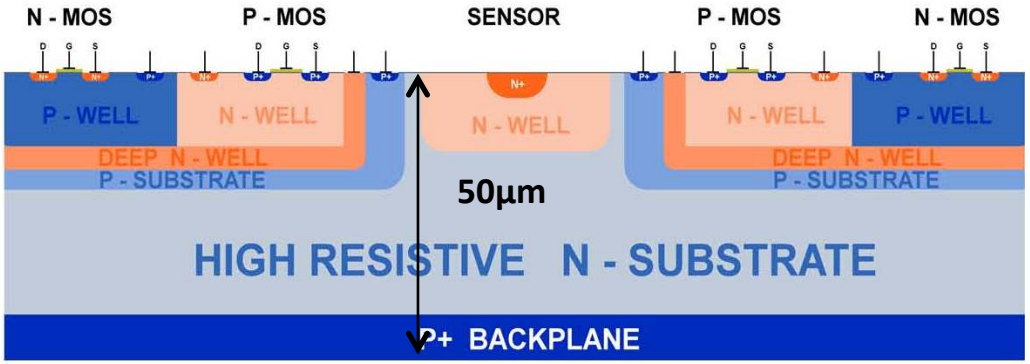
Bonn, CPPM, Karlsruhe



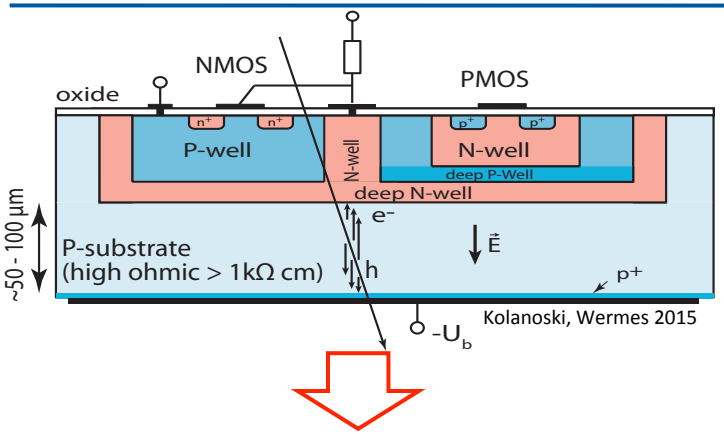
ESPROS: Electronics outside collection well

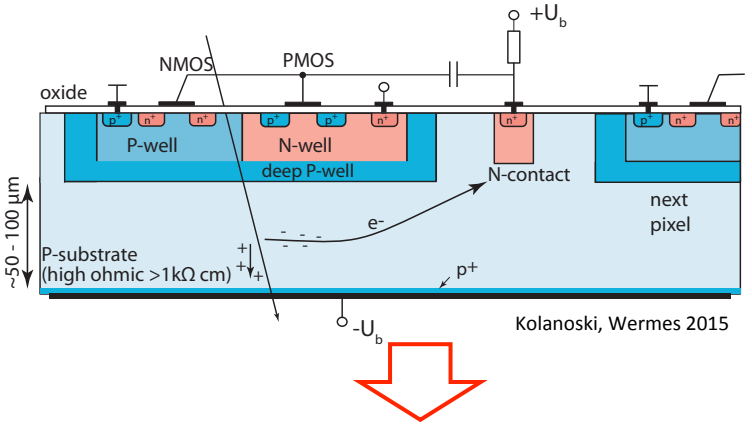
- Small fill factor, no competing wells
- Full CMOS, isolation via deep n- and p-well
- HR substrate **>2kΩ cm**, n bulk
- **Backside** thinning **and implant**: default option
- 150 nm

Bonn, Prague



HR-CMOS: LFoundry and ESPROS prototypes





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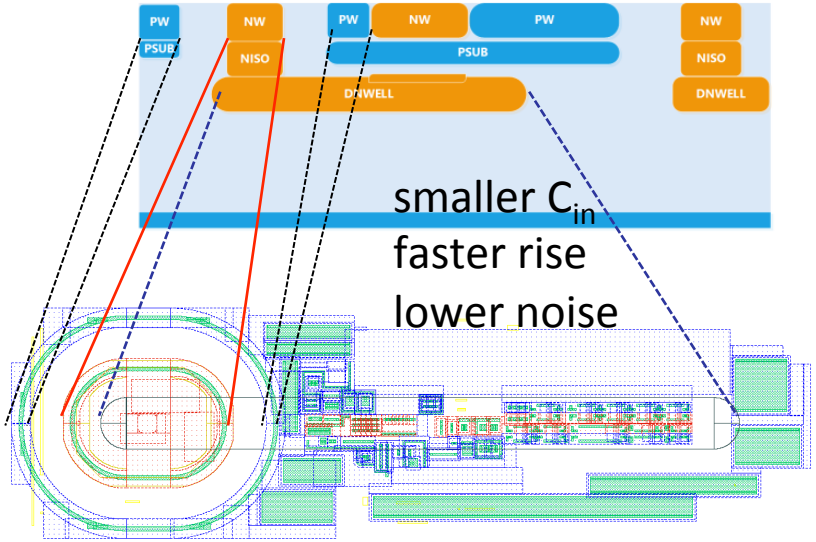
Bonn, CPPM, Karlsruhe



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- HR substrate **>2kΩ cm**, n bulk
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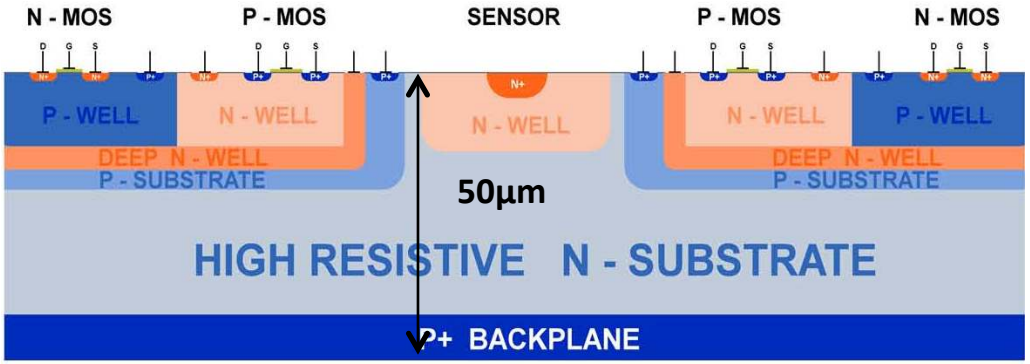
Bonn, Prague



HR-CMOS: LFoundry … preamp characterizations

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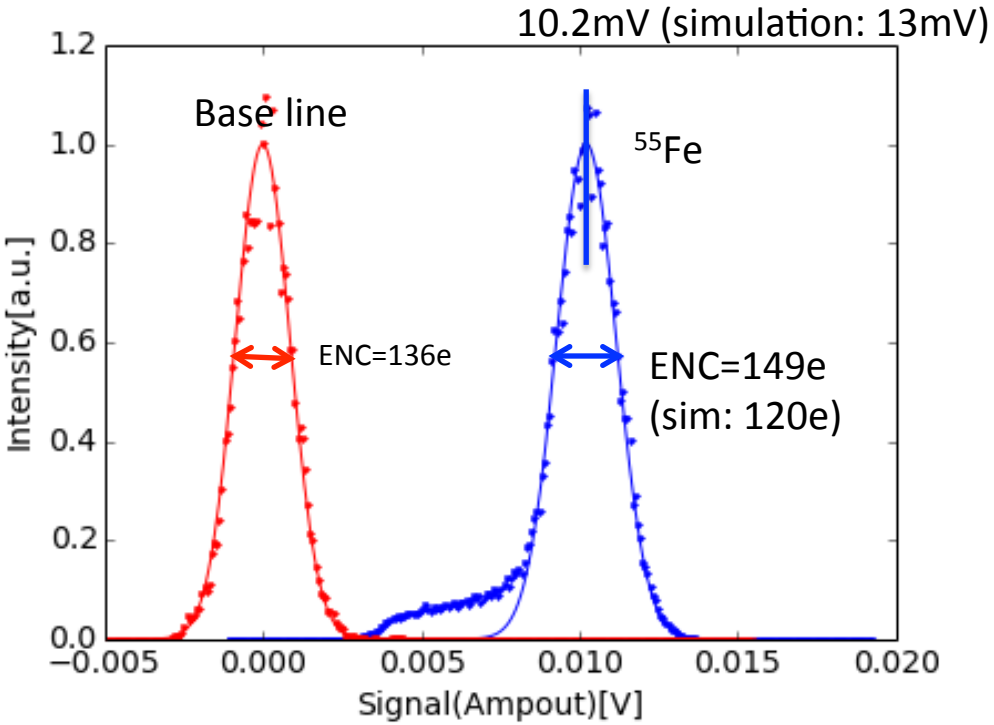
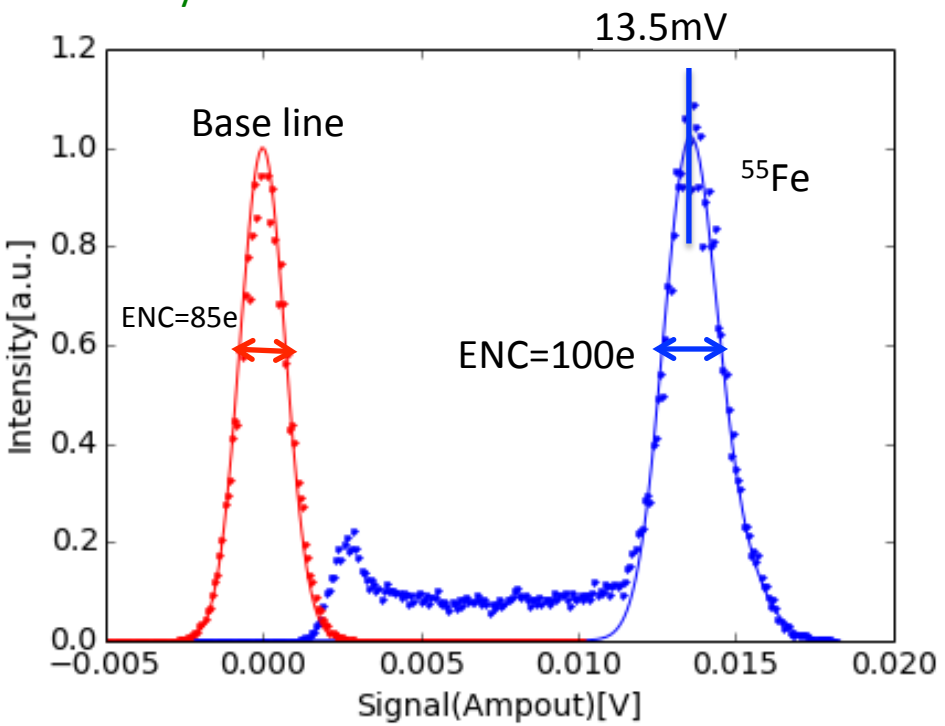
- Version A
  - Bias: 110V (4nA)
  - Pixel: CSA ELT
  - Source: ^{55}Fe

- Version B
  - Bias: 20V (39nA)
  - Pixel: HV connection Diode, CSA ELT, PSUB everywhere
  - Source: ^{55}Fe



measm'ts by Toko Hirono



Noise and gain agree reasonably with simulations!

x-talk less for version B than A, but < 3% ! (CPPM)

HR-CMOS: Lfoundry … charge spectra **3.2 GeV electrons**

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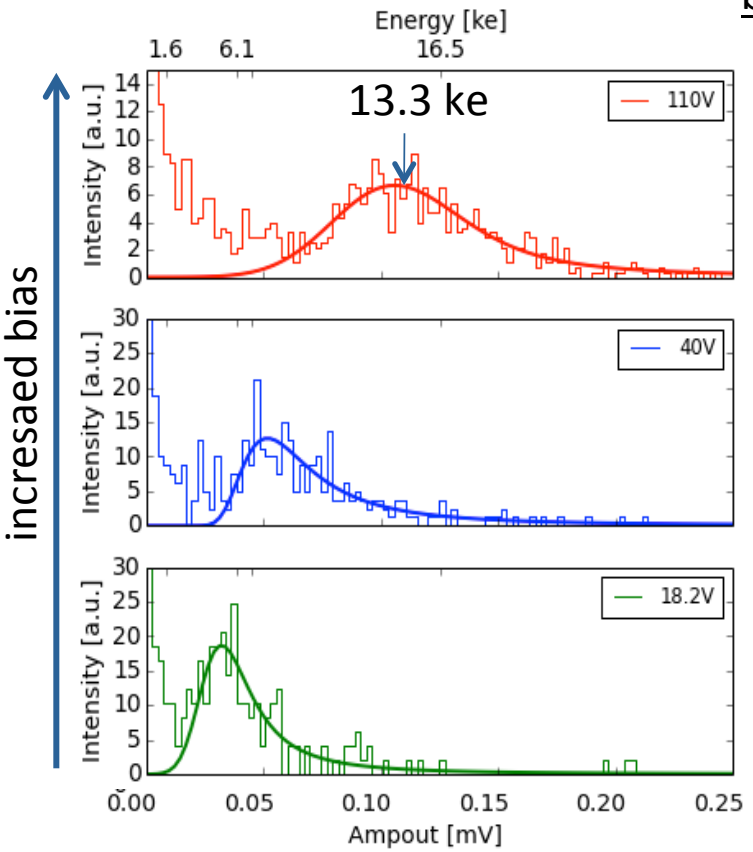
- Version A
  - Bias: 110V (4nA)
  - Pixel: CSA ELT
  - Source: ^{55}Fe

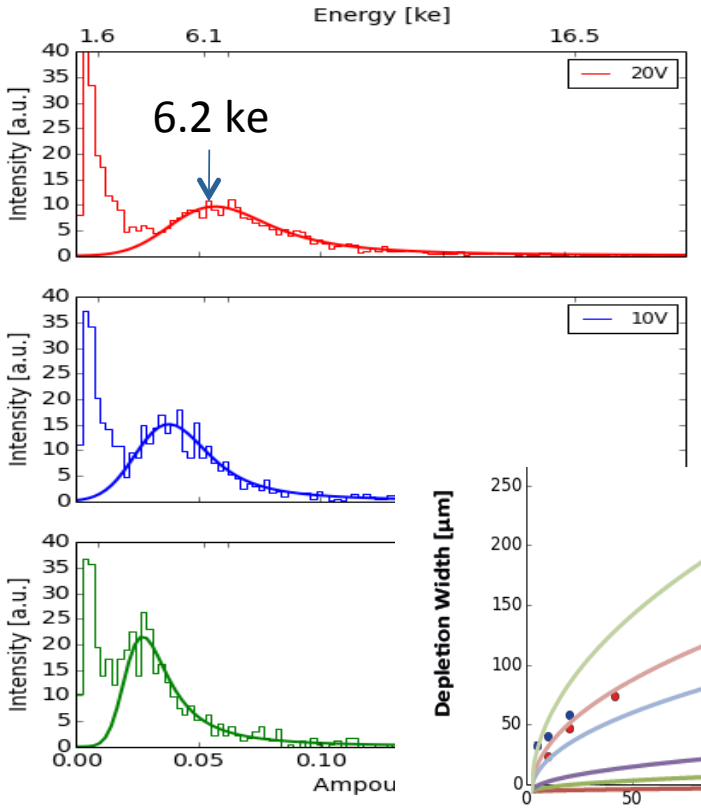
- Version B
  - Bias: 20V (39nA)
  - Pixel: HV connection Diode, CSA ELT, PSUB everywhere
  - Source: ^{55}Fe

6.9

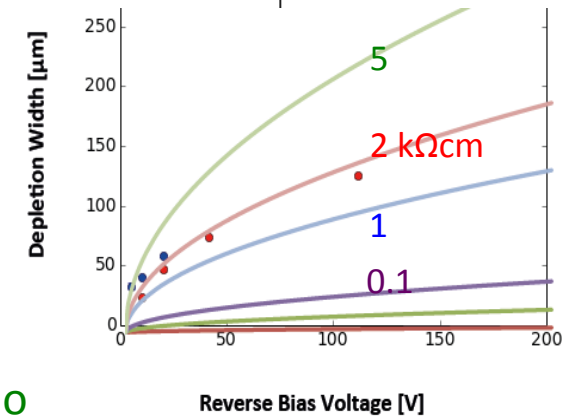
before thinning: ~700 µm



i.e. ~120 µm depl. depth



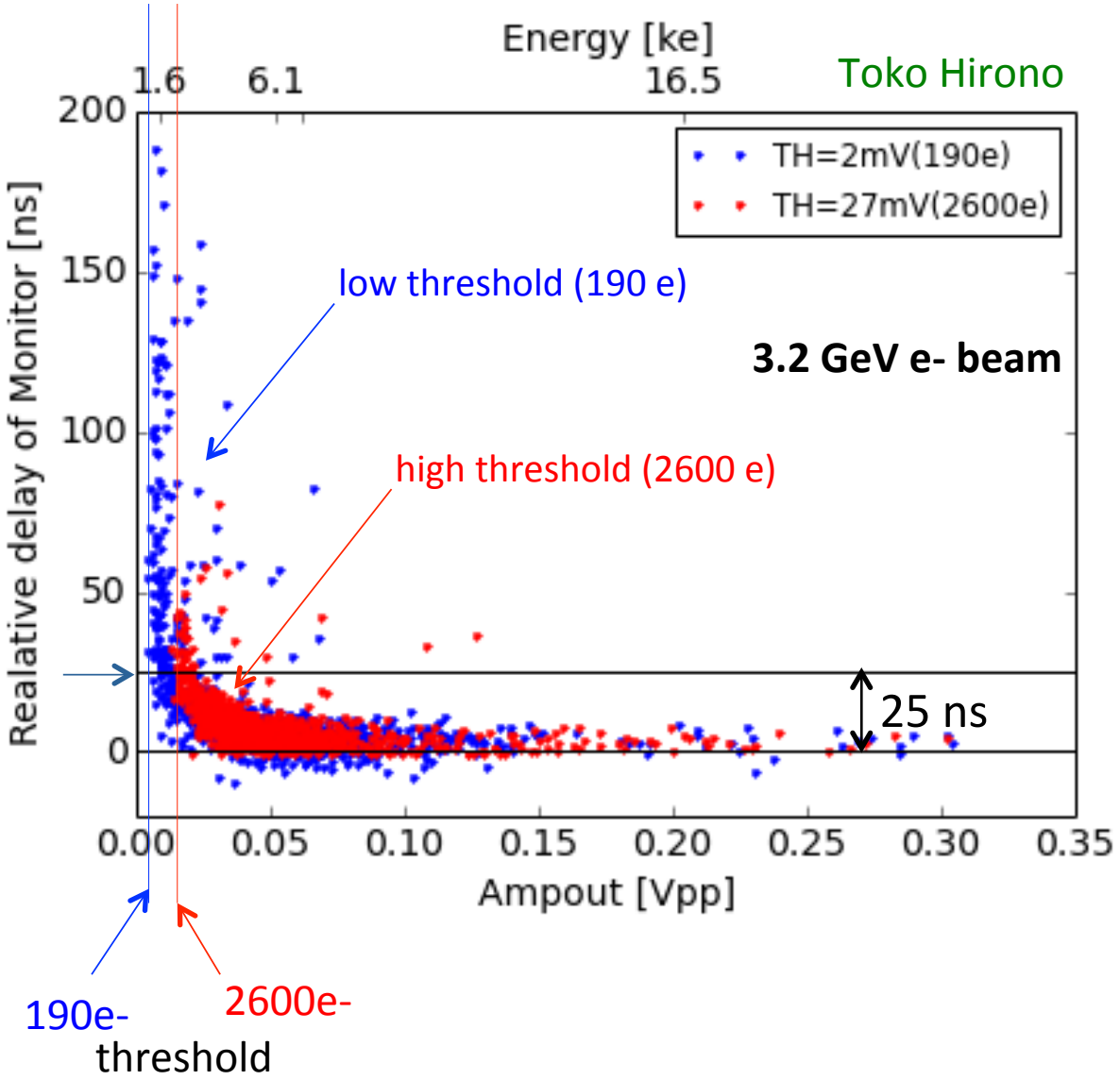
i.e. ~60 µm depl. depth



T. Hirono

test beam @ ELSA/Bonn

HR-CMOS: LFoundry … time walk



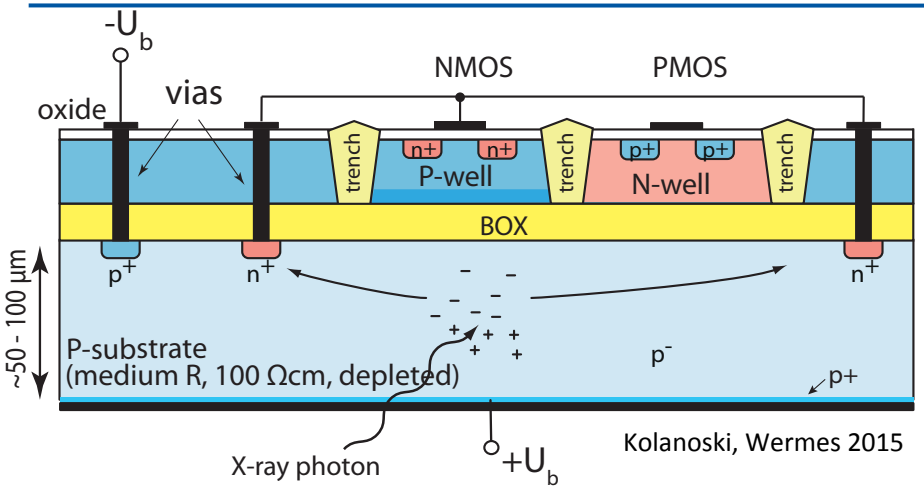
fraction of
"in-time (25 ns)" hits

- 190 e threshold: 79%
- 2600 e threshold: 91%

next: performance

- w/ thinned sensor (300 µm)
- backside implant
- irradiated

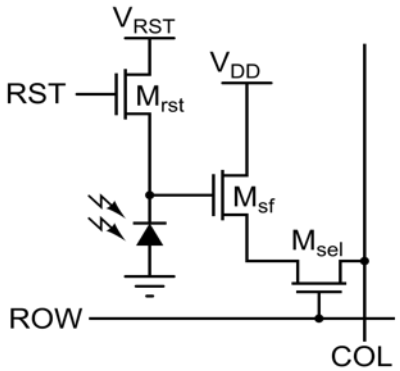
HV-SOI: test chips XTB01 and XTB02

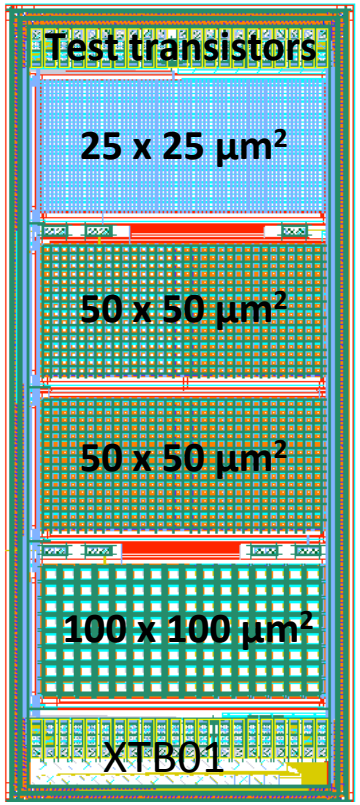


XFAB 180 nm: Electronics outside collection well

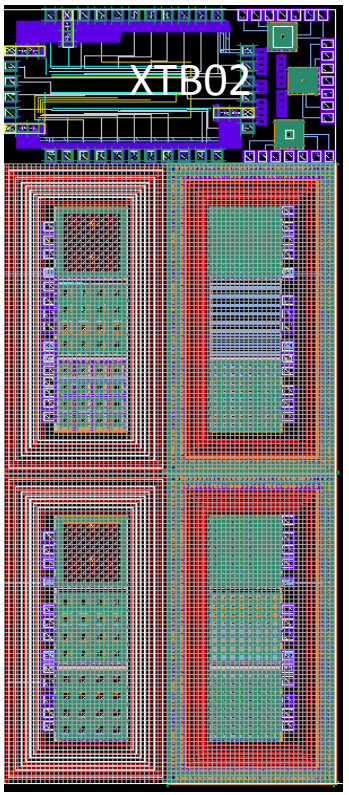
- Small charge collection well
- Full CMOS, no backgate effect
  due to isolation via deep p-well (non-depleted)
  between CMOS layer and BOX
- HV technology + MR substrate (100 Ωcm), p bulk

- 3 T readout





Design: Bonn
Testing: Bonn, CERN



dedicated structures to test the technology further (leakage, break down voltage, etc.)

see also poster by Heinz Pernegger

XFAB SOI XTB01 prototype chip: first irradiation tests

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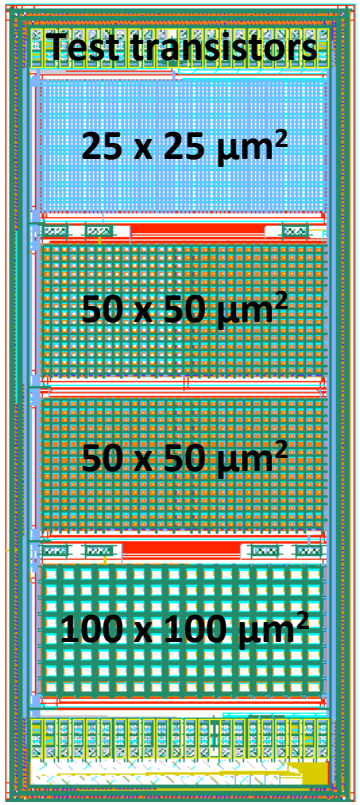
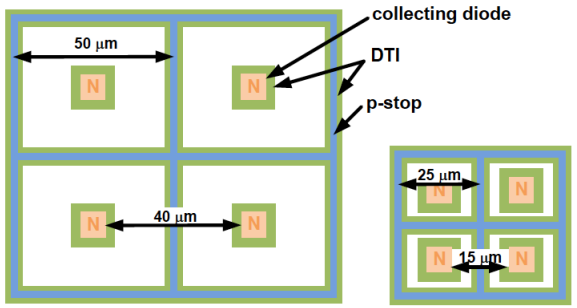
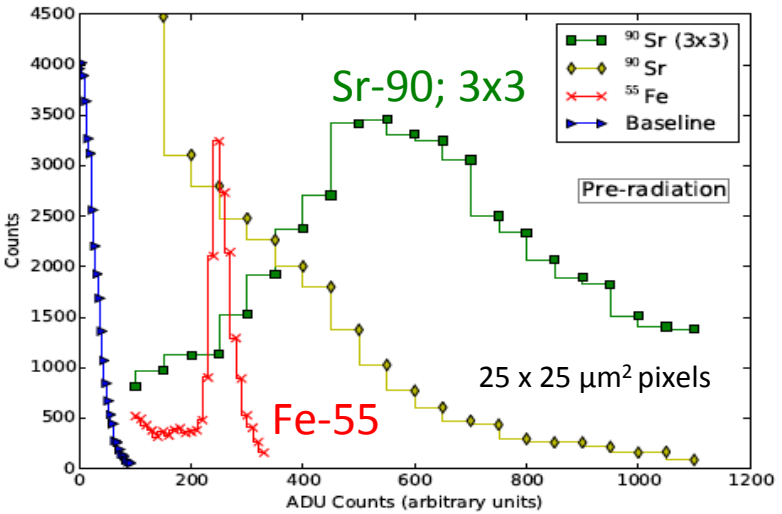




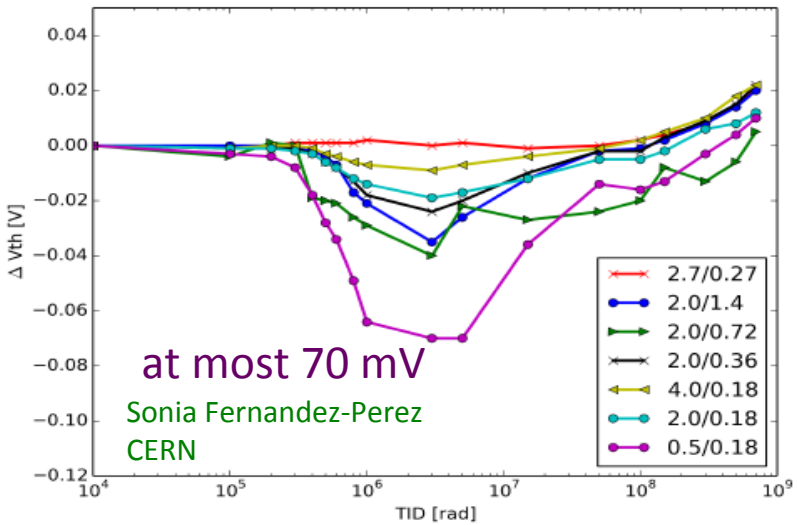
NIEL

TID

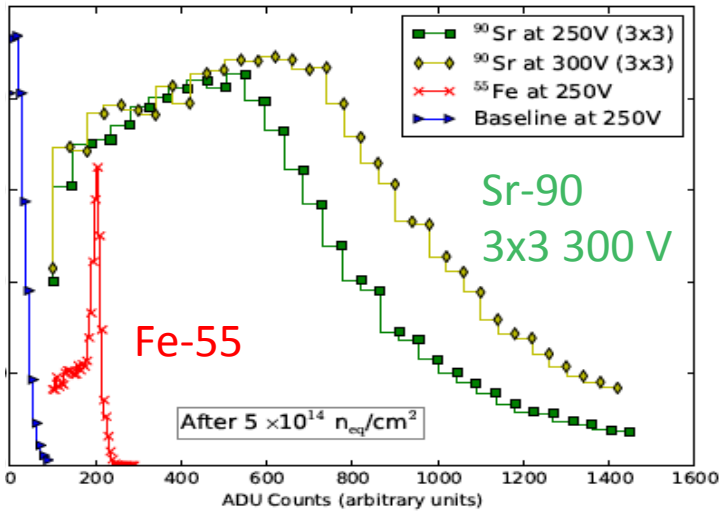
before irradiation



NMOS threshold shift after **700 Mrad**



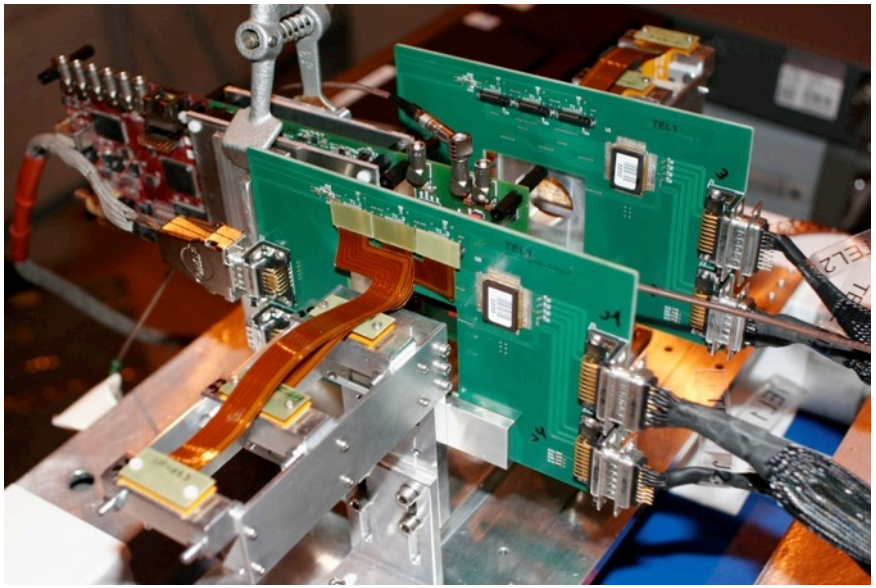
after irradiation: **5 x 10¹⁴** n_{eq}/cm^2

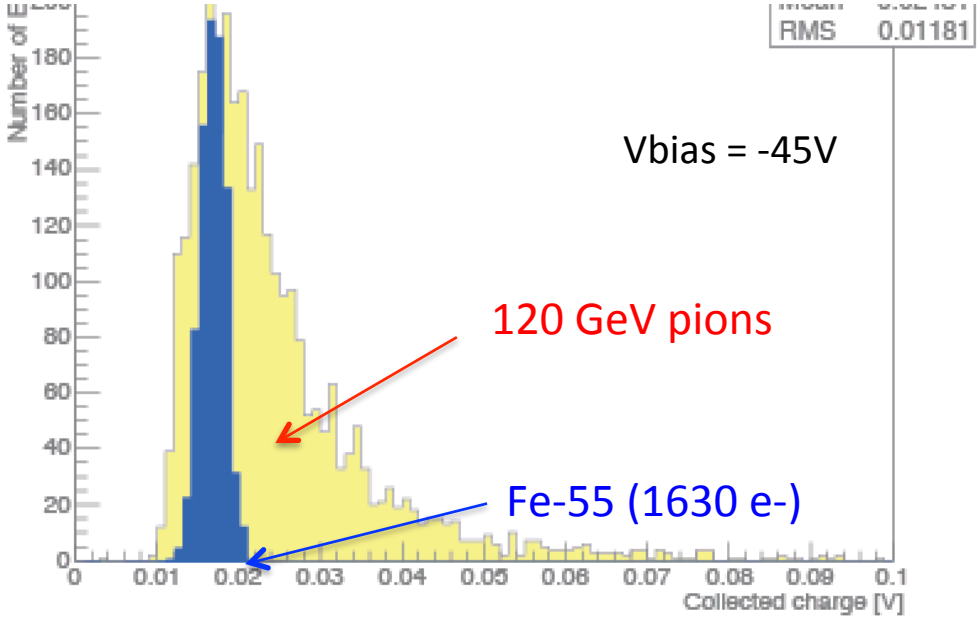


PMOS shift ~100 mV after 1 Grad

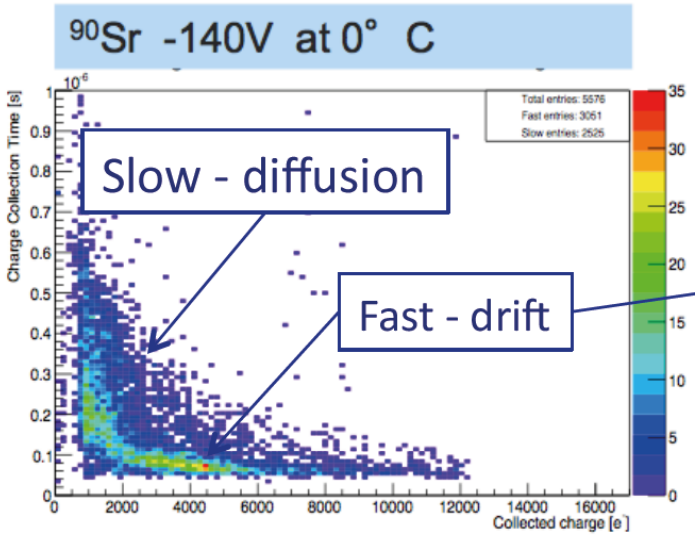
Hemperek, Kishishita, Krüger, NW
arxiv 1412.3973, accepted NIM A

XBT01 in test beam - 50x50µm² pixel





Depletion depth ≈ 31µm
Calculated depth = 36µm (@100 Ωcm, -45V)



observation:
charge collected from high-field (fast drift)
and low field (slow diffusion) regions

Conclusions

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- There is a large momentum in R&D for CMOS active pixels as an attractive direction for LHC experiments, even for LHC-pp.

- … outer layers … cost saving … less radiation
- … inner layers … small pixel sizes … position decoding

- R&D profits from micro electronics process and technology variations and its rapid progress.

BACKUP

Hybrid Pixels @ LHC: PROs and CONs

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- complex signal processing already in pixel cells possible
  - zero suppression
  - temporary storage of hits during L1 latency
- radiation hardness to >10^{15} n_{eq}/cm^2
- high rate capability (~MHz/mm^2)
- spatial resolution ~ 10 – 15 µm

PRO

… but also

- relatively large material budget: **~3% X_0** per layer (1% X_0 @ ALICE)
  - sensor + chip + flex kapton + passive components
  - support, cooling (-10°C operation), services
- complex and laborious module production
  - bump-bonding / flip-chip
  - many production steps
  - expensive

CON

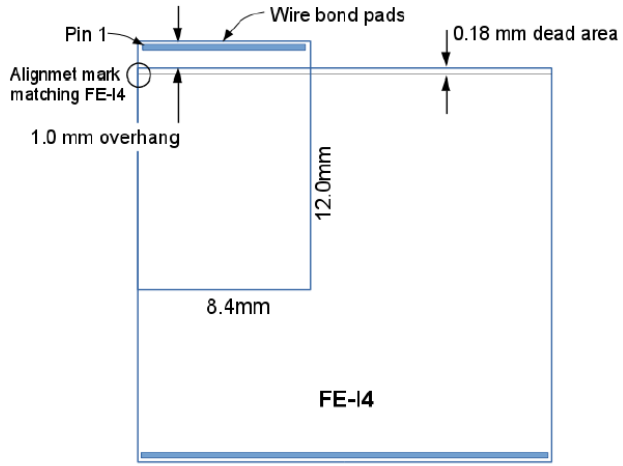

Fig. 1: Alignment of demonstrator to FE-I4 chip

- **goal:** develop a **cm² sized CMOS pixel module**
  - at first: bondable to a FE-I4 R/O chip (option

- **specs**
  - radiation tolerant to **50 Mrad (TID), 10^{15} /cm² (NIEL)**
  - **> 95% in-time** (<25 ns) efficiency after irradiation
  - < 20 µA power per pixel
  - **bondable** via bumps or glue to FE-I4

  - an area read out **through the pixel chip** (bonded to FE-I4)
  - an area read out **standalone** -> to characterize CMOS part
  - a **passive** area -> to compare to standard hybrid pixels

Technical support

Rate and radiation challenges at the innermost pixel layers

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Hybrid Pixels

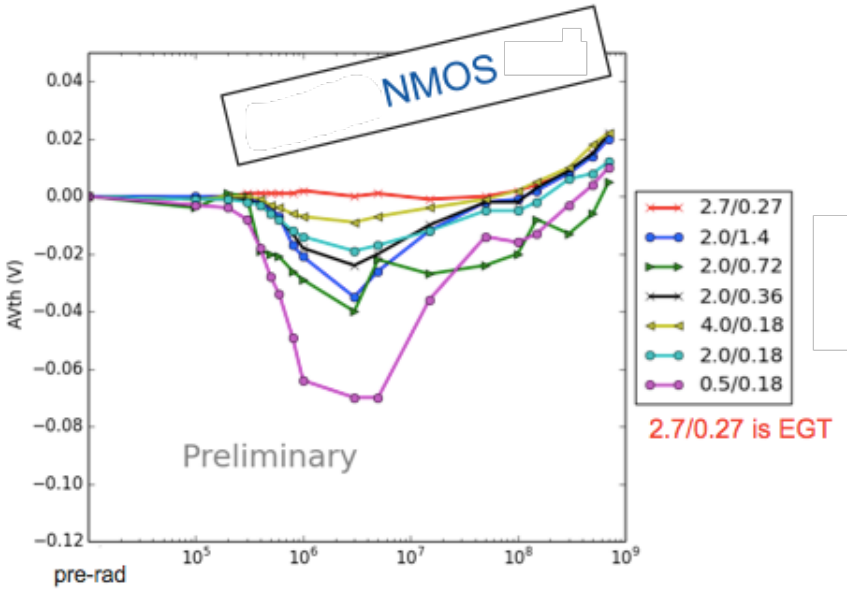
	BX time	Particle Rate	NIEL Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	Mrad per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	2×10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	25	10000	2×10^{16}	> 500
LHC Heavy Ions (6×10^{27} cm^{-2} s^{-1})	20.000	10	$>10^{13}$	0.7
RHIC (8×10^{27} cm^{-2}s^{-1})	110	3.8	few 10^{12}	0.2
SuperKEKB (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	0.4

Monolithic Pixels

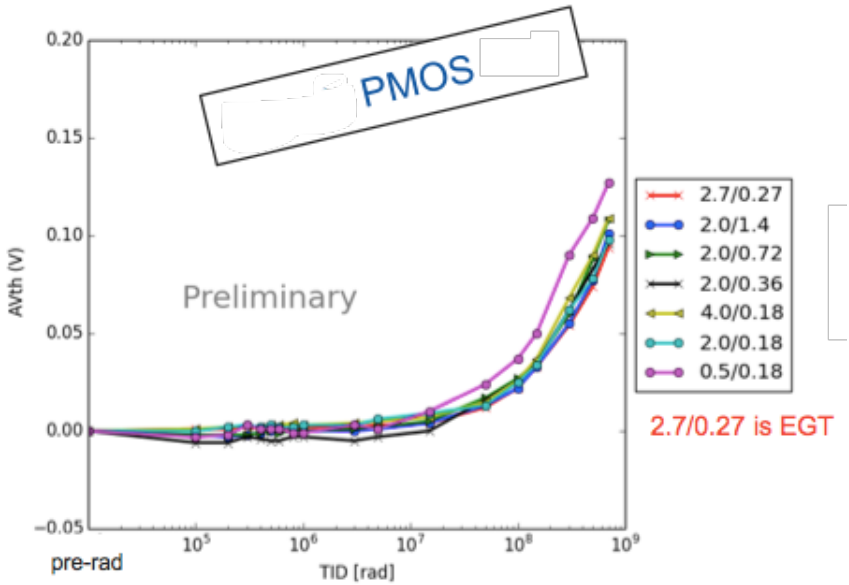
lower rates
lower radiation
smaller pixels
less material
better resolution

DEPFET: Belle II
MAPS: STAR@RHIC
and future
ALICE ITS

assumed lifetimes:
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years



2.7/0.27 is EGT



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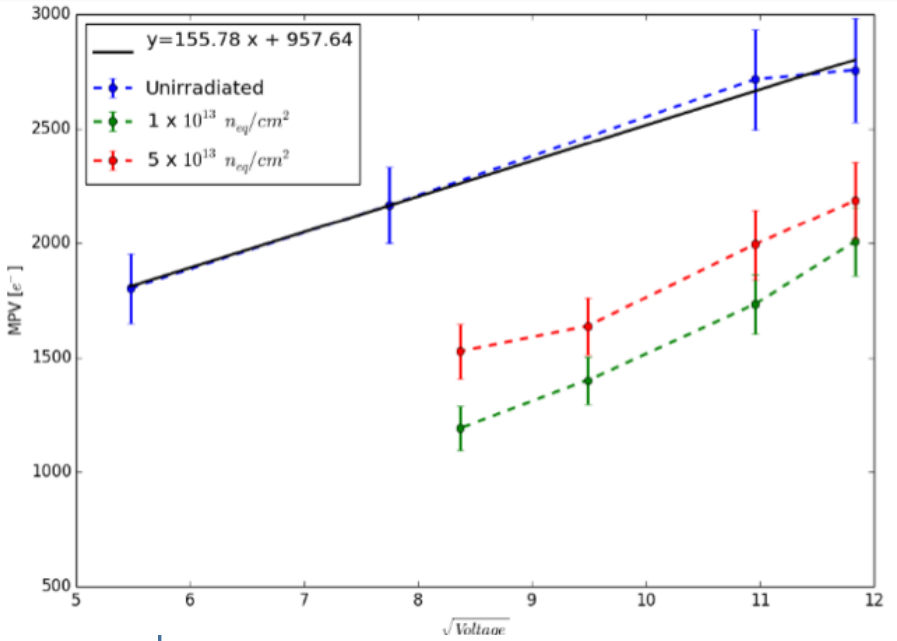
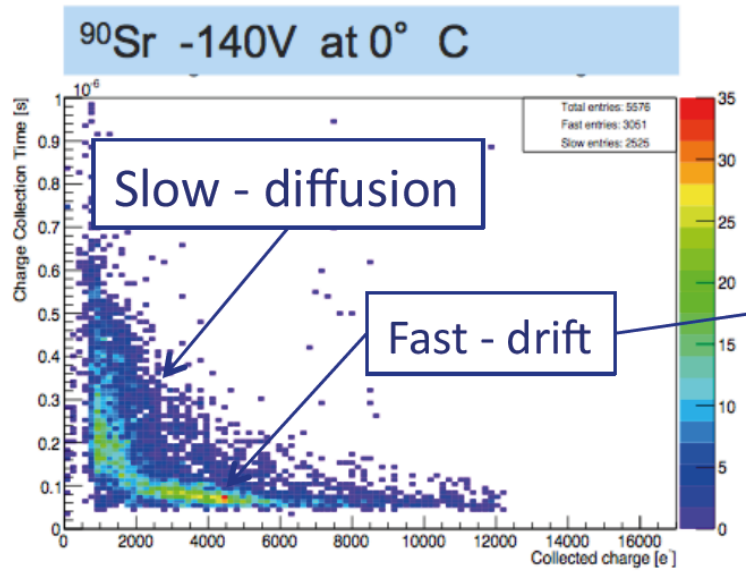
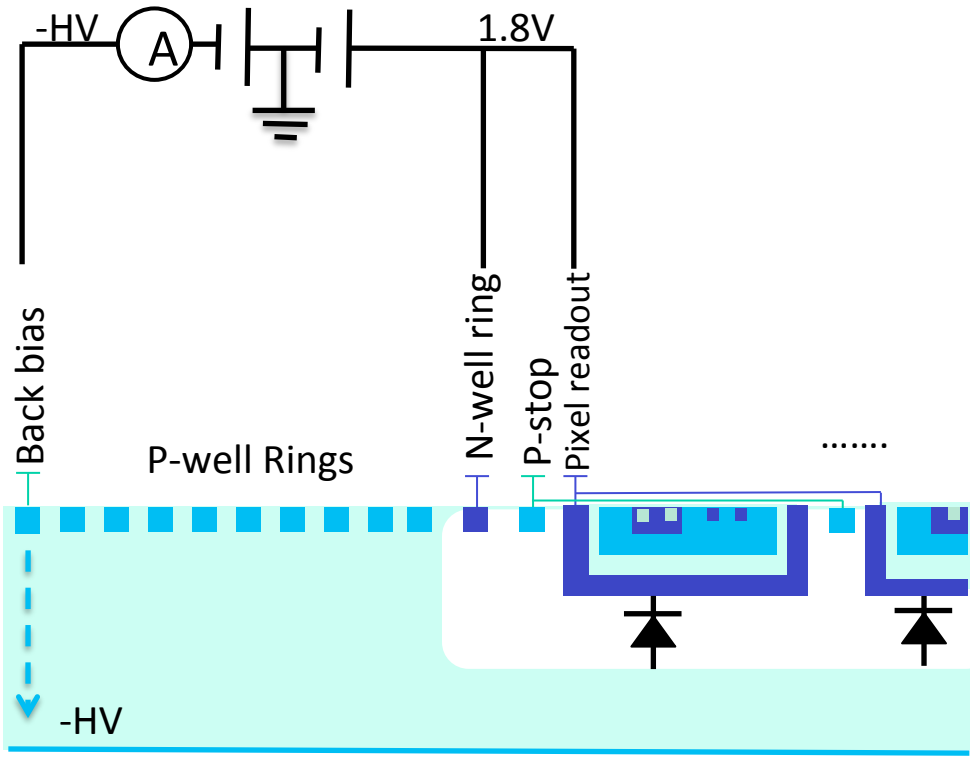


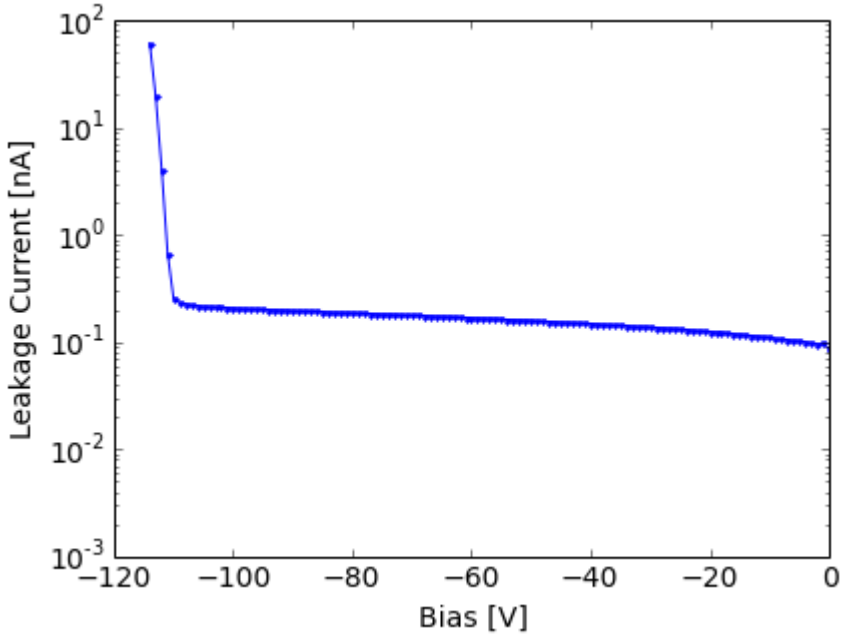


Structure of CCPD_LF

- IV curves (Version A)

1.8V on collection well
negative high voltage on “Back bias”



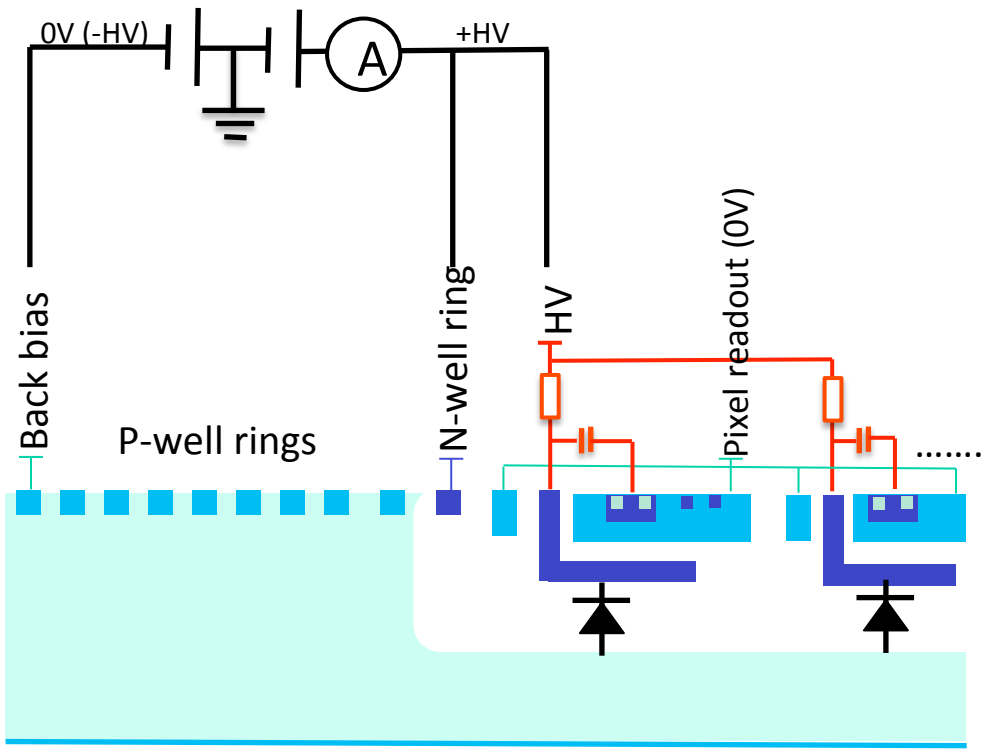


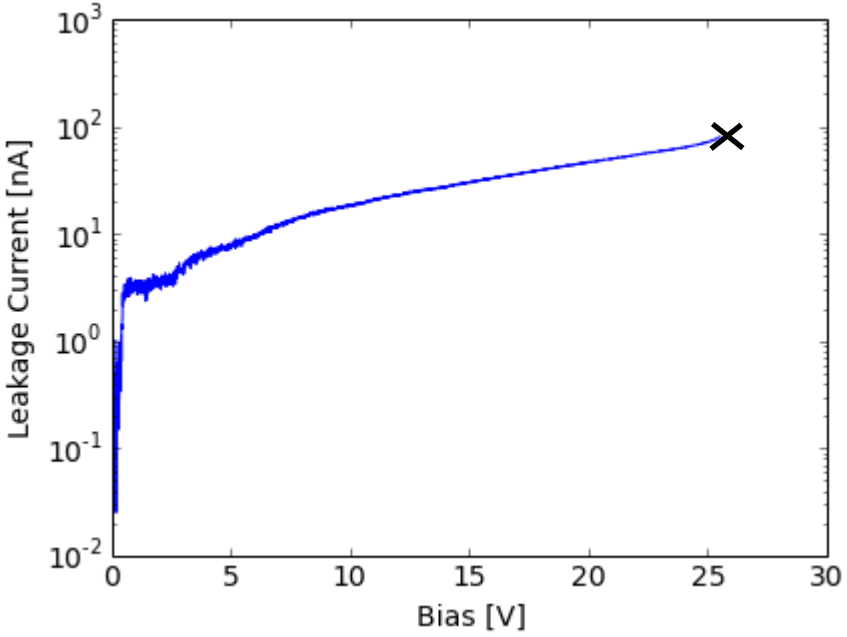
Breakdown = -114V

Structure of CCPDLF

- IV curves (Version B)

positive high voltage on collection well, “HV”
HV and electronics are coupled with C





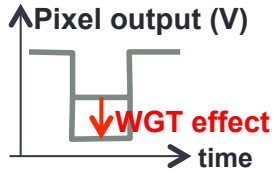
High voltage was applied without breaking the capacitor

CCPD_LF tests results

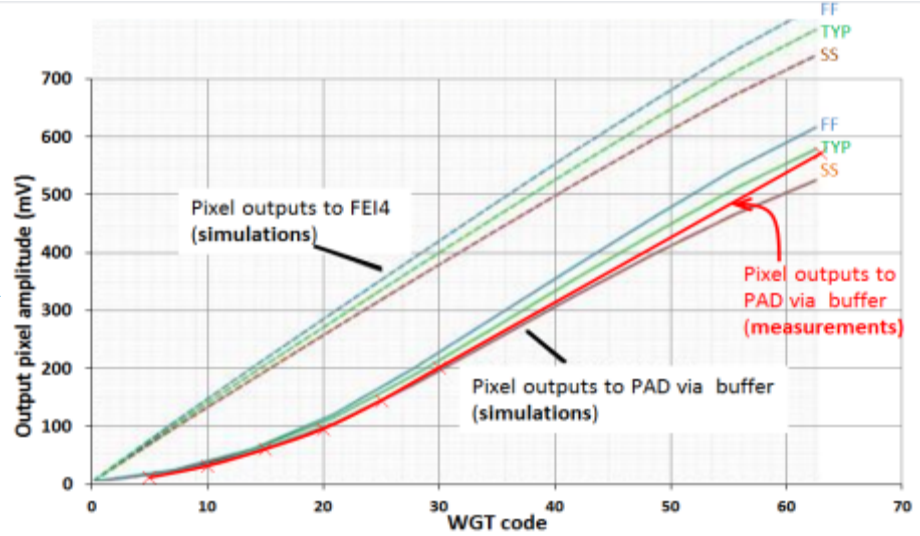
1. Bias Generator functioning :

- The Bias cell is composed of 11 6-bit DACs and generates all the bias for the pixels.
- Simulations and tests of the DACs give similar results:
  - Internal voltage reference:

    1,202V in test / 1,134V in simulation
  - Example with the DAC of WGT bias:



WGT customizes the weight (amplitude) of the pixel output.

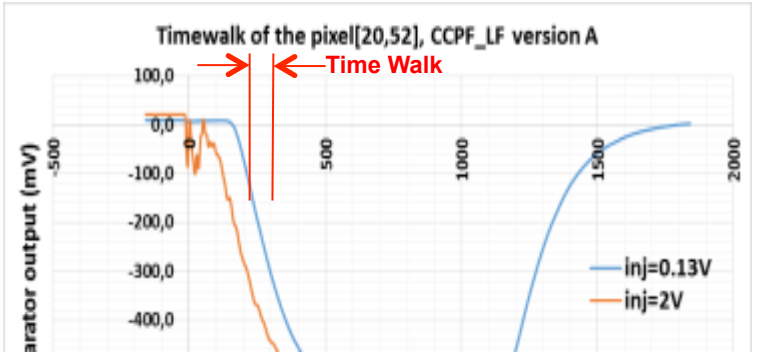


Pixel output amplitudeas a function of global DAC (WGT) setting.

2. Time Walk of CCPD_LF version A :

- The Time Walk is presented here as the delay between the comparator responses of a small signal and a huge signal.
- **Measurements with the Injection** (0,13V and 1,6V at BL=0,75V and TH=0,8V):

	Pixel type	Time Walk
Pixel<20,52>	FB L=0,9µ	**~57ns**
Pixel<12,52>	FB L=1,5µ	**~56ns**
Pixel<4,52>	FB ELT	**~53ns**



Definition of the TimeWalk

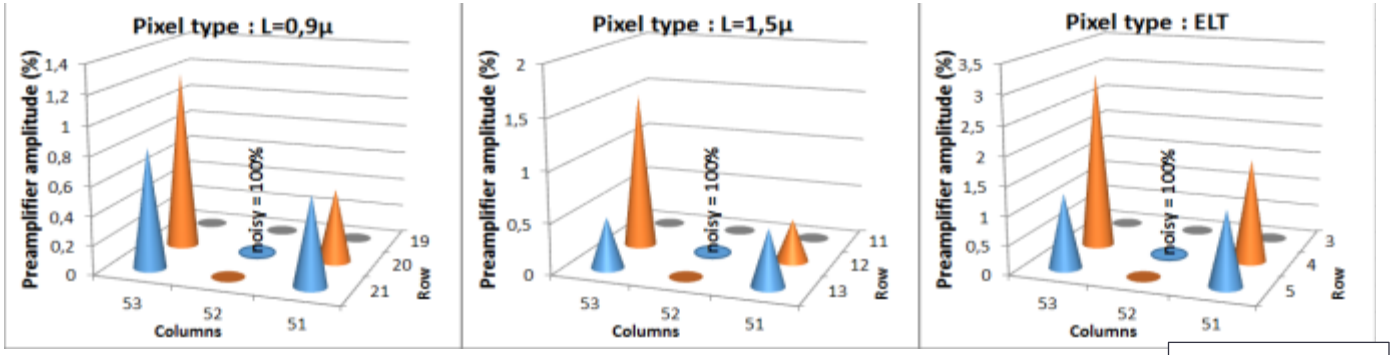
A **schematic simulation** with a parasitic circuit (L,R and C) for the path of the Injection gives **~57ns**.

Note : The TimeWalk measured/simulated with the Injection is high due to the parasitic elements on Injection signal. **So the TimeWalk should be reduced with "real" charge (i.e. with a source).**

CCPD_LF tests results

3. CrossTalk measurements with the Injection:

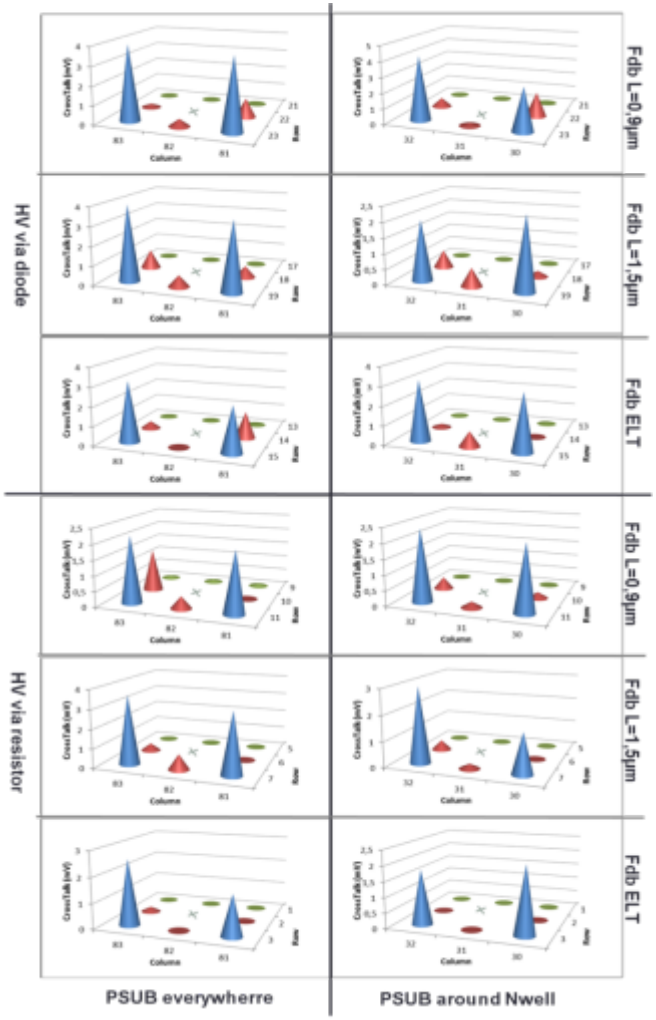
- The CrossTalk is measured on a sub-matrix of 3x3 pixels. The pixel in the middle is the only one which accepts the Injection.
- Measurements for version A :



Preamplifier response of the peripheral pixels (relative to the central pixel)

BL=0,75V
TH=1V
1V of injection

for version B :



a) CrossTalk is seen only between pixels which belong to the same group of 6-pixels.

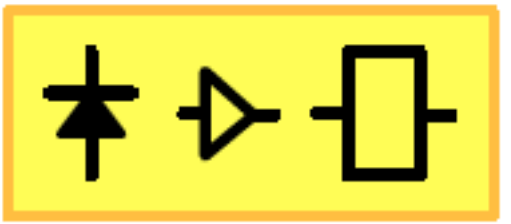
b) For ver B : The CrossTalk is MAINLY between the 3 pixels connected to the same FEI4-plate

   For ver A : The CrossTalk appears on the 6 pixels.

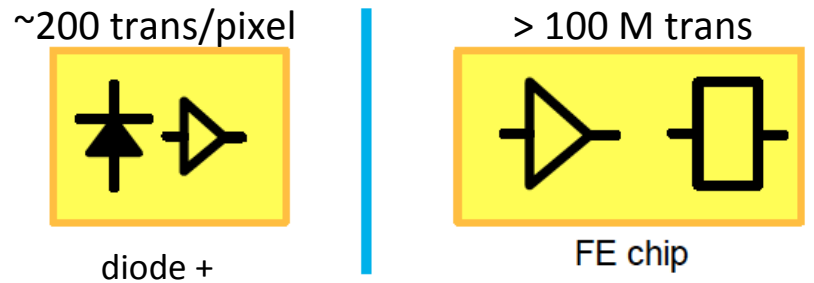
c) The value of the cross-talk is small (only a few percent relative to the amplitude of the injected pixel in the middle).

One can think of different realisations for the Inner Tracker Upgrade

- ❑ fully monolithic providing the complete R/O architecture on-chip (FE-I3 or FE-I4 like)

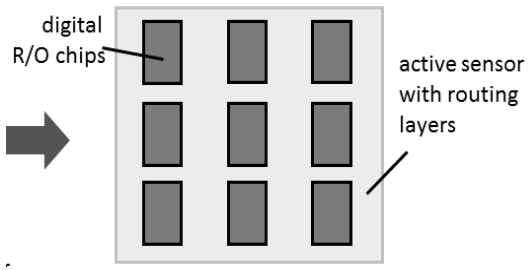


- ❑ smart CMOS pixel sensor + FE-chip



- ❑ Sparsified CMOS

exploiting in-Si routing options and possibly large bump pitches, eg C4 bumps, for low cost



current focus of CMOS demonstrator WG using well understood FE-I4 as R/O chip

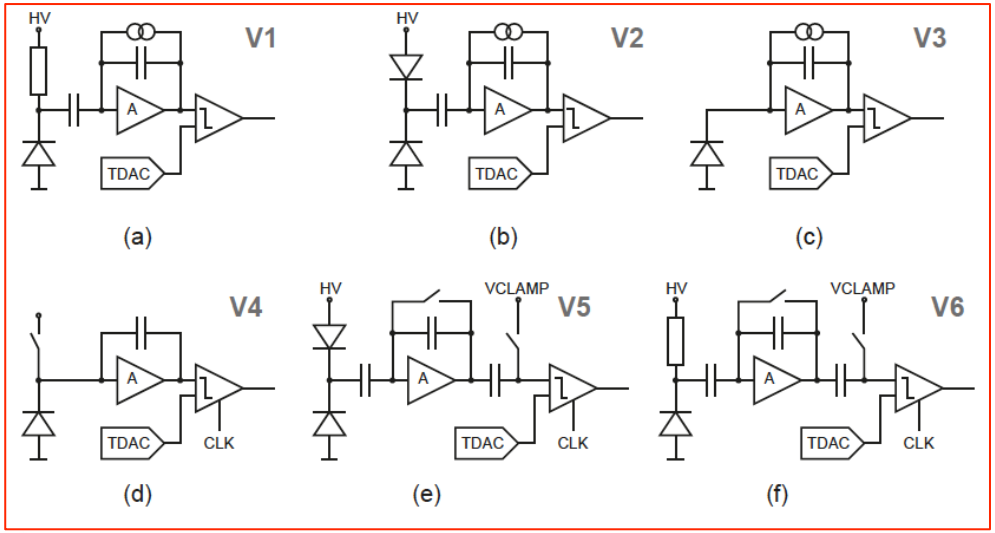
demands/requirements are quite different for inner pixel layers (r=3-6 cm, small area) and outer pixel layers (r > 25 cm, large area)

see also poster by Heinz Pernegger

ESPROS prototypes: test chips EPCB01 and EPCB02

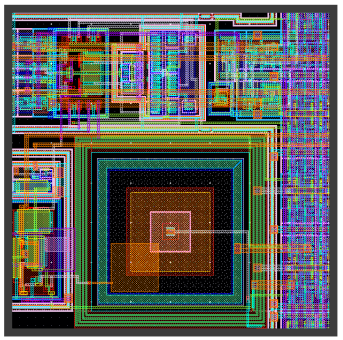
universitätbonn

- 150nm CMOS, 6 metal layers
- deep p-well, isolated full CMOS
- substrate: **n-type bulk** (> 2 kΩ cm)
- bias voltage up to 20V
- **50µm thin + p-implant (backside)**
- 6 pixel matrices
- pixel size: 40 × 40µm²
- **~50 µm depletion depth**

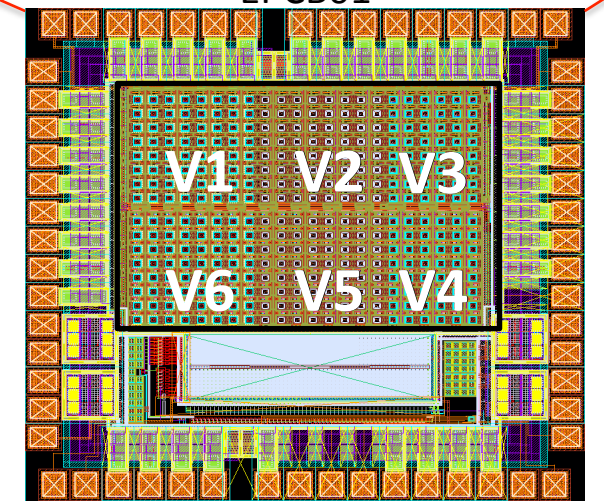


main goal: characterization of designs & technology

Matrix version	Biasing & coupling	Analog FE
V1	Resistor + AC	Continuous
V2	Diode + AC	Continuous
V3	Direct + DC	Continuous
V4	Direct + DC	Switched
V5	Diode + AC	Switched
V6	Resistor + AC	Switched



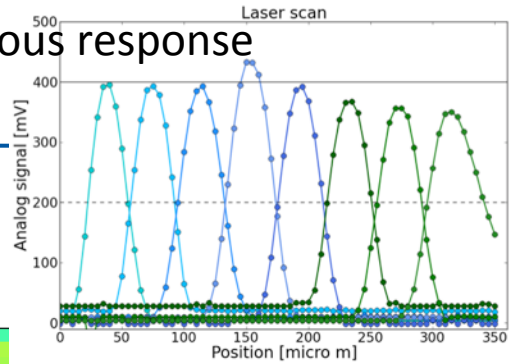
EPCB01



Design & testing: Bonn, Prague

EPBC01 & EPBC02 (improved version)

homogeneous response to laser



- Best values for **V2:**
  - Noise = 25e-
  - Gain = 135 µV/e- spread = 11µV/e-
- Threshold dispersion
  - 80e- after tuning (V2 @1000e-)
- some charge loss in EPBC01, no loss in EPCB02
- irradiations ongoing