Contribution ID: **241** Type: **Poster**

The Level 0 trigger processor for the NA62 experiment

Thursday, 28 May 2015 17:32 (0 minutes)

The NA62 experiment at CERN SPS is devoted to the measurement of the very rare kaon decay K+-> pi+ nu nubar. The expected branching ratio has been recently estimated to be of the order of 10−10, thus requiring a high intensity kaon beam. The high rate of incident particles affects the design of the trigger and data acquisition for the experiment. In particular, the lowest level (L0) trigger represents a crucial component in reducing the event rate, estimated to be about 10 MHz, by a factor 10 with a maximum latency of 1 ms. More recently, the implementation of trigger processors has been based on FPGA devices, gaining great flexibility in maintaining, improving filter algorithms and configuring hardware functionalities by specific programming languages. For the NA62 experiment, two approaches for the realization of L0 trigger processor were developed. A first approach is totally based on the use of a commercial FPGA, while the second one joins a commodity PC to the same tool. In both cases the FPGA device receives data from detectors via Gigabit Ethernet links and routes selected triggers to the local trigger unit of the experiment. In the second approach data are immediately stored, via PCI-express, into the DDR memory of the PC, which performs the event selections. The first approach features fully real-time processing with guaranteed constant latency, but limitations appear in the limited FPGA resources, concerning algorithm implementation and memory depth. On the other hand, in the PC-based trigger processor the implementation of complex algorithms is much simpler and any maintenance operation does not imply to re-configure the FPGA. Anyway, one can lose the full synchronization inside L0 because the PC does not respond as a real-time device.

Summary

Two approaches were developed for realization of Level 0 trigger processor for the NA62 experiment at Cern. The first approach is totally based on a FPGA device while the second one joins an off-the-shelf PC to the FPGA. The performance of the two systems will be compared.

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Session Classification: Front end, Trigger, DAQ and Data Management - Poster Session

Track Classification: S5 - Front End, Trigger, DAQ and Data Management