The Level 0 Trigger Processor for the NA62 Experiment

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Summary

- At the NA62 experiment at CERN the **high rate** of incident particles affects the design of the **trigger** and DAQ system.
- **The Level 0 trigger (L0)** is crucial because it must reduce an event input rate of 10 MHz to 1 MHz within a maximum latency of 1 ms.
- For realization of Level 0 Trigger Processor (**L0TP**) **two approaches** were developed.
- The first approach is totally based on a commercial **FPGA** device while the second one joins an off-the-shelf **PC** to the FPGA.
- The performance of the two systems are highligthed and compared.