ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade

Magnus Mager (CERN)

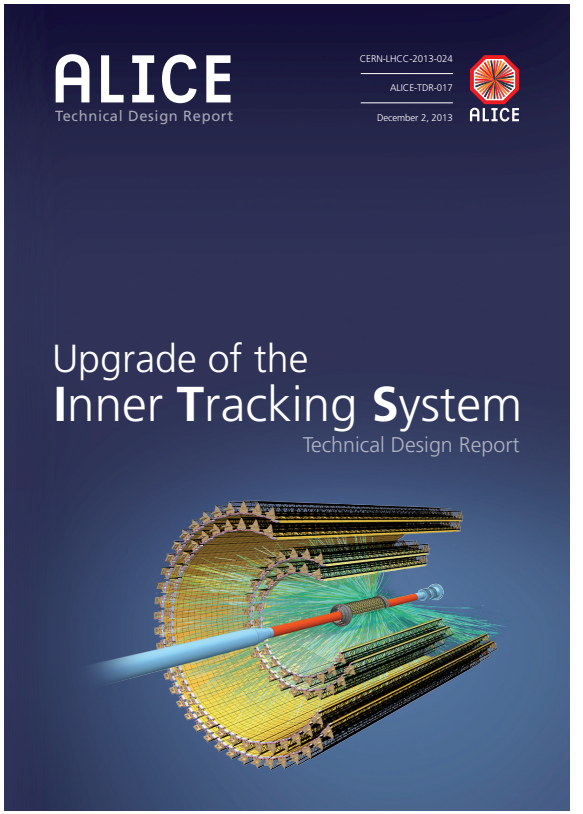
on behalf of the ALICE collaboration

Contents

Contents

ITS upgrade

- Main goal: replacement of ALICE Inner Tracking System (ITS) during LHC long shutdown II in 2018–2019
- Design objectives:
  - **Increased spatial resolution:**
    - $\lesssim 5\,\mu m$ in longitudinal and transverse directions
  - **Closer to interaction point:**
    - move to $r = 23\,mm$
  - **Reduced material:**
    - aiming at $\lesssim 0.3\,\%\ X_0$ for innermost layers
    - additional benefit from thinner beam pipe
  - **Increased readout speed:**
    - Record 50 kHz Pb–Pb collisions (minimum bias)



CERN-LHCC-2013-24
fully approved

ALICE

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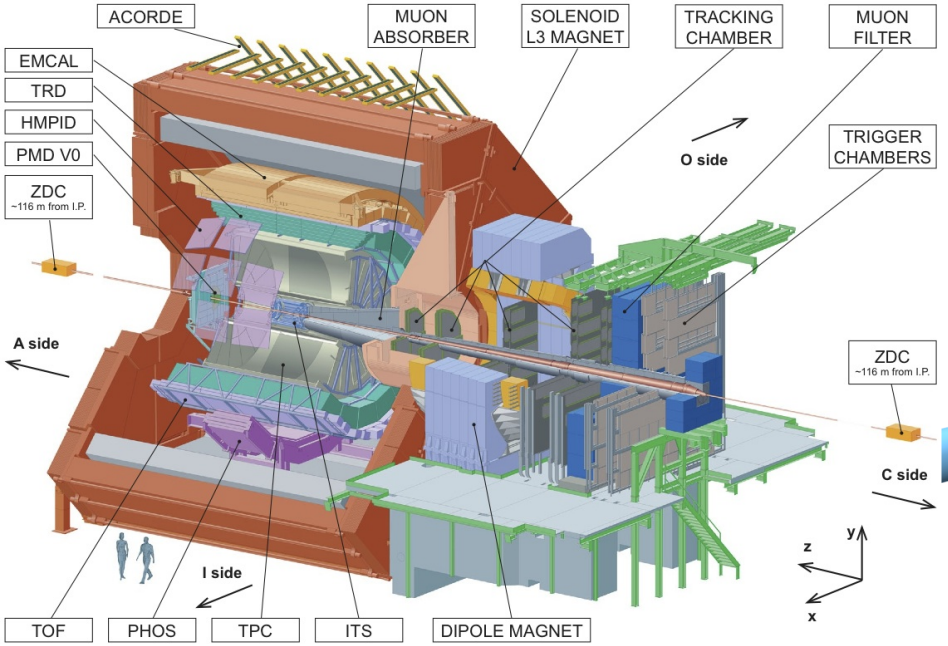
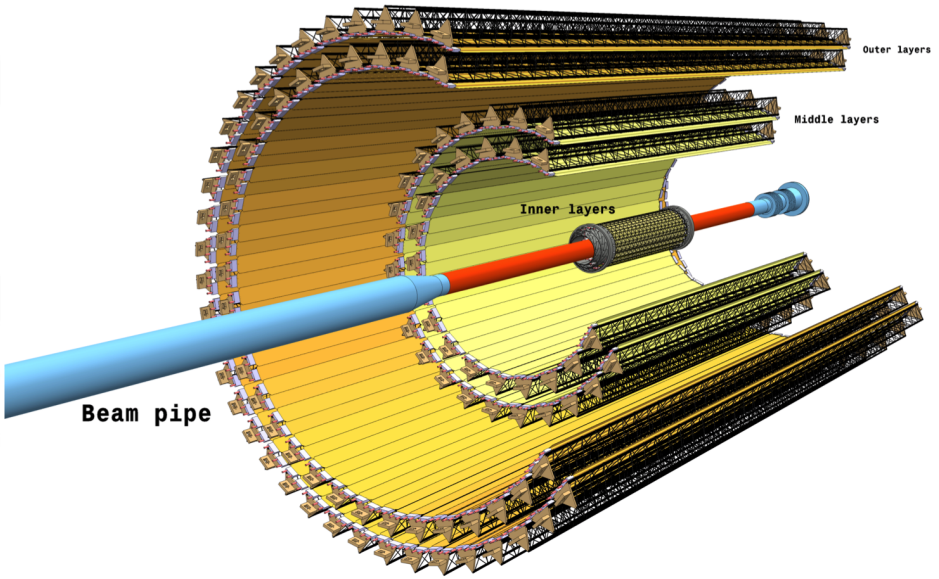
J. Phys. G **41** 087002

Detector design





- 7 layers of monolithic active pixel sensors (MAPS)
  - 3 layers in inner barrel with $X/X_0 \approx 0.3\,\%$ from $r = 23\,\text{mm}$
  - 2+2 layers in outer barrel with $X/X_0 \approx 1\,\%$ to $R = 400\,\text{mm}$
  - Total area of about $10\,\text{m}^2$
- Coverage: $2\pi \times (|\eta| \leq 1.22)$ for 90 % most luminous region

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Sensor requirements

Parameter	Inner Barrel	Outer Barrel
Sensor thickness	50 µm	50 µm
Spatial resolution	5 µm	10 µm
Dimensions	15 mm × 30 mm	15 mm × 30 mm
Power density	300 mW cm^{-2}	100 mW cm^{-2}
Time resolution	30 µs	30 µs
Detection efficiency	99 %	99 %
Fake hit rate*	10^{-5}	10^{-5}
TID radiation hardness**	2700 krad	100 krad
NIEL radiation hardness**	1.7×10^{13} 1 MeVn_{eq}/cm^2	10^{12} 1 MeVn_{eq}/cm^2

* per pixel and readout

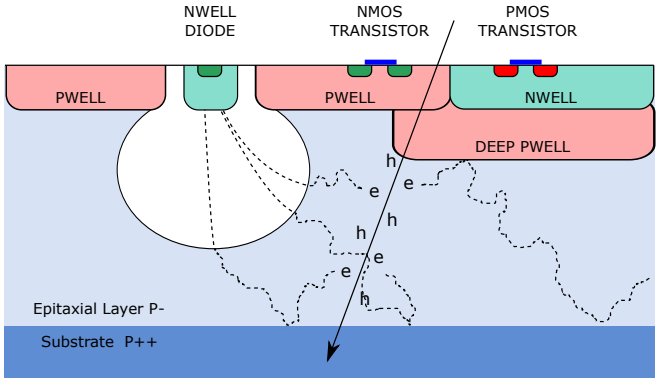
** including a safety factor of 10, revised numbers wrt. TDR

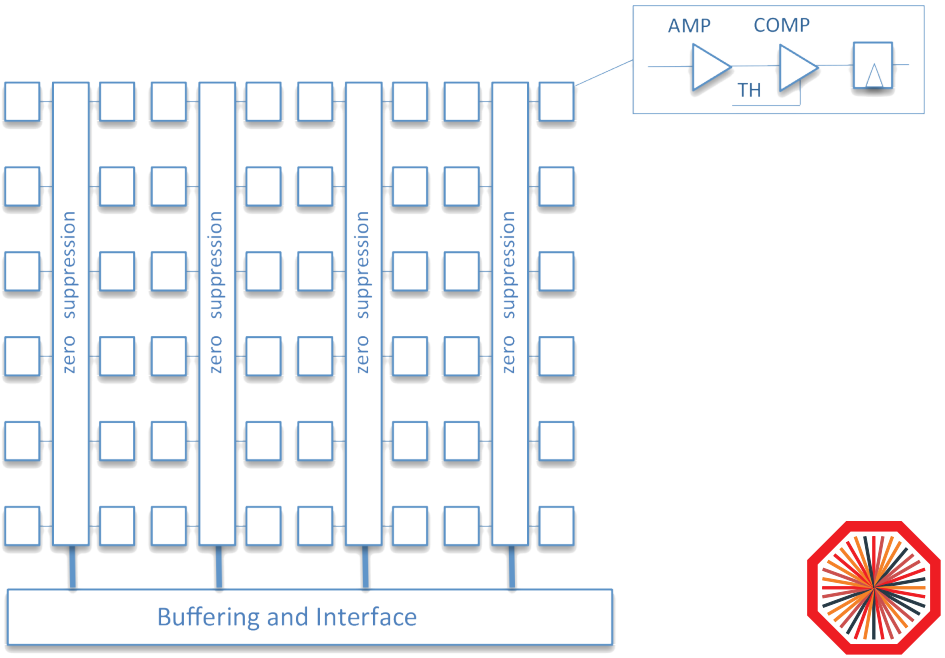
- ⇝ Well suited for Monolithic Active Pixel Sensors
- Two (pin-)compatible sensors are being developed:
  - ALPIDE (project baseline; this presentation)
  - MISTRAL-O (more classical approach, optimised for outer barrel)

Contents

Architecture

- Use of TowerJazz 180 nm CMOS Imaging Sensor process
  - deep p-well (full CMOS within matrix)
  - high density (complex in-pixel circuitry)
- In-pixel amplification, discrimination and hit storage
  - no transmission of analogue signals over the matrix
- Combinatorial readout of fired pixels ("priority encoder")
  - reduced digital switching (power)
  - higher readout speed
- Possibility to apply moderate ($\leq$8 V) reverse substrate bias





Specifications

- **Dimensions**
  - 1.5 cm × 3 cm, 512 × 1024 (rows × columns) 28 µm × 28 µm pixels
  - total thickness: 50 µm, epitaxial layer (>1 kΩ cm) thickness: 18 µm
- **Power supply**
  - analogue: 11 mA at 1.8 V
  - digital: 90 mA at 1.8 V
  - total: 40 mW cm^{-2}
- **Interface**
  - flip chip mounted onto flex PCB using pads over matrix
  - high-speed serial link (1.2 Gb/s 8b10) driver capable of driving 5 m cables
- **Detection efficiency and fake rate**
  - $\gg$99 % at $\ll 10^{-5}$ fake hits per pixel and event
- **Resolution**
  - space: ≈5 µm (tested with perpendicular MIPs)
  - time: ≈2 µs
- **Radiation tolerance**
  - 1.7×10^{13} 1 MeVn_{eq}/cm^2 (NIEL)
  - 2700 krad (TID)

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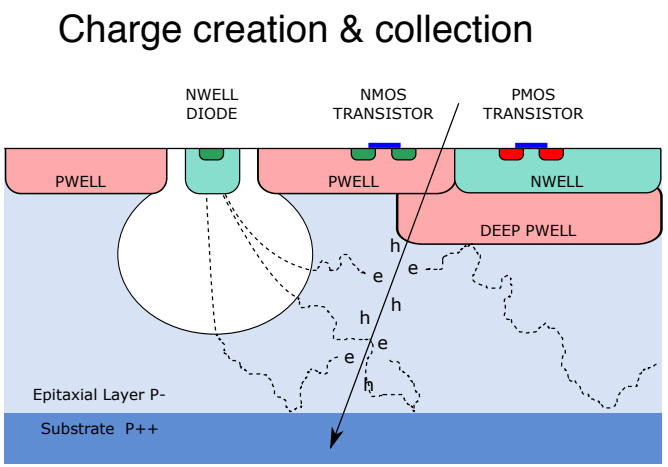
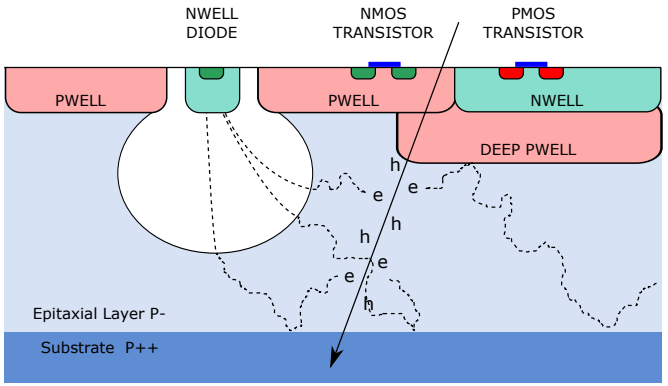
Principle of operation



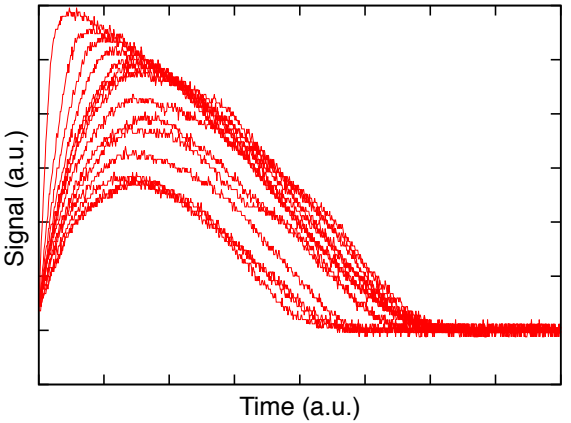
- Charge is created in the epitaxial layer

Principle of operation

Charge creation & collection

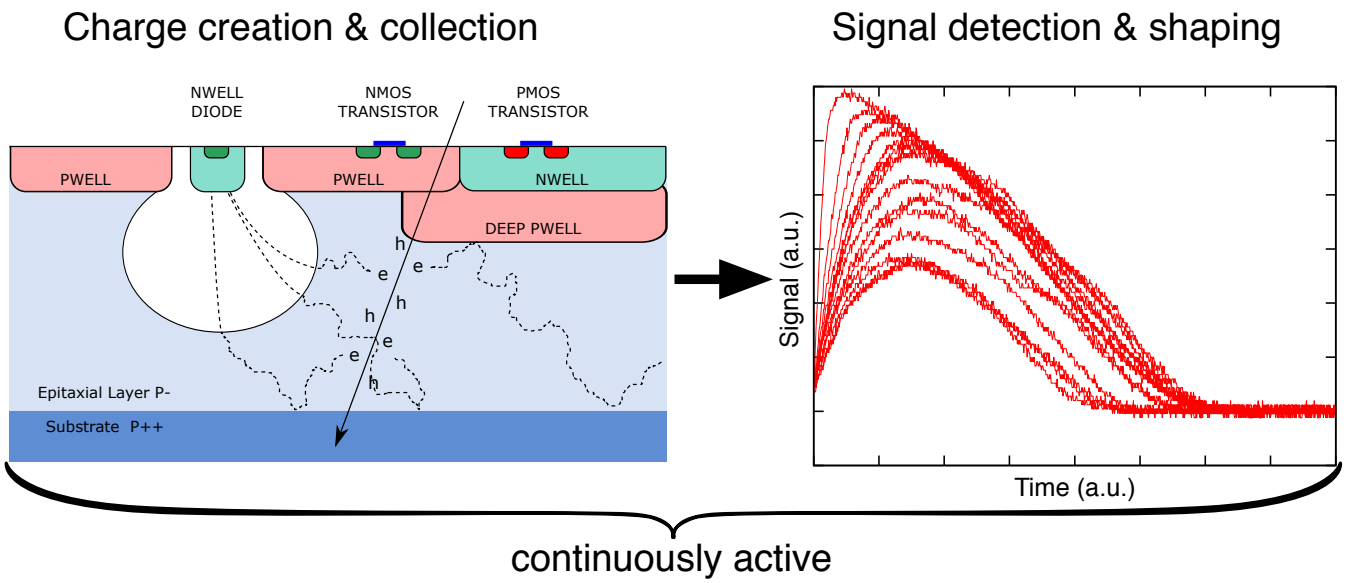


Signal detection & shaping



- Charge is created in the epitaxial layer
- Signal is shaped:
  - rise-time: $<2\,\mu s$ (defines timing resolution)
  - total pulse length: $10\,\mu s$ to $20\,\mu s$

Principle of operation



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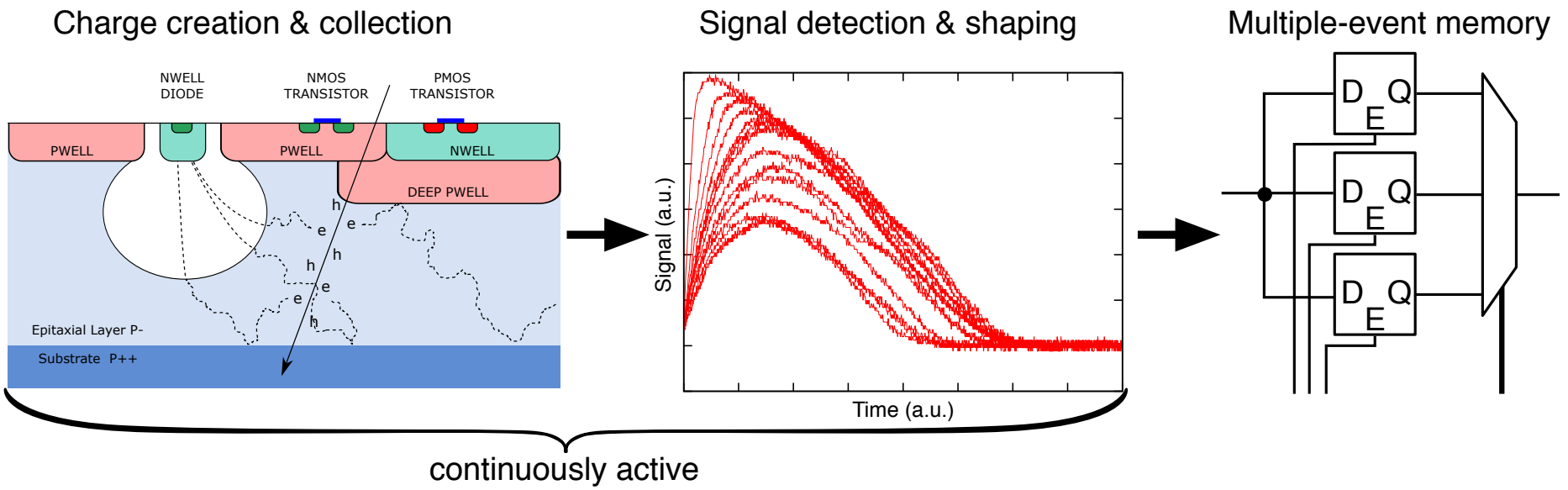

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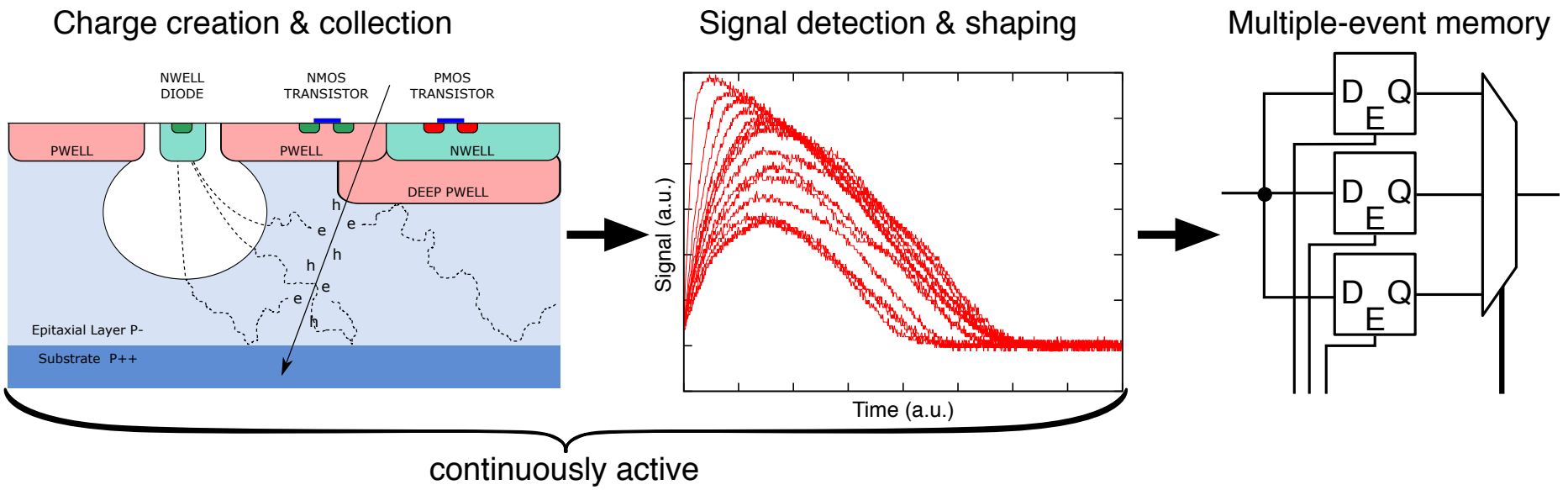
- Signal is strobed into memory
  - either upon trigger
  - or with constant frequency (continuous/"trigger-less" operation)

Principle of operation



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- Front-end acts as delay line
- Signal is strobed into memory
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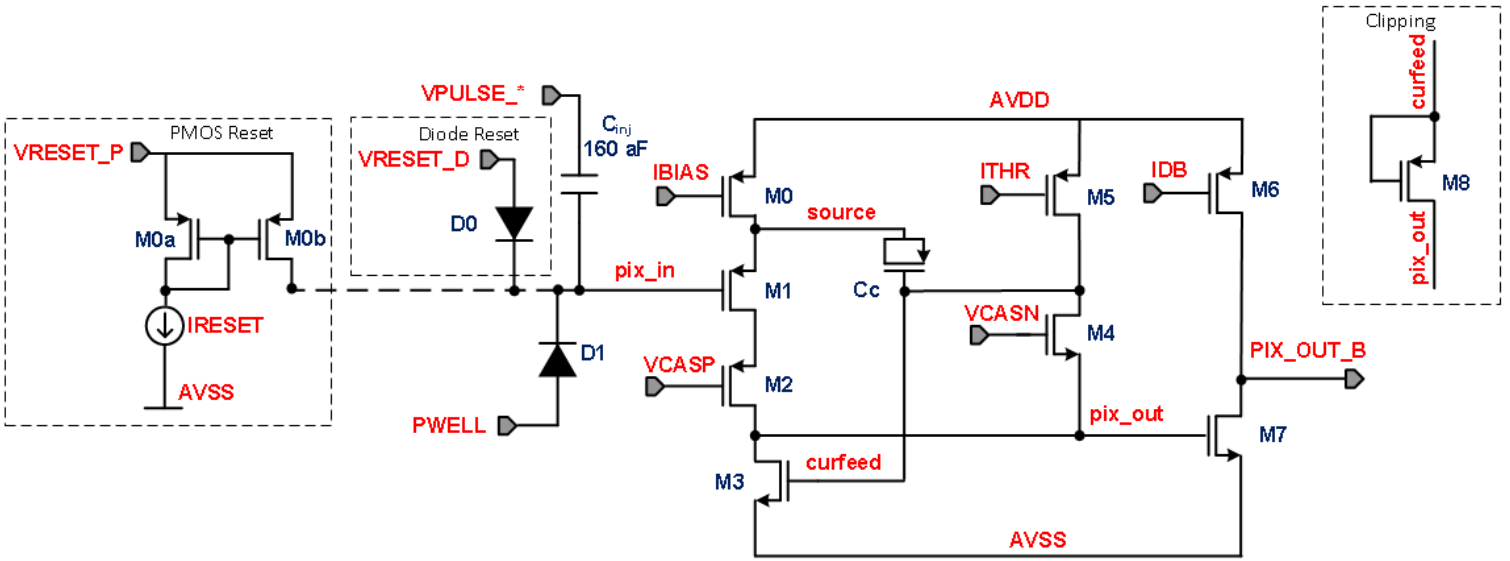
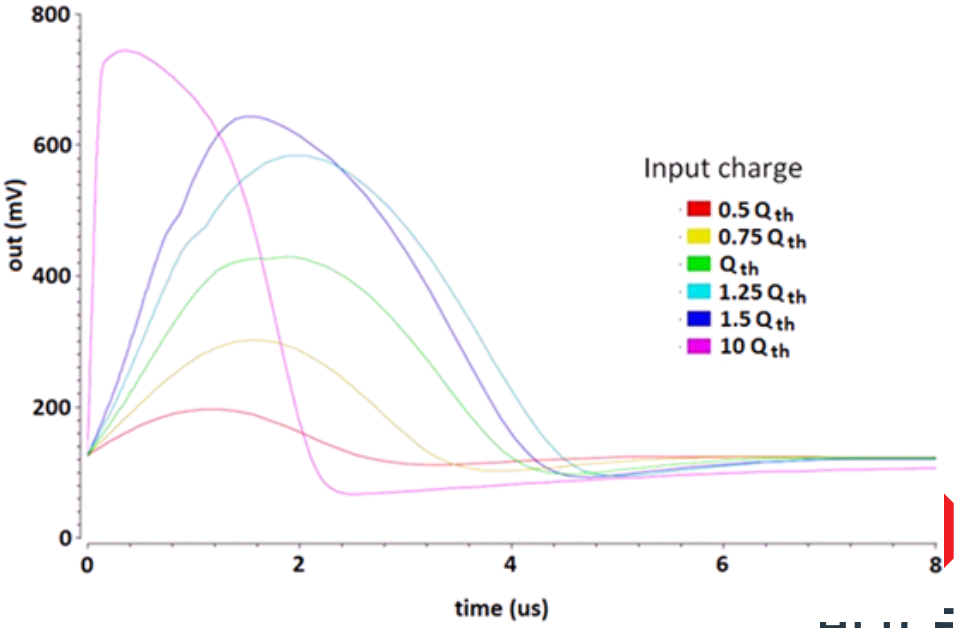
  - or with constant frequency (continuous/"trigger-less" operation)
- Hit pixels are read out asynchronously

In-pixel front-end circuit

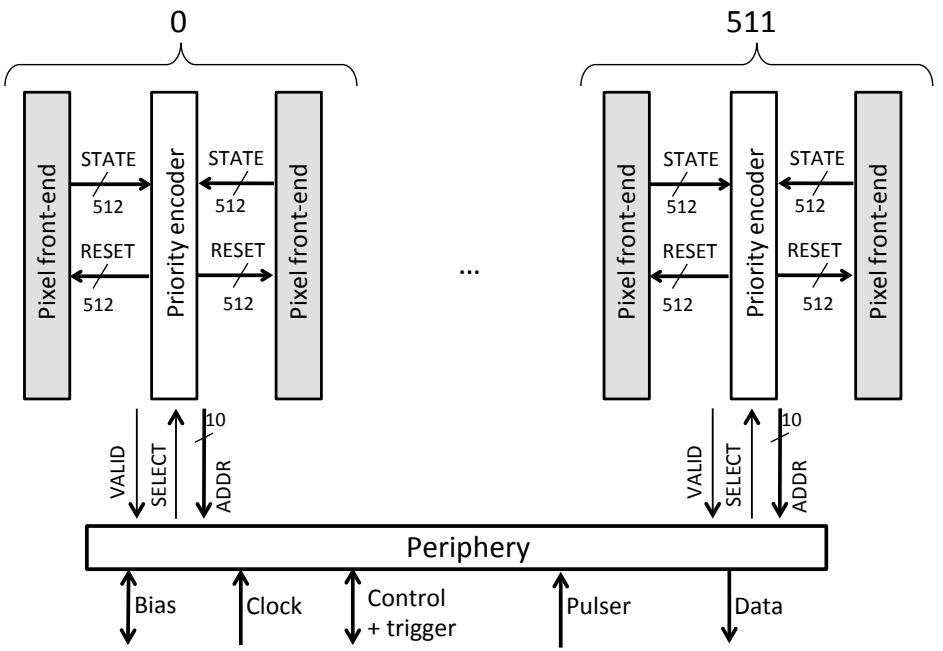


- One main current branch
- AC sensitive to negative charge input
- Non-linear dependence on input charge

⇝ Very low power consumption:
$I_{\text{bias}} = 20\,\text{nA}$, $I_{\text{thr}} = 500\,\text{pA}$
(or: ≈40 nW per pixel)



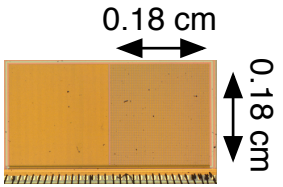
Readout



- The matrix is read out asynchronously and sparsely by use of 512 priority encoders
- High speed serial point-to-point link with up to 1.2 Gb/s (8b/10b) for data readout
- Serial bus for configuration and triggering (≈40 MHz)
- *More details in Adam Szczepankiewicz's presentation later today*

Contents

Prototype generations

Timeline	Layout	Pixels
2012 Explorer (analogue)		90 × 90 (20µm × 20µm) 60 × 60 (30µm × 30µm)

not to scale

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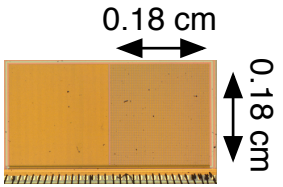
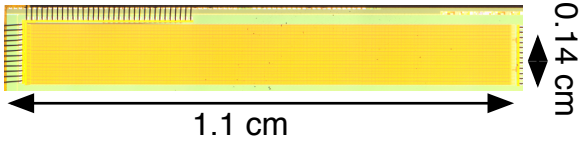
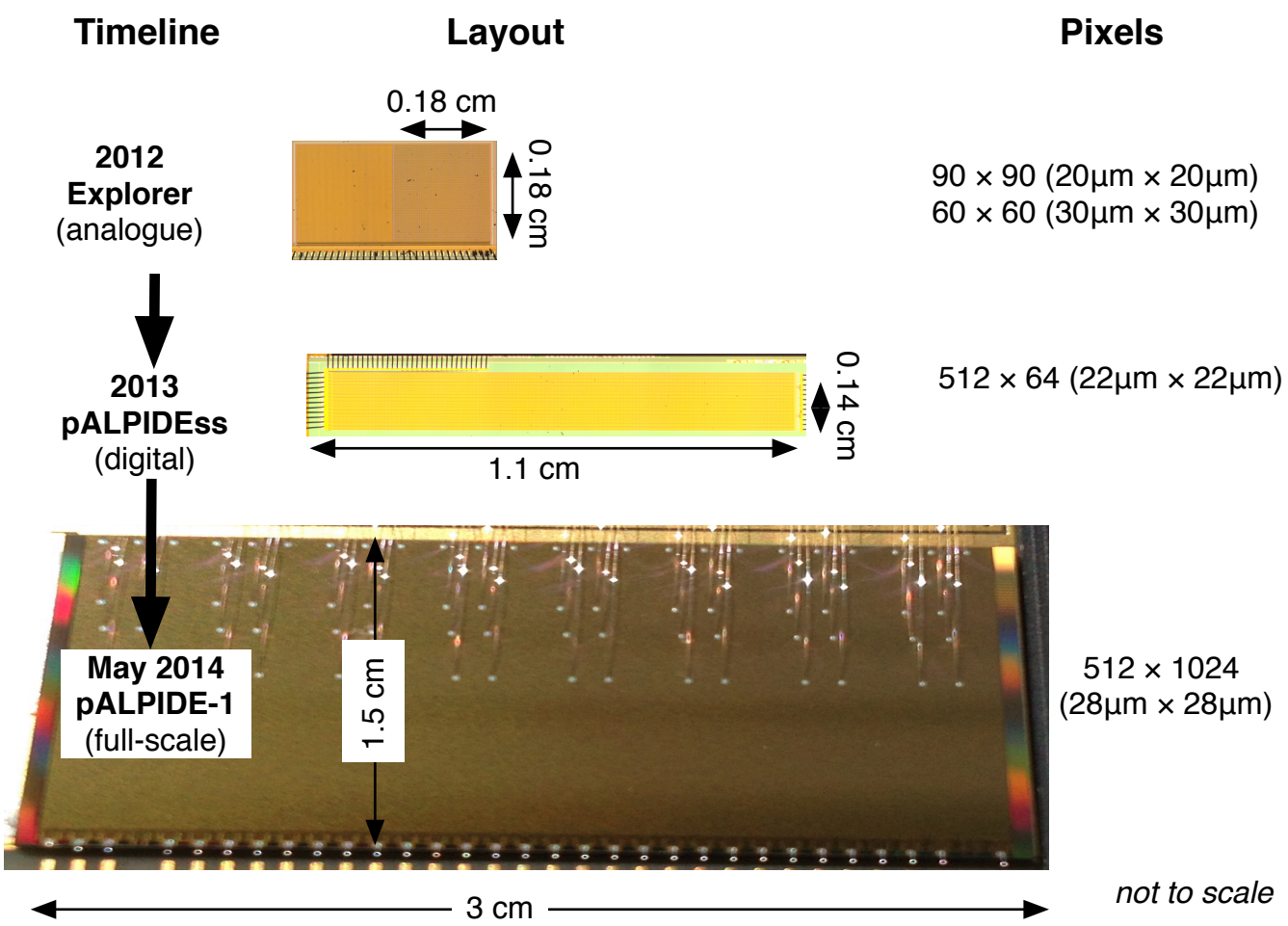
2012 Explorer (analogue)		90 × 90 (20µm × 20µm) 60 × 60 (30µm × 30µm)
2013 pALPIDEss (digital)		512 × 64 (22µm × 22µm)

not to scale

Prototype generations



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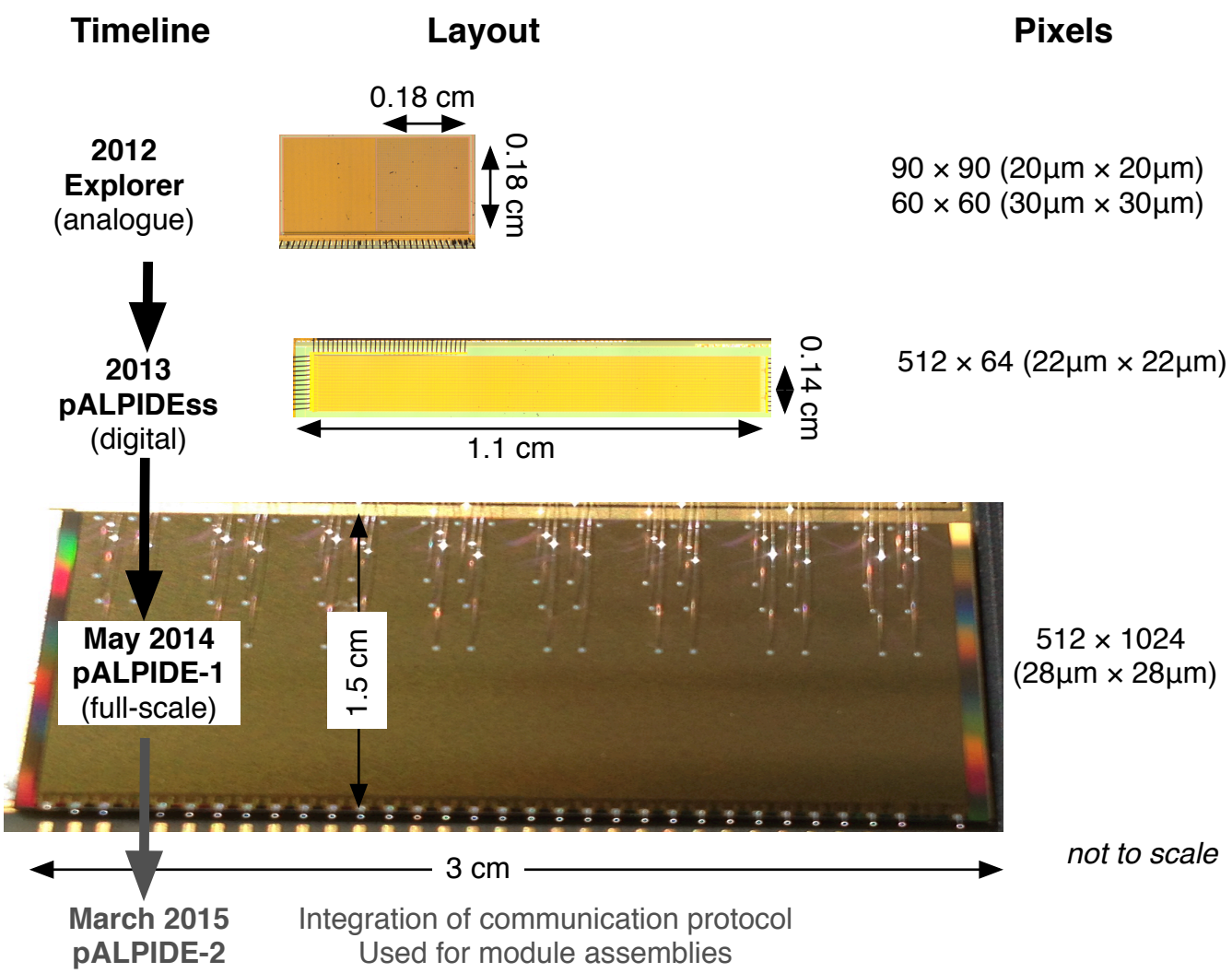

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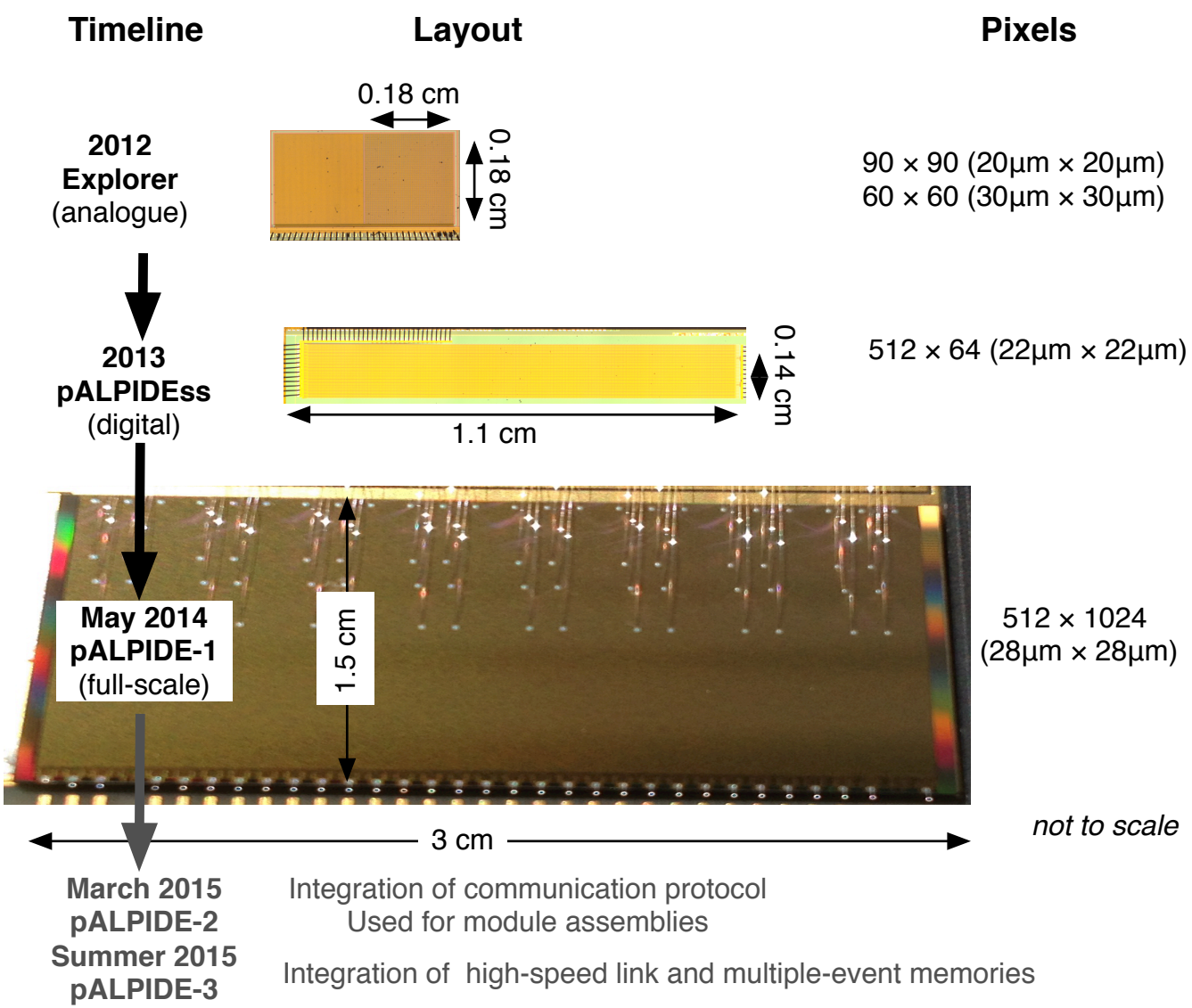

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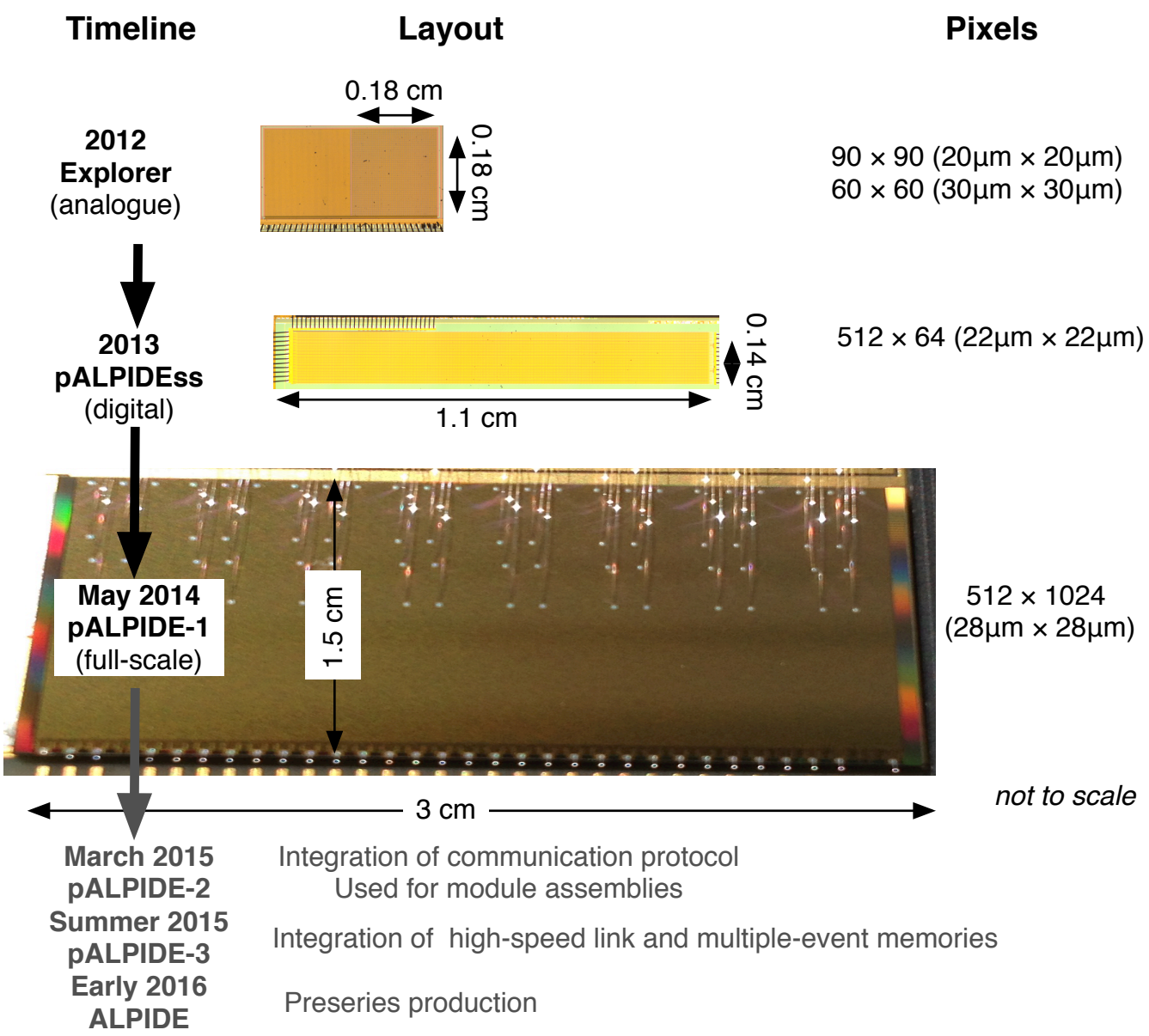
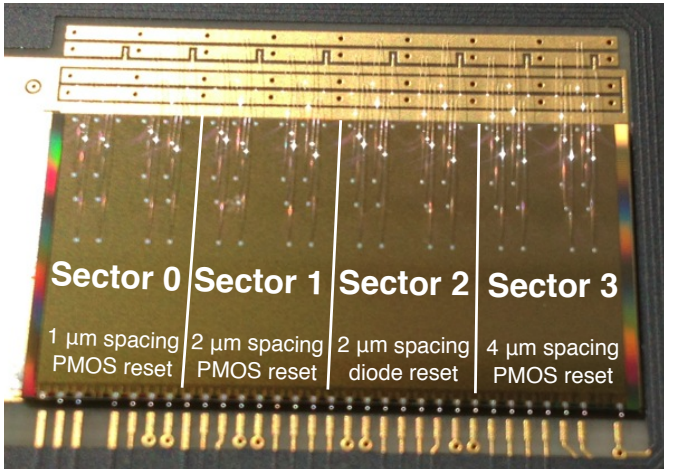
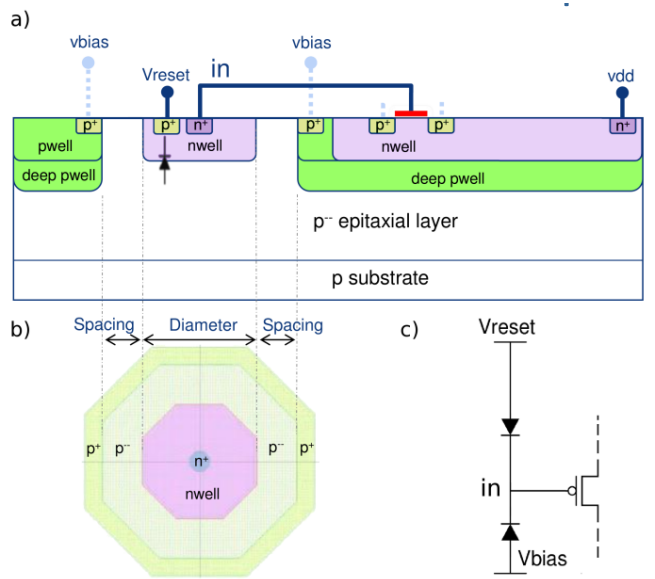


pALPIDE-1 specifications

- Pixel pitch: $28\,\mu m \times 28\,\mu m$
- Power consumption: $<40\,mW\,cm^{-2}$
- Diode: 4 different flavours
- Multiple-event memory: 1 register (ALPIDE: 3)
- Readout: 8-bit 40 MHz parallel interface (ALPIDE: high-speed serial link)

- Peaking time: $2\,\mu s$
- Pulse length: $10\,\mu s$ to $20\,\mu s$
- Fake-hit rate: $\ll 10^{-5}$ per pixel and event
- Detection efficiency: $\gg 99\,\%$

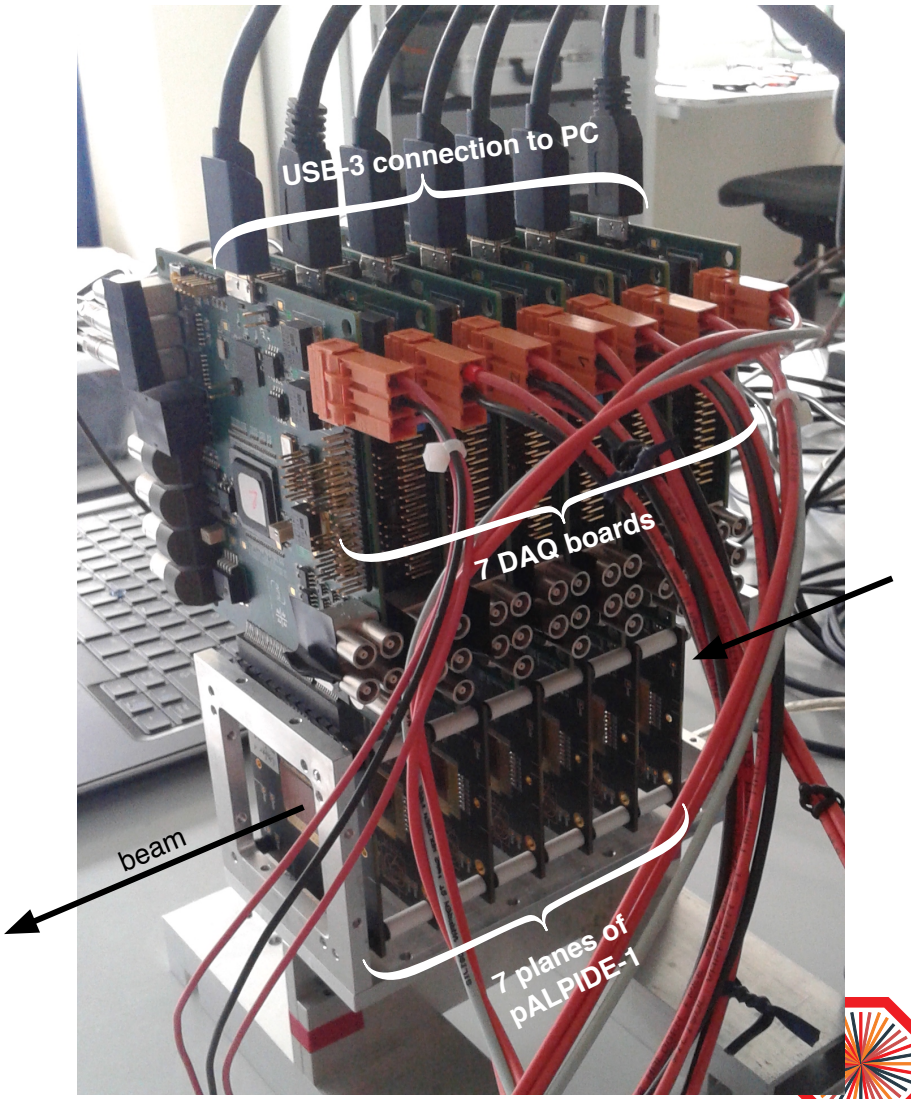




Contents

Test beam set-up

- Test beams are carried out using a telescope made entirely of pALPIDE-1
- Extensive campaign with beams at PS, SPS, PAL (Korea), BTF (Italy), DESY (Germany)
- In the following: results with 6 GeV/c π^- from CERN PS
- Tests before and after neutron irradiation



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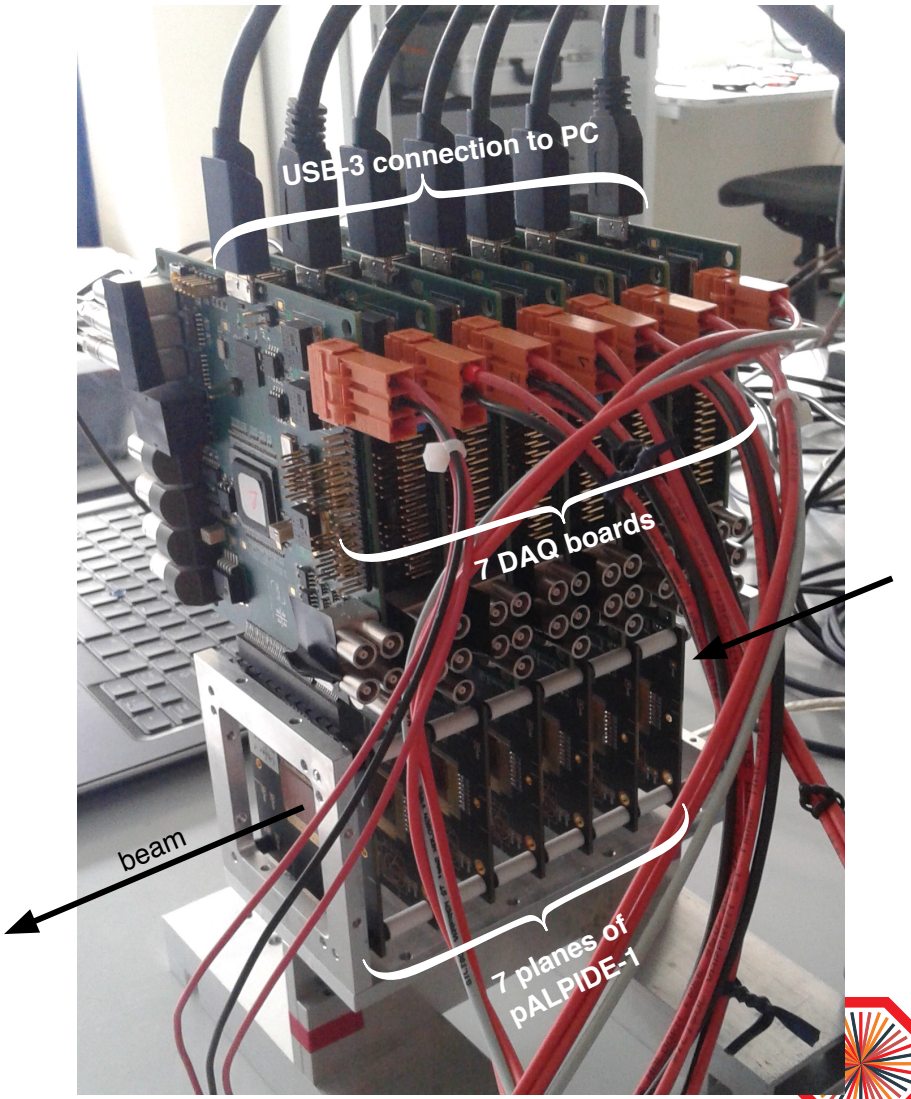
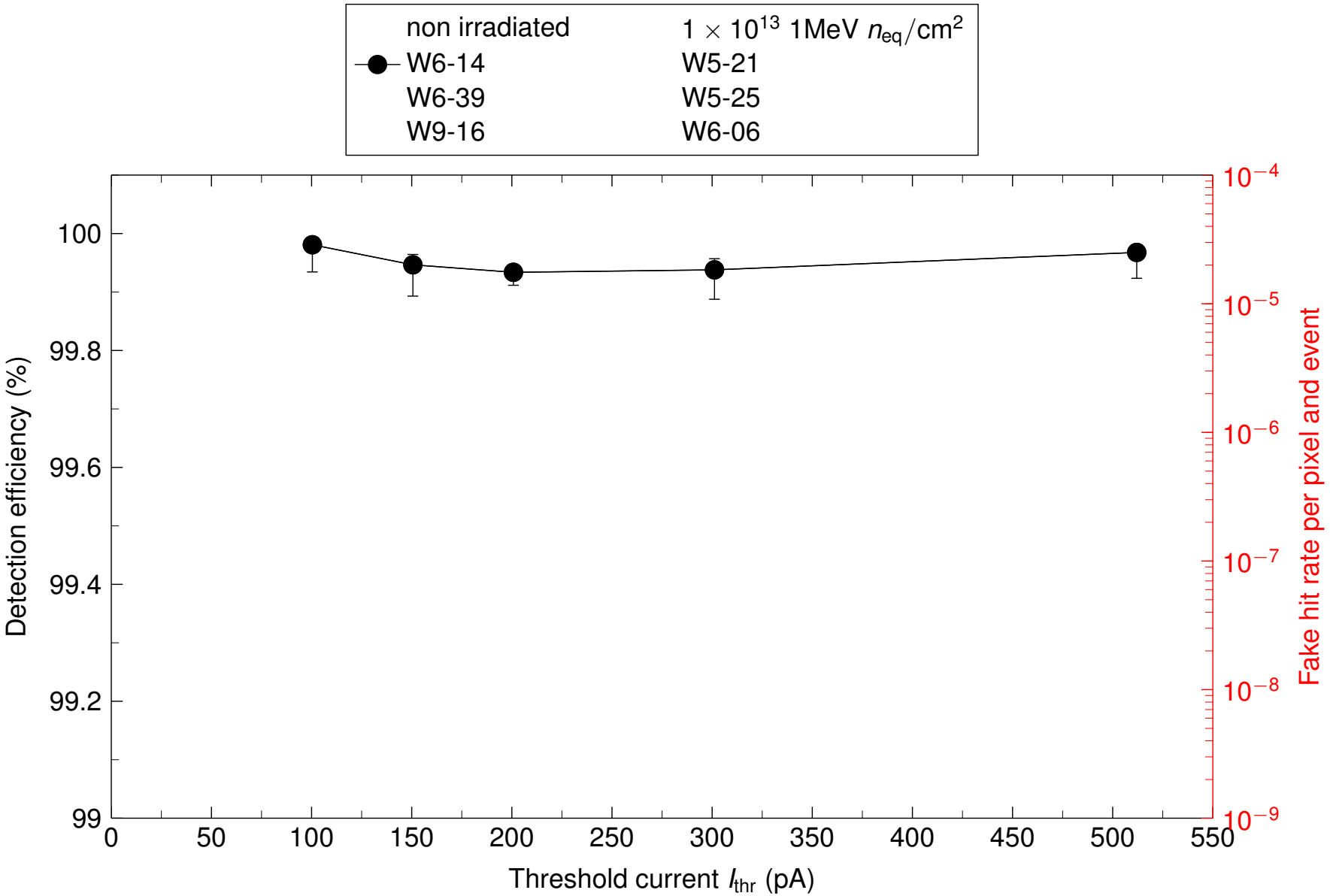
- **Many thanks to our colleagues from the host institutes for their excellent support!**



Detection efficiency



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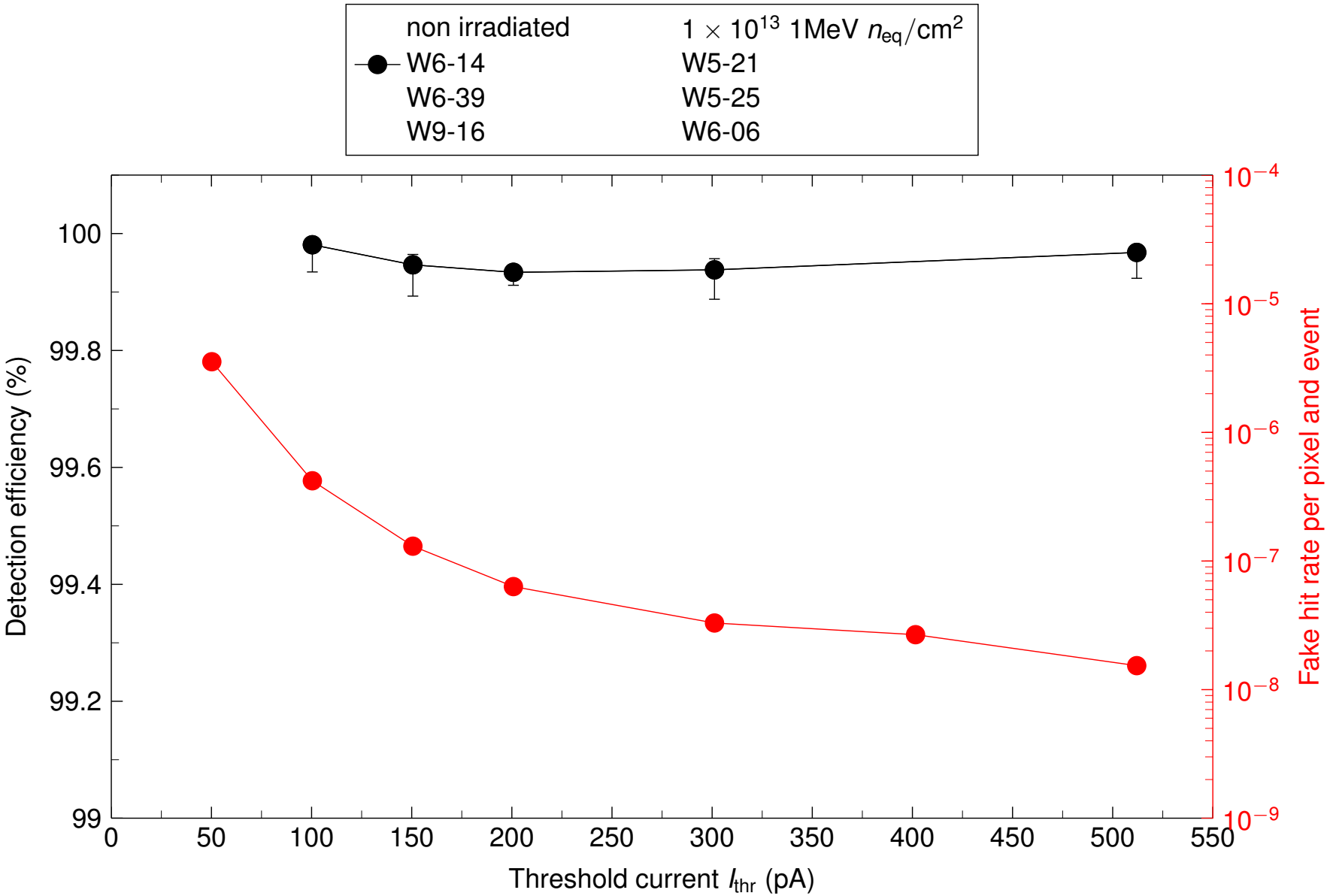

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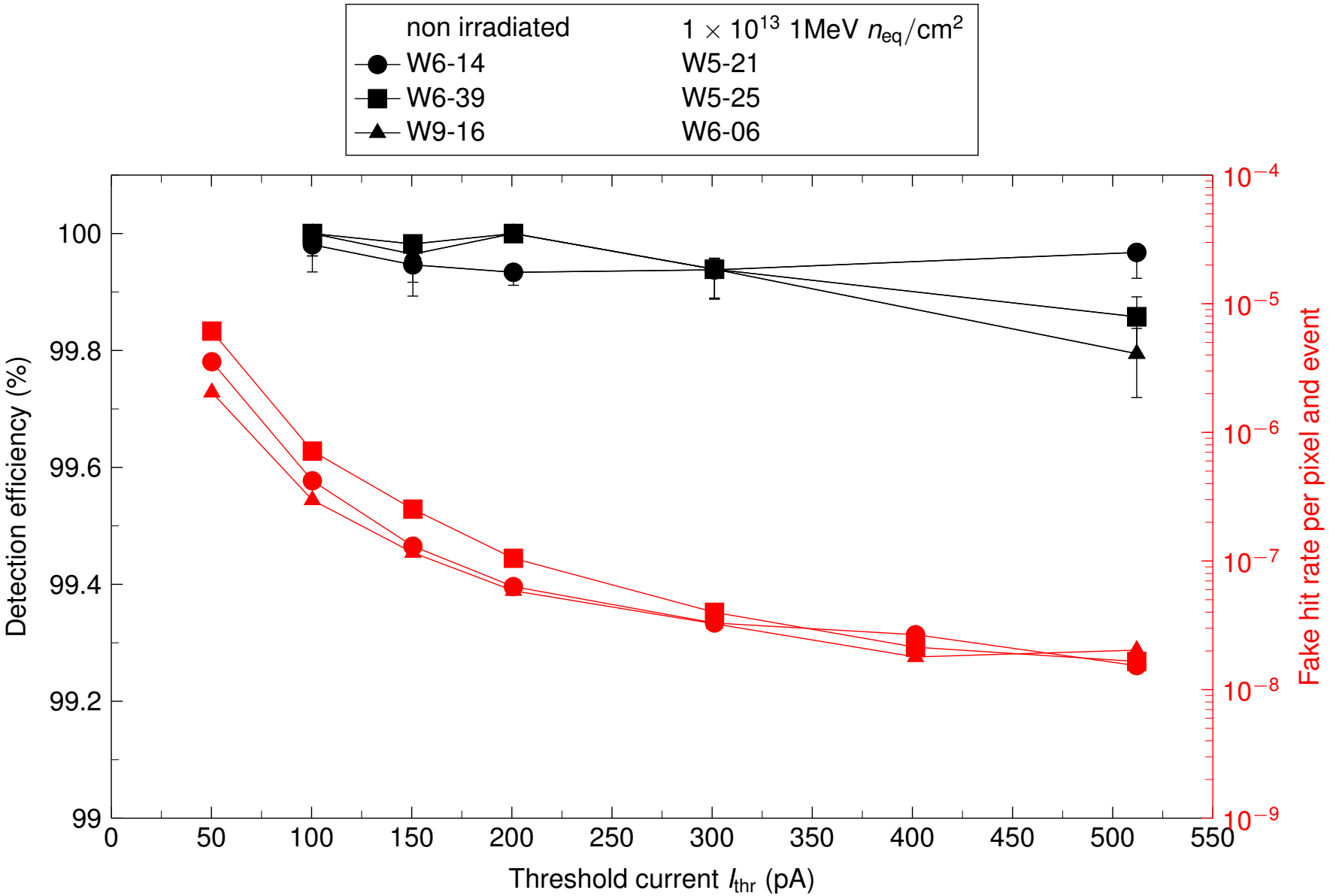

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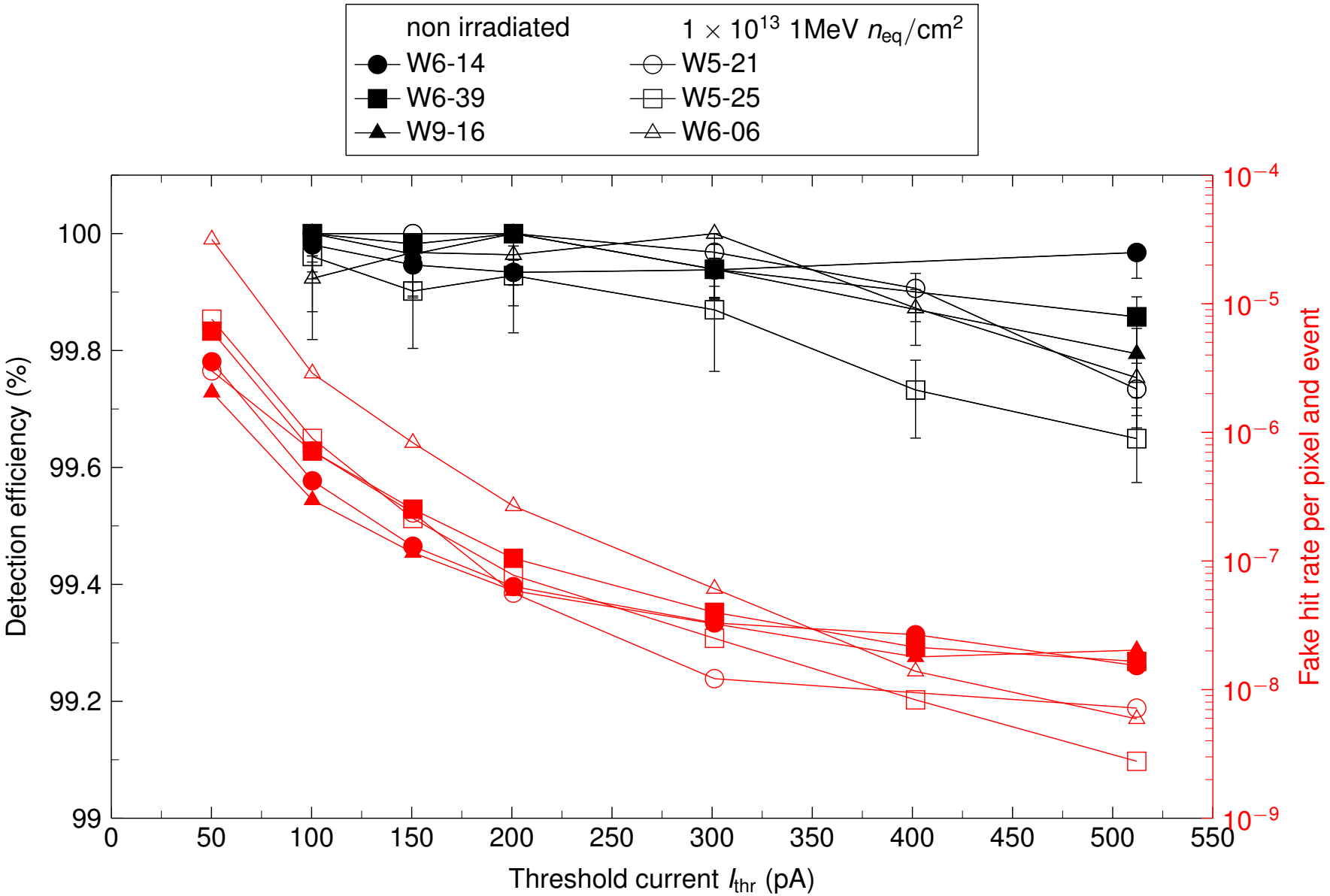
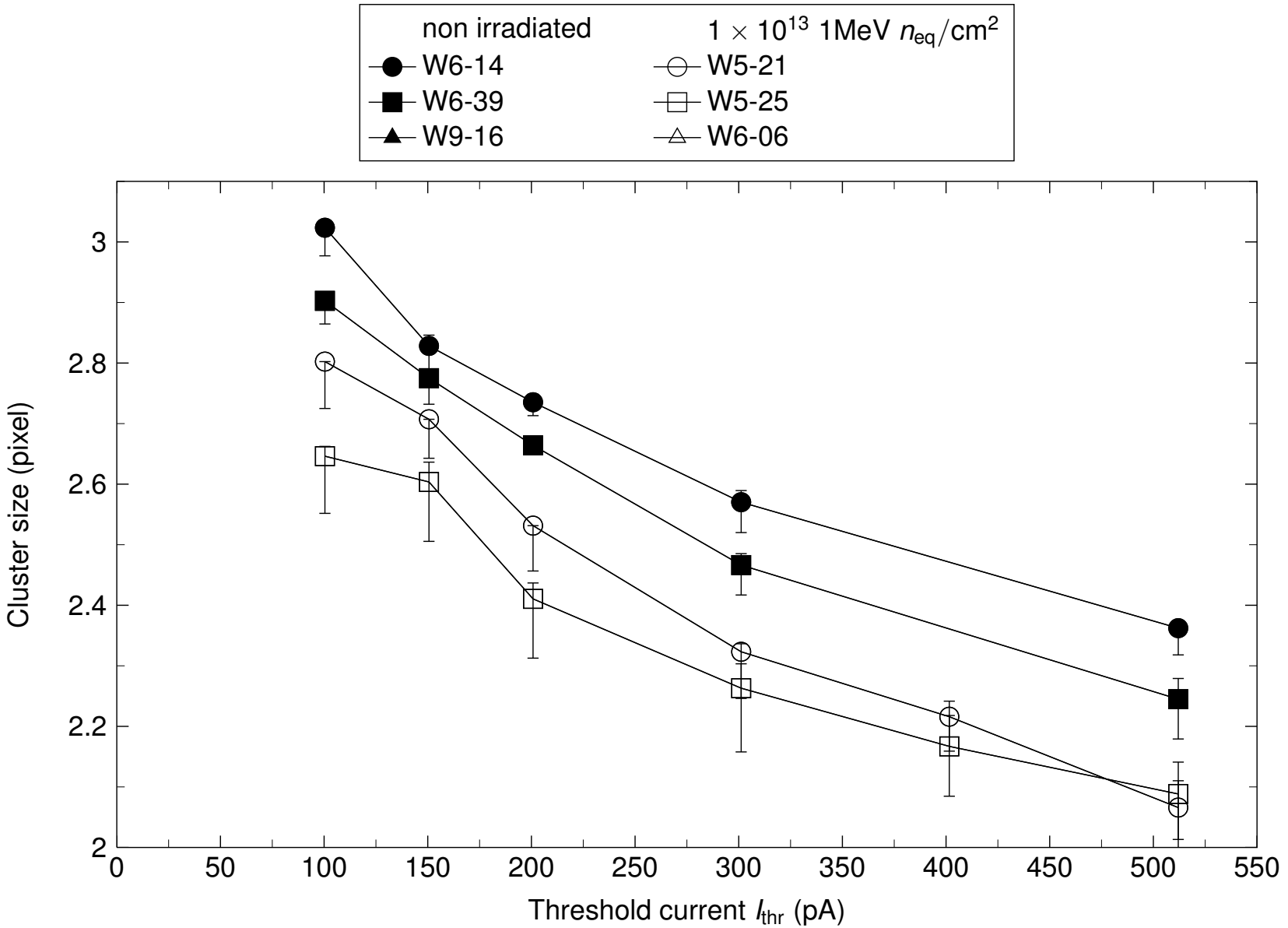
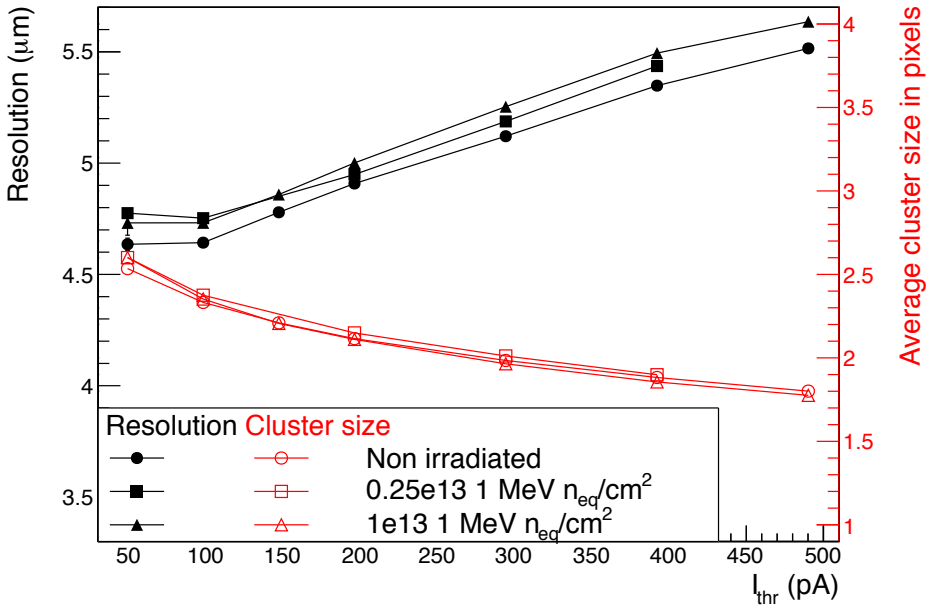


Cluster sizes



Spatial resolution



- Average cluster sizes of 1.5–3 pixels
- Spatial resolution of around 4.5 µm to 5.5 µm

Spatial resolution

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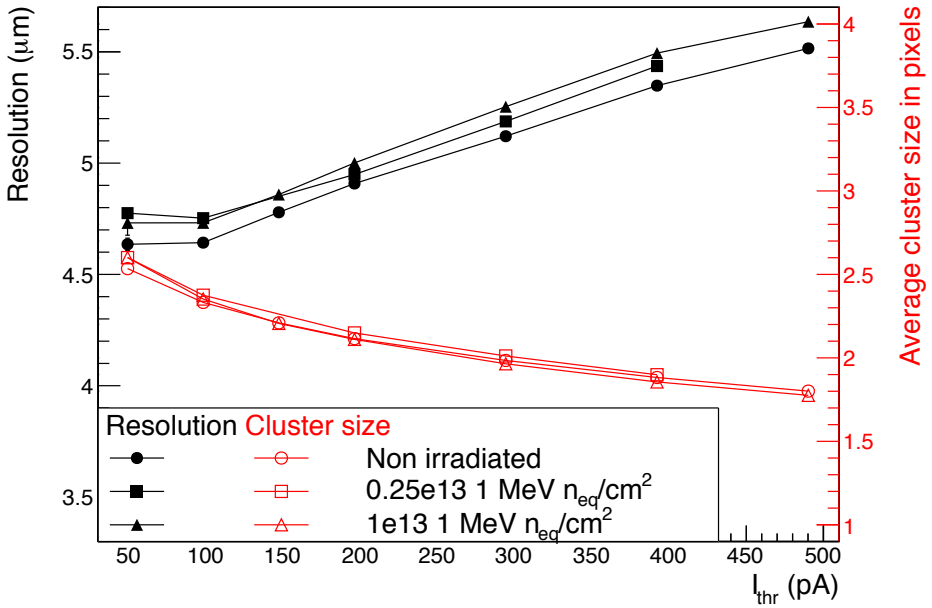
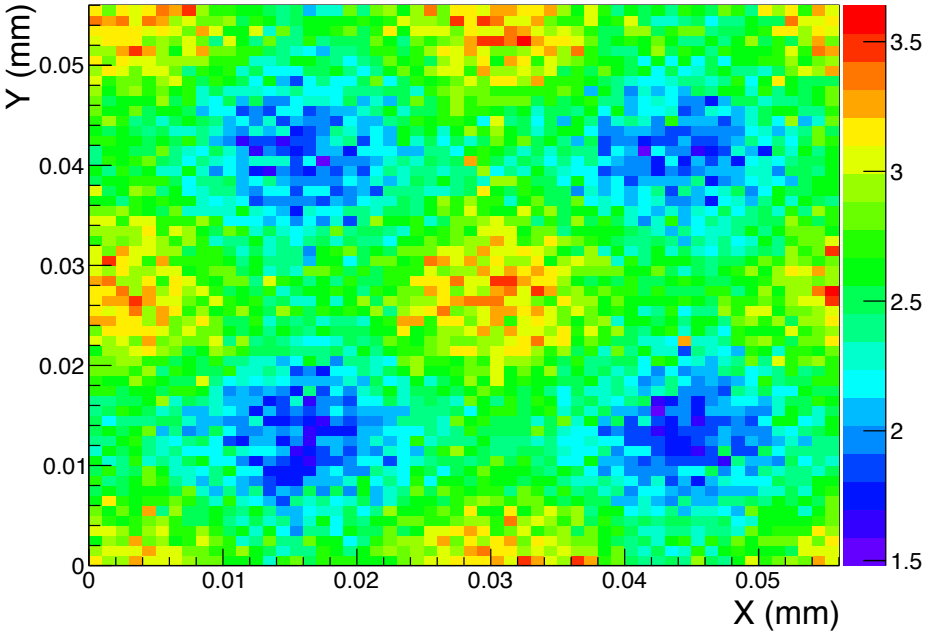


Cluster size



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⇝ Can use telescope tracking to study properties differential in track impinging point

- Cluster size varies nicely leading to good intrinsic resolution

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Summary & Outlook

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- Comprehensive R&D program is being carried out to develop and qualify a MAPS for the ALICE ITS upgrade
- Full-scale prototype chips show expected performance

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Outlook

- Remaining blocks are being integrated into the next generations of prototypes:
  - inclusion of inter-chip communication, enabling the fabrication of detector modules/staves:
    pALPIDE-2 (silicon received last month)
  - inclusion of high-speed link and multiple-event memories:
    pALPIDE-3 (about to be submitted for fabrication)
- Qualification of larger detector assemblies (modules, staves)
- Final submission of ~~p~~**ALPIDE**

The pALPIDE-1